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Analysis of Standard-MOS and Ultra-Low-Power Diodes Composed by SOI UTBB Transistors

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ABSTRACT The main objective of this work is to present an analysis of the performance of Ultra-Thin-Body and Buried Oxide transistors working as Ultra-Low-Power and standard-nMOS diodes. The implementation of different ground planes and substrate biases is analyzed. It is shown a reduced leakage current and increased ratio between the on and off-state currents for both systems with the nMOS devices' substrate biased at −2V. The standard-nMOS shows a reduced leakage current and increased ratio between the on and off-state currents with the substrate bias at −2 V and with a P-type ground plane implemented while the Ultra-Low-Power presents only a significative influence of the ground planes on the ratio between the on and off-state currents. The ground planes do not provoke a significant change in the leakage current, but a noticeable variation can be observed in the ratio between the on and off-state currents due to the higher threshold voltage in relation to the system without ground plane.

INDEX TERMS Ground plane, SOI, standard-MOS-diodes, ultra-low-power diodes, UTBB.

I. INTRODUCTION

The Ultra-Thin-Body and Buried Oxide (UTBB) has been proposed as an evolution of the SOI technology [1], and this SOI transistor presents silicon layer thickness (t_{Si}) on the order of 6-10 nm and buried oxide (BOX) thickness (t_{box}) on the order of 10-25 nm, resulting in a better capacitive coupling of the structure. The reduced t_{box} presented by UTBB transistors makes the substrate biasing (V_{SUB}) more effective acting as a second gate, significantly improving the control of the channel charges and allowing for the modulation of the threshold voltage (V_{TH}) according to the application. This enables the UTBB device to be used in multi-V_{TH} architectures [2]. Additionally, a ground plane (GP) region, which consists of a thin highly doped layer below the BOX layer, can be implemented to avoid substrate depletion-related effects.

These UTBB features are responsible for making the device suitable for low power analog [2] and RF [3] applications, and also in Ultra-Low-Power (ULP) systems [4], [5], [6], where low threshold voltage and low leakage current are required. One of these applications consists in RF diodes, frequently used in energy harvesting systems [7], [8], [9]. High performance diodes can be easily implemented in standard-MOS transistors by short-circuiting its drain and gate terminals whereas Ultra-Low-Power (ULP) diodes [10], [11] can be implemented in UTBB transistors by the application of Complementary MOS (CMOS) technology similarly to double-gate MOSFETs on RFID rectifiers [12]. To the best of our knowledge, the performance of UTBB devices working as standard and ULP diodes has not been studied in the literature. Therefore, this work presents an analysis of the main electrical characteristics of these devices considering different GP configurations and substrate biases. The work was carried out through numerical simulations validated with experimental data from literature. Section II presents the physical characteristics of the studied devices as well as the calibration of the simulations to experimental data. The electrical characteristics of both standard and ULP

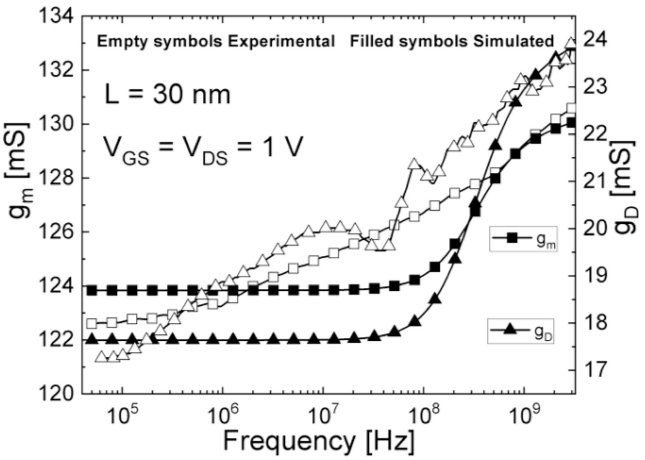

FIGURE 1. Simulated and experimental g_D and g_M versus frequency of the 30 nm-long UTBB n-MOSFET at $V_D = V_{GS} = 1$ V.

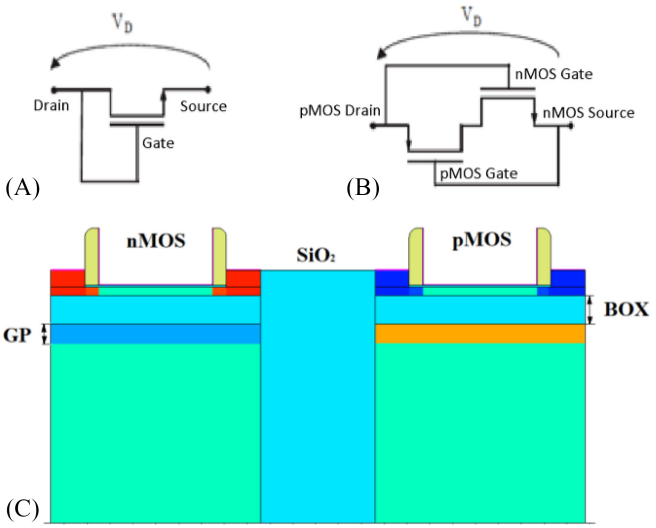

FIGURE 2. Electrical schematics of the diode implemented with a Standard nMOS device in (A), electrical schematics of the ULP diode in (B) and the longitudinal view of the CMOS device in (C).

UTBB diodes are presented and discussed in Section III, and overall conclusions of the work are highlighted in Section IV.

II. DEVICES CHARACTERISTICS AND APPLIED METHODOLOGY.

The analysis was carried out throughout devices DC and AC 2D simulations on the software Synopsys Sentaurus TCAD [13] calibrated to experimental data from literature. Models accounting for the carriers' generation and recombination [14], [15], bandgap narrowing [16], [17], low field mobility [18], [19] and the mobility dependence on vertical and longitudinal electric fields [20], [21] have been considered in all the simulations. For energy balance, the hydrodynamic transport mechanism, which also considers the impact ionization on the output characteristics, was used. It is worth to mention that the Self-Heating effect was not considered in this work.

Firstly, the simulations were calibrated to present characteristics near of experimental devices. Considering that the diodes operation in RF regime is essential for several applications, such as energy harvesting ones, the required figures of merit transconductance (g_M) and output conductance (g_D) were extracted through AC simulations as a function of the frequency and are presented in Fig. 1. To obtain these curves, simulations were performed with devices presenting characteristics similar to those described in [22], with Si film, BOX, channel length and effective gate oxide thickness of 7, 25, 30 and 1.3 nm, respectively. g_M and g_D curves from experimental devices are also presented in Fig. 1 along with the simulated curves. As one can observe, the simulated devices present AC behavior close to the one presented in [22] at the temperature of 300 K with the g_D presenting 18 and 22 mS at 50 kHz and 3 GHz, respectively, and g_M presenting 124 and 131 mS at the same frequencies. This assures that simulated devices are well matched in relation to the experimental ones. It is worth to mention that validation of the simulations for DC drain-voltage characteristics was presented in detail in previous works [23], [24].

The simulations were extended to devices with channel lengths of 100 and 25 nm for the implementation of the diodes. The standard-MOS had the gate and the drain terminals of a nMOS device short-circuited as exhibited in Fig. 2A, and for the ULP structure the CMOS scheme shown in Fig. 2B was applied. The gate of the pMOS device is connected to the source terminal of the nMOS one, which had its gate terminal tied with the drain terminal of the pMOS transistor as shown in Fig. 2B. For the devices with the GP implemented, in the ULP ones was considered a P-type GP for the nMOS device and a N-type GP for the pMOS device [2], both with the thickness of 10 nm and $1x10^{18}$ cm^{-3} of P and N doping materials. The nMOS and the pMOS are separated by a 100 nm long layer of SiO_2 acting like a Shallow-Trench-Isolation (STI) that isolates the devices from the top source-drain regions until the bottom substrate in order to allow the individual substrate biasing as shown in the scheme of Fig. 2C.

III. ELECTRICAL ANALYSIS AND DISCUSSIONS

A. STANDARD AND ULP DIODES UNDER DIFFERENT SUBSTRATE BIASES

Firstly, to verify the standard-nMOS UTBB device without GP (No GP) operating as a diode, simulations were performed applying a voltage (V_D) from -1 to 1 V. Fig. 3 A shows the diode absolute current ($|I_D|$) as a function of the applied V_D for different substrate biases and two gate lengths. As UTBB devices allow an independent back gate biasing, different V_{SUB} were considered and a special condition was also considered, where the substrate is connected with the already tied gate and drain terminals ($V_{SUB} = V_{GS} = V_D$). It is worth to mention that in this case, the back gate bias will vary dynamically with the gate voltage. This condition could be interesting to avoid the need of an external supply source. It is observed that the

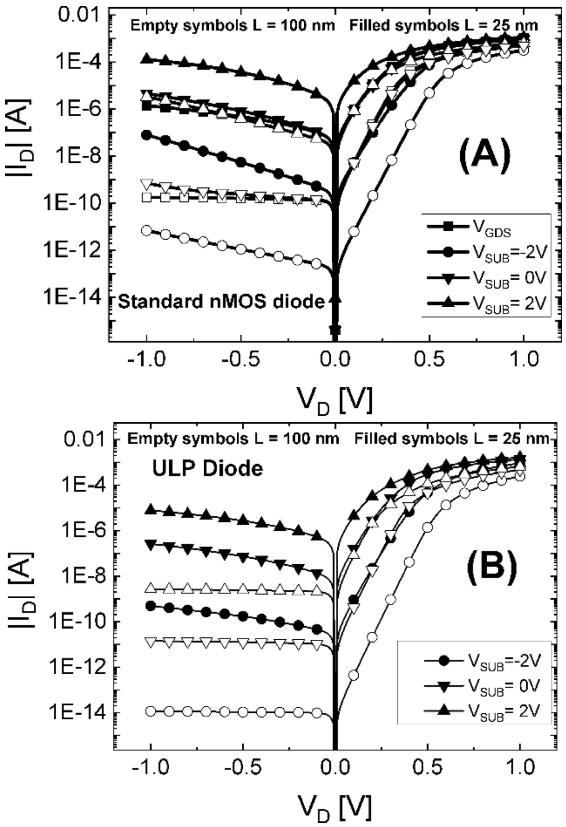

FIGURE 3. $|I_D|$ vs. V_D with different substrate bias for L = 100 and 25 nm standard-nMOS (A) and ULP (B) diodes without GP.

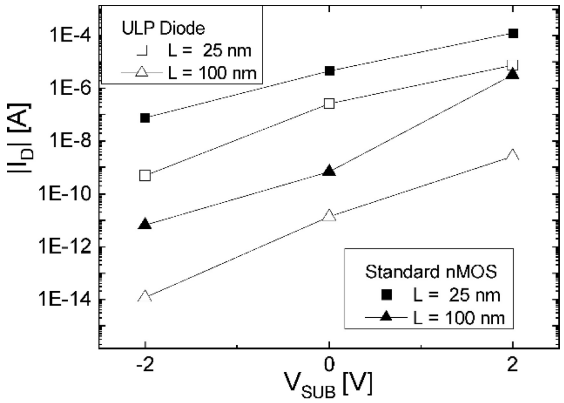

FIGURE 4. $|I_D|$ vs. V_{SUB} for ULP and Standard-nMOS devices without GP composed by devices with L = 25 and 100 nm for $V_D = -1$ V.

25 nm-long device presents higher leakage current levels than the 100 nm long one. With respect to the back biasing conditions, the devices with the substrate biased with 2 V present higher leakage current level for both channel lengths. The $V_{SUB} = V_D$ condition comes in the sequence and shows a behaviour similar to the substrate with zero bias, and the substrate biased at -2 V presents the lowest leakage current, which is in the order of 7 pA and 0.7 nA for the L = 100 and 25 nm devices, respectively, at $V_D = -1$ V.

To evaluate the performance of the ULP diode implemented with devices without GP, the same analysis was performed in a set of different substrate bias. In this case, V_{SUB} refers to voltage applied to the substrate of the nMOS device whereas the substrate of the pMOS receives the opposite voltage, i.e., if -2 V is applied to the substrate of the nMOS, 2 V is applied to the pMOS. This configuration was adopted based on previous results for CMOS circuits compounded by UTBB devices [25]. It is worth to mention that for $V_{SUB} = 0$ V, the substrates of both devices are tied to the ground. The substrate was biased with -2, 0 and 2 V. Fig. 3B presents the curves of the absolute current ($|I_D|$) as a function of the applied V_D. for the ULP structure. One can note the reduction of the leakage current with the reduced substrate bias, this effect could be related to the change in the capacitive coupling of the structures promoted by the application of the back gate bias, which will be discussed later this work.

To compare the results of both diode configurations, Fig. 4 presents the curves of the leakage current as a function of the substrate bias for $V_D = -1$ V. Taking the condition where the devices present the higher leakage current levels, i.e., $V_{SUB} = 2$ V, the ULP structure presents leakage current on the order of 7 μA and 3 nA while the standard-nMOS structure presents 130 μA and 3 μA for the 25 and 100 nm long devices structures, respectively. In relation to the channel length, the 25 nm long ULP diode presents leakage current value next to the one observed in the standard-nMOS diode. Additionally, shorter devices present higher leakage current levels in both structures.

The I_{ON}/I_{OFF} ratio is an important figure that correlates the performance of the diodes in terms of their on- and off-state currents [26]. To obtain these curves, the currents in the interval from 0.5 to 1 V of V_D (on-state) were divided by the current on the interval of V_D between -1 V and -0.5 V (off state). This was done to consider the application of a symmetric sinusoidal signal at the diode. Thus, Fig. 5A shows the I_{ON}/I_{OFF} of the diode implemented with the standard-nMOS device without GP. It is shown that the 25 nm device presents lower I_{ON}/I_{OFF} ratio in relation to the 100 nm device and, when the substrate is biased at -2 V, both devices present the larger I_{ON}/I_{OFF} ratio followed by the zero bias substrate and the $V_{SUB} = V_D$ configuration. The lower I_{ON}/I_{OFF} conditions are given by the substrate biased at 2 V, where values on the order of $5x10^2$ and $1x10^1$ for the 100 and 25 nm channel length devices are obtained.

Fig. 5B shows the I_{ON}/I_{OFF} of the ULP diode implemented with devices without GP as a function of $|V_D|$. As one can observe, the 25 nm device-based ULP presents lower I_{ON}/I_{OFF} ratio in relation to the 100 nm one. When the substrate is biased at -2 V and $|V_D| = 1$ V, both devices present the larger I_{ON}/I_{OFF} ratio while the lower I_{ON}/I_{OFF} conditions are given by the substrate biased at 2 V and $|V_D| = 0.5$ V. Fig. 6 shows the I_{ON}/I_{OFF} at 0.5 and 1 V of $|V_D|$ as a function of the substrate bias. Higher values are obtained for the longer ULP devices in the order of 7×10^{10} and 4×10^9 for $|V_D|$ of 1 and 0.5 V at $V_{SUB} = -2$ respectively,

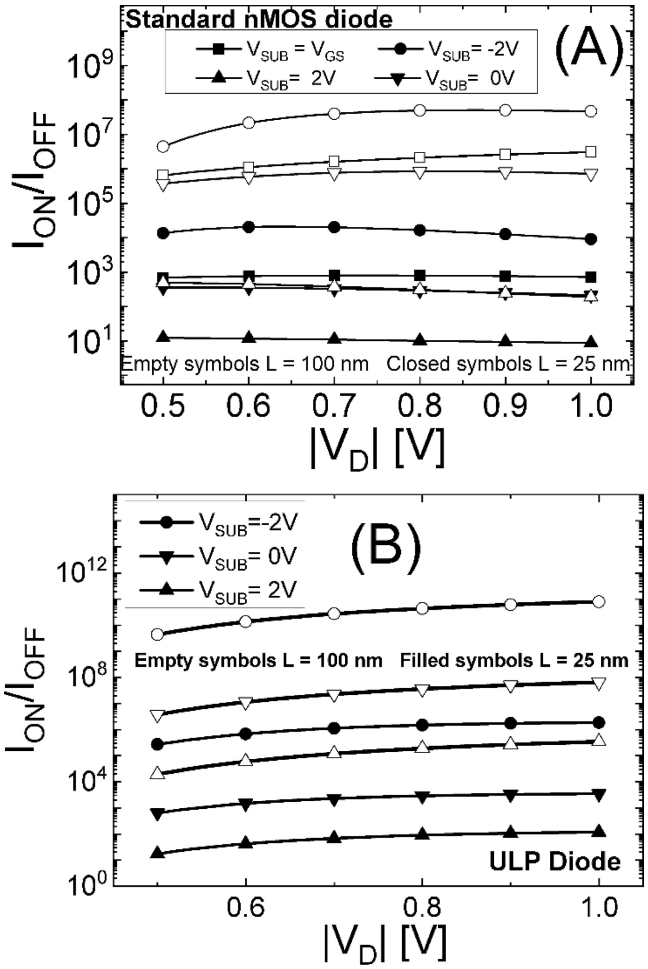

FIGURE 5. I_{ON}/I_{OFF} ratio vs V_D with different substrate bias for L = 100 and 25 nm standard-nMOS (A) and ULP (B) diodes without GP.

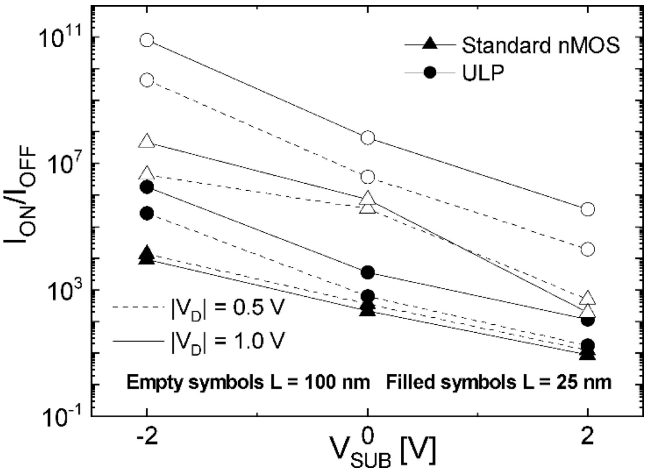

FIGURE 6. I_{ON}/I_{OFF} vs. V_{SUB} for ULP and Standard-nMOS devices without GP for $|V_D|$= 0.5 and 1 V.

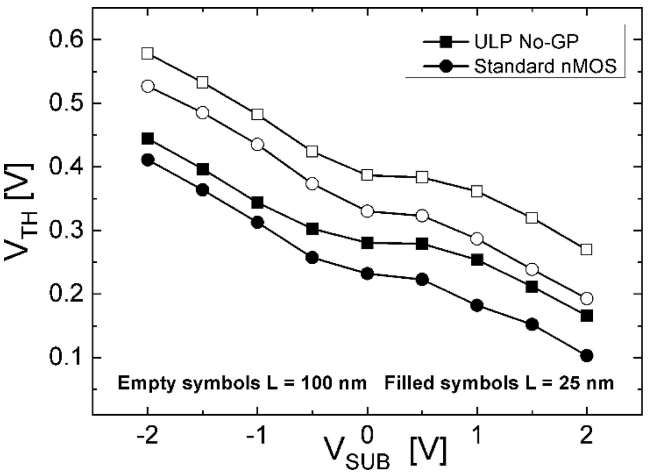

FIGURE 7. Threshold voltages (V_{TH}) vs V_{SUB} for standard-nMOS and ULP diodes for L = 100 and 25 nm devices.

while the longer standard-nMOS devices exhibits 5×10^7 and 4×10^6 at the same bias conditions. To better visualize the differences between the devices, Table 1 shows a comparison of the ratio for the L = 25 nm devices. It is also interesting to note a reduction of the ratio between 1 and 0.5 V of $|V_D|$ for the ULP in all substrate bias and for the longer standard-nMOS device biased at the smaller substrate bias, indicating increased dependence of $|V_D|$ for the devices on these conditions which could be related to the threshold voltage of the devices that will be discussed later this work.

To elucidate the behavior behind the difference in I_{ON}/I_{OFF} ratio, the threshold voltage (V_{TH}) for each substrate bias conditions was extracted through the method described in [27] and is presented in Fig. 7 for both standard-nMOS and ULP devices. As one can note in Fig. 7, the standard-nMOS exhibits lower V_{TH} in relation to the ULP structure. With respect to the substrate bias, the lower the V_{SUB} bias condition, the higher V_{TH} is observed for both diode types. This effect is related to the change in the surface potential in the second interface, i.e., the interface between the channel and the BOX, at each step of the substrate bias.

B. EFFECT OF THE GROUND PLANE (GP)

Figs. 8 and 9 present the same analysis for different GP types for the standard-nMOS and for the ULP diodes. In Fig. 8, it is shown that, for $V_{SUB} = -2$ V, the shorter device does not present a substantial change in the leakage current for different GPs, whereas the 100 nm long device with the P-type GP presents lower leakage than the N-type and the No-GP ones. For the zero bias substrate configuration, the P-type GP device presents lower leakage current followed by the No-GP and the N-type GP configurations. For the shorter device, leakage currents of 20, 5 and 2 μA are observed at $V_D = -1$V for the N-type, No-GP and P-type, respectively. In the 100 nm device, a reduction of the leakage current with the V_D increasing from -1 to 0 V for the P and N-type GPs can be observed. However, the No-GP exhibits a lower leakage current dependence on V_D for the same biasing interval. For the substrate biased at 2 V, one can note the same leakage current levels for the different GP configurations in both devices, although the leakage current

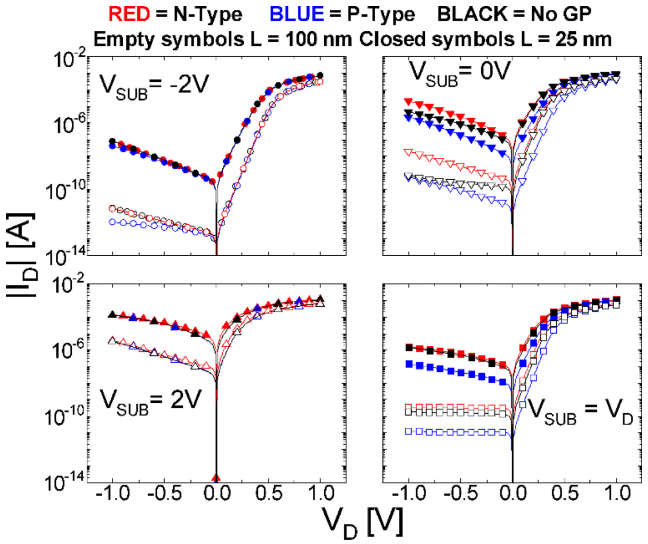

FIGURE 8. $|I_D|$ vs. V_D with different substrate bias for L = 100 and 25 nm standard-nMOS devices with different GPs.

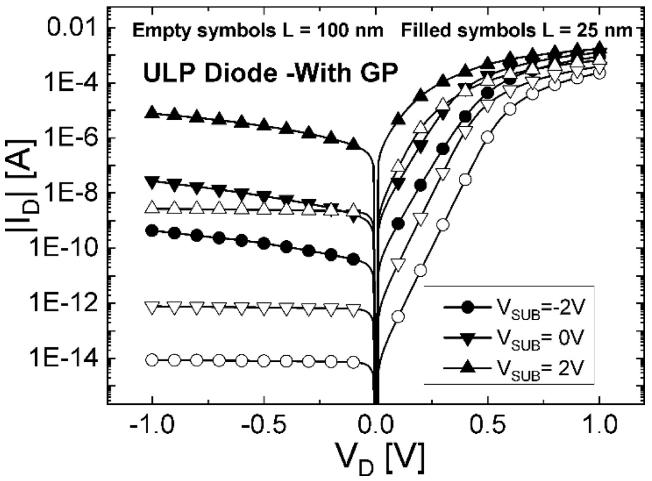

FIGURE 9. $|I_D|$ vs. V_D with different substrate bias for L = 100 and 25 nm ULP devices with GP.

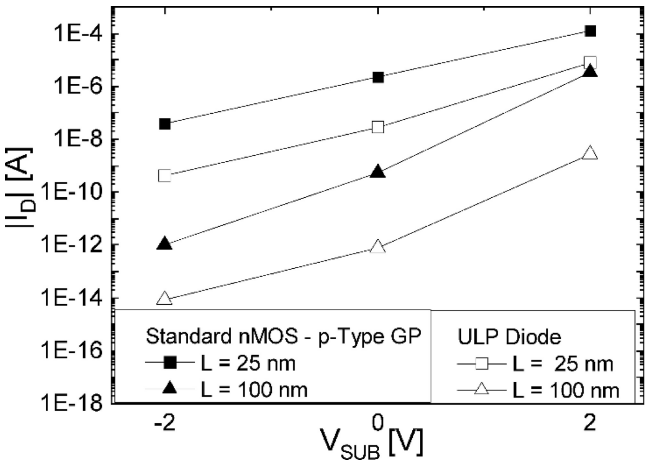

FIGURE 10. $|I_D|$ vs. V_{SUB} for ULP and Standard-nMOS devices with GP for $V_D = -1$ V.

is higher for L = 25 nm, as expected. Finally, when analyzing the case in which the substrate bias is connected to the gate, it is possible to observe that N-type GP and No-GP devices present similar leakage current levels whereas the P-type one presents the lower current for both 25 and 100 nm channel devices.

For ULP diodes implementation of the GPs, the high-V_{TH} (HVT) specific condition is achieved with the application of a P-type GP in a nMOS device and a N-type GP in a pMOS device [4]. Thus, the simulations were performed in devices composing a CMOS scheme with the GPs configurations under these conditions. Fig. 9 presents the curves for the ULP structure with GP and, as one can observe, its implementation in the ULP diode did not provoke a substantial change in the leakage current levels when compared to the No-GP ULP shown in Fig. 3 B. In the same way, the behavior with respect to the substrate bias and the channel length is similar to the one for the structure without GP, i.e., reduction of the leakage current with the reduced V_{SUB} bias and the lower leakage current for longer devices.

Fig. 10 presents the curves of the leakage current as a function of the substrate bias for $V_D = -1$ V for the standard nMOS device with P-type GP, where the lowest leakage current levels were observed, and for the ULP diode. The latter repeats the trend observed with the absence of GP, exhibiting lower leakage currents levels. Taking the condition with the highest current levels, $V_{SUB} = 2$ V, the ULP structure shows 8 μA and 3 nA for the 25 and 100 nm devices, respectively, while the standard-nMOS presents 130 μA and 3 μA at the same conditions. The influence of the GP on the overall current of the standard-nMOS and ULP diodes is correlated to the variation of the potential close to the BOX and to the different work functions of the GP layer [28], [29]. For devices with N-type GP, the flatband voltage of the BOX interface (V_{fb2}) is about -0.76 V and for P-type GP, $V_{fb2} = 0.18$ V, while both diodes without GP presents $V_{fb2} = 0$ V. For that reason, the interface between channel and BOX in the standard-nMOS devices with N-type GP, in $V_{SUB} = V_{GS}$ and the ULP diodes without GP start to deplete for lower V_D.

Fig. 11 shows the I_{ON}/I_{OFF} analysis for the standard-nMOS devices with different GPs. One can observe higher I_{ON}/I_{OFF} ratios for the P-type GP devices with respect to the other ones. The only exception is when the substrate is biased at 2 V where there is no difference in the ratio between the GPs. The N-type and the No-GP present similar I_{ON}/I_{OFF} behavior for almost all substrate biasing, except for $V_{SUB} = 0$ V where the N-type presents the lower ratio.

Fig. 12 shows the I_{ON}/I_{OFF} analysis for the ULP devices with GPs as a function of $|V_D|$. One can observe the same behavior with respect to the No-GP structure: the longer devices present higher I_{ON}/I_{OFF} ratio in relation to the shorter one, and the lower ratio is observed when the substrate is biased at 2 V and $|V_D| = 0.5$ V. In this poorer condition,

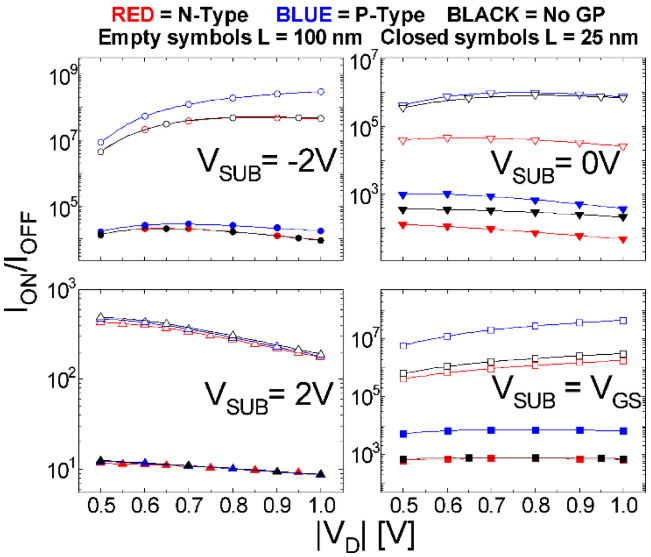

FIGURE 11. $|I_D|$ vs. V_{SUB} for Standard-nMOS devices with GP.

TABLE 1. I_{ON}/I_{OFF} ratio comparison between ULP and standard-nMOS diodes for L = 100 and 25 nm devices.

Biasing Condition	L = 25 nm			
	ULP ($\|V_D\|$=0.5 V)	ULP ($\|V_D\|$=1.0 V)	Standard ($\|V_D\|$=0.5V)	Standard ($\|V_D\|$=1.0V)
V_{GDS}			7×10^{2}	7×10^{2}
V_{SUB} = -2 V	3×10^{5}	2×10^{6}	1×10^{4}	1×10^{4}
V_{SUB} = 0 V	6×10^{2}	3×10^{3}	3×10^{2}	2×10^{2}
V_{SUB} = 2 V	2×10^{1}	1×10^{2}	1×10^{1}	0.9×10^{1}

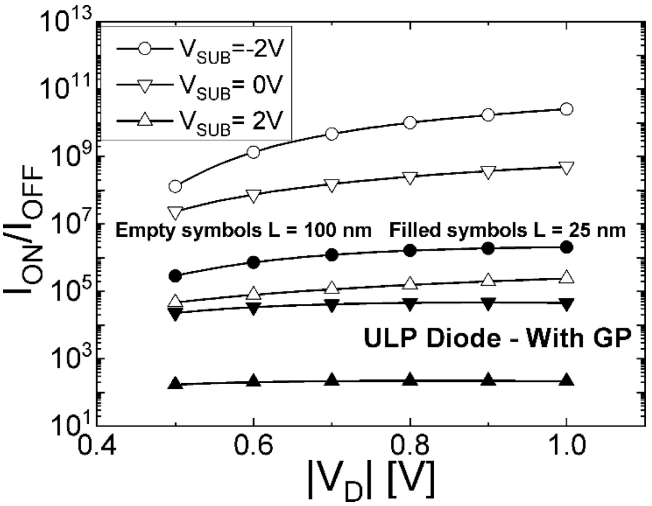

FIGURE 12. I_{ON}/I_{OFF} ratio vs V_D with different substrate bias for L = 25 and 100 nm.

the implementation of the GP presents an increase in the ratio with respect to the No-GP structure. This is seen especially for the shorter device. While the No-GP ULP with L = 25 nm exhibited $I_{ON}/I_{OFF} = 2\times10^{1}$, the GP scheme improved it to 2×10^{2}. However, it is also interesting to note that the decrease of the ratio in the interval between

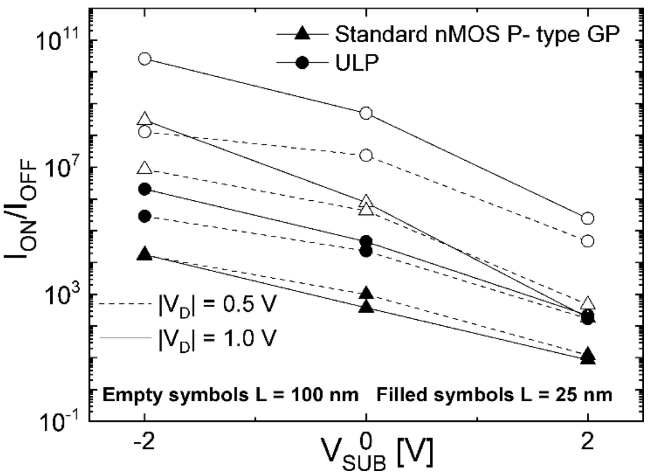

FIGURE 13. I_{ON}/I_{OFF} vs. V_{SUB} for ULP and Standard-nMOS devices of L = 25 and 100 nm with GP for $|V_D|$= 0.5 and 1 V.

TABLE 2. Threshold voltages (V_{TH}) for the standard-nMOS diodes with different GP and substrate bias for L = 100 and 25 nm devices.

Biasing Condition	L = 100 nm V_{TH} [V]			L = 25 nm V_{TH} [V]		
	N-Type	*P-Type*	*No GP*	*N-Type*	*P-Type*	*No GP*
V_{GDS}	0.289	0.378	0.317	0.204	0.281	0.224
V_{GD} V_{SUB} = -2 V	0.525	0.530	0.527	0.413	0.415	0.411
V_{GD} V_{SUB} = 0 V	0.314	0.416	0.330	0.225	0.307	0.232
V_{GD} V_{SUB} = 2 V	0.155	0.192	0.193	0.076	0.109	0.103

0.8 and 0.5 V of $|V_D|$ is more pronounced in this case. For the No-GP ULP with L = 100 nm devices biased at $V_{SUB} = -2$ V, an I_{ON}/I_{OFF} reduction from 4×10^{10} to 4×10^{9} is observed, whereas the ULP with GPs present a lowering from 1×10^{10} to 1×10^{8} indicating an accentuated dependence of the ratio with $|V_D|$ on the ULP devices with GP. In Fig. 13, which compares the I_{ON}/I_{OFF} ratio obtained for both structures taking the condition where the standard-nMOS devices present the higher ratio (P-type GP), the ULP structure shows a ratio of 2×10^{10} down to 1×10^{8} and 2×10^{6} down to 3×10^{5} for the 100 and 25 nm long devices at $V_{SUB} = -2$ V and $|V_D|$ of 1 and 0.5 V respectively, while the standard-nMOS presents 3×10^{8} down to 8×10^{6} for the 100 nm long device and the shorter one exhibits 2×10^{4} for both $|V_D|$ at the same analysis.

Fig. 14 and Table 2 presents the threshold voltage as a function of the substrate bias for both ULP and standard diodes with and without ground planes. As seen in Table 1, the longer standard-nMOS P-type GP devices exhibit higher V_{TH} followed by the No-GP and the N-type GP. A noticeable difference can be observed in the ULP diodes with substrate bias between 0 and −2 V where the ULP diodes with GP present higher V_{TH} than the ones without GP. This explains the greater shift in the I_{ON}/I_{OFF} ratio in the longer devices with GP making them more dependent on V_D. The influence of the GP on V_{TH} of the standard-nMOS and ULP diodes is correlated to the variation of the potential close to the BOX as explained before. Standard-nMOS devices with P-type GP

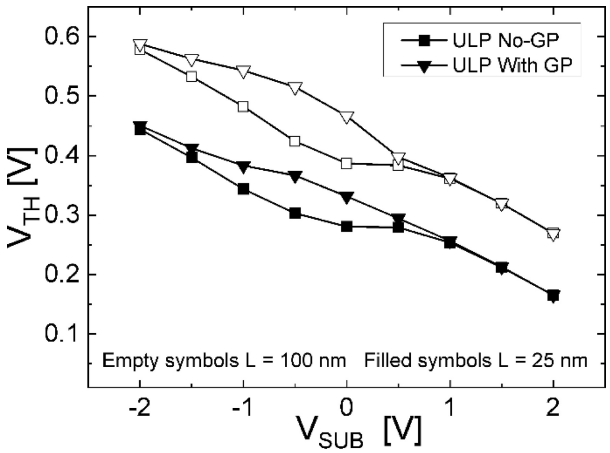

FIGURE 14. Threshold voltages (V_{TH}) vs V_{SUB} for standard-nMOS and ULP diodes for L = 100 and 25 nm devices.

presents the higher flat-band voltage (0.18 V) benefiting the higher V_{TH}. For that reason, the interface between channel and BOX in the standard-nMOS devices with N-type GP, in $V_{SUB} = V_{GS}$ and the ULP diodes without GP presents smaller V_{TH} and higher leakage current.

IV. CONCLUSION

This work has evaluated the performance of UTBB transistors operating as standard-nMOS and Ultra-Low-Power diodes for the first time. The overall analysis has shown that the Ultra-Low-Power diode without ground plane presents a better performance than the standard-nMOS, although it presents a higher threshold voltage. Both systems composed by longer devices present lower leakage current and higher ratio between the on- and off-state currents. Additionally, the nMOS UTBB biased at lower substrate values also present lower leakage current and higher ratio between the on- and off-state currents. The ground planes implementation produces a reduced leakage current and increased ratio between the on- and off-state currents in the standard-nMOS diode with P-type GP, and when the substrate is connected to the drain contact, while the Ultra-Low-Power diodes do not present a significative influence of the ground planes. However, for the ratio between- the on and off-state currents, the ground plane provokes a substantial change for both systems.

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