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Rectifying Schottky Contact in ZrN/Polycrystalline p-Ge

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ABSTRACT Fermi-level pinning (FLP) at the metal/Ge interface makes it difficult to control the Schottky barrier height, which forces an ohmic behavior on p-Ge and a rectifying behavior on n-Ge. This study first demonstrates the rectifying behavior on polycrystalline (poly) p-Ge on a glass substrate, using sputter-deposited ZrN contacts under 350 °C process. The rectifying characteristics depend on the poly-Ge quality derived from the grain size and the defect-induced acceptor density. The highest quality Ge is formed by solid-phase crystallization (SPC) of amorphous Ge deposited at 125 °C and exhibits the lowest reverse leakage current as well as the highest hole (the lowest electron) barrier comparable to a single-crystal Ge substrate. In contrast, the Zr contact exhibits ohmic behavior, suggesting the importance of ZrN in alleviating FLP. The forward and reverse currents are determined by Ge resistance and grain boundaries in Ge, respectively. These technologies will further aid the development of electronic devices on glass or plastic substrates with low heat resistance, including n-channel thin-film transistors.

INDEX TERMS Low-temperature process, polycrystalline Ge, rectifying contact, Schottky barrier diode, ZrN.

I. INTRODUCTION

Low-Temperature processed complementary metal-oxide-semiconductor (CMOS) devices are crucial for the application of high-performance 3-dimensional large-scale integrated circuits and high-functionality mobile terminals. Ge is a promising material for these applications, with lower crystallization temperature, higher carrier mobility for both electron and hole, lower grain boundary (GB) barrier than Si, and compatibility with conventional Si processing.

Research efforts have focused on the low-temperature synthesis of polycrystalline (poly-) Ge films using solid-phase crystallization (SPC) [1], [2], [3], [4], [5], laser annealing [6], and metal-induced crystallization [7], [8], [9], [10]. In addition, recent developments in Ge-MOS field-effect transistor (FET) technology [11], [12], [13], [14] have demonstrated poly-Ge thin-film transistors (TFTs). However, TFT performance is limited by poly-Ge film quality, having

a high hole concentration p because of defect-induced acceptors and a low Hall hole mobility μ derived from GB scattering. Our recently developed SPC method using a densified amorphous (a-) Ge precursor changed the Hall carrier mobility of poly-Ge to 690 cm²/Vs for holes [15], [16] and to 370 cm²/Vs for electrons [17], [18]. Furthermore, we have demonstrated accumulation-mode p-channel TFTs based on SPC-Ge with a high field-effect mobility (170 cm²/Vs) [19].

For n-channel Ge-TFTs in CMOS applications, source/drain (S/D) contacts with a low electron barrier are indispensable, including the metal contacts on n⁺-Ge for pn junction S/D or on p-Ge for Schottky S/D. However, the metal/Ge interface forms a high electron (low hole) barrier regardless of the metal work function due to Fermi-level pinning (FLP) near the valence band edge of Ge [20], [21]. Therefore, most metal contacts exhibit ohmic behavior on p-Ge and rectifying behavior on n-Ge.

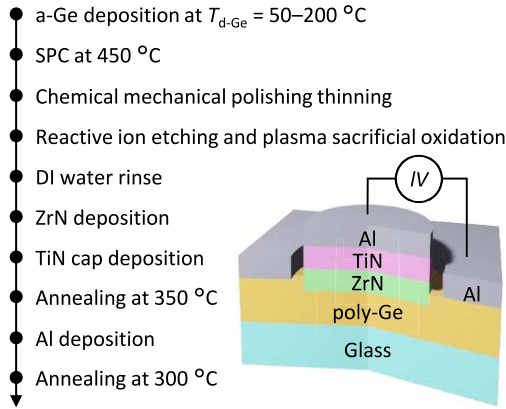


FIGURE 1. Fabrication process flow and schematic of the lateral poly-Ge SBDs.

Single-crystal Ge substrates have been used to study how to alleviate FLP in metal/Ge contacts. This has been realized by inserting thin-film interlayers (Ge_3N_4 [22], MgO [23], TiO_2 [24], [25], ZnO [26], a-Ge [27], $\text{TiO}_2/\text{GeO}_2$ stack [28], and SiGeSn [29]) between the metal and Ge, terminating the interface state with fluorine [30] and sulfur [31], growing epitaxial metals (Fe_3Si [32] and NiGe [33]), and using low electron density metals (GdGe_x [34] and Bi [35]). We successfully fabricated rectifying Schottky barrier diodes (SBDs) using direct sputter-deposited metal nitrides on single-crystal p-Ge substrates [36], [37], [38], [39], [40]. This was done because the N-containing amorphous-interlayer (a-IL) alleviates FLP [38]. Particularly ZrN/single-crystal p-Ge SBDs were shown to exhibit low electron (high hole) barriers [39]. Conversely, these metal contacts on poly-Ge have yet to be studied, let alone achieved low electron barrier, due to the low quality of conventional poly-Ge.

In this study, we first demonstrate rectifying ZrN/poly p-Ge SBDs using our SPC and contact formation technique. We then clarify the correlation between the SBD and poly-Ge properties. These results open the possibility of Schottky barrier control in poly-Ge and provide useful findings for all poly-Ge-based electronic devices, including n-channel TFTs.

II. SAMPLE PREPARATION

We fabricated lateral SBDs on poly p-Ge formed by SPC with the process and structure shown in Fig. 1. The a-Ge layers (100 nm thick) on SiO_2 glass substrates were deposited using the Knudsen cell of a molecular beam deposition system. The deposition temperature $T_{d-\text{Ge}}$ ranged from 50 to 200 °C. The samples were annealed in N_2 at 450 °C for 5 h to induce SPC. The SPC-Ge layers were thinned to approximately 55 nm by a chemical mechanical polishing (CMP) system, consisting of a rotating polishing pad and a sample carrier with the addition of a slurry, assuming the fully-depleted devices [19]. The photoresist was patterned into an open circular window (radius $r_1 = 25\text{--}200 \mu\text{m}$), and reactive ion etching (RIE) (16 nm depth) was performed for

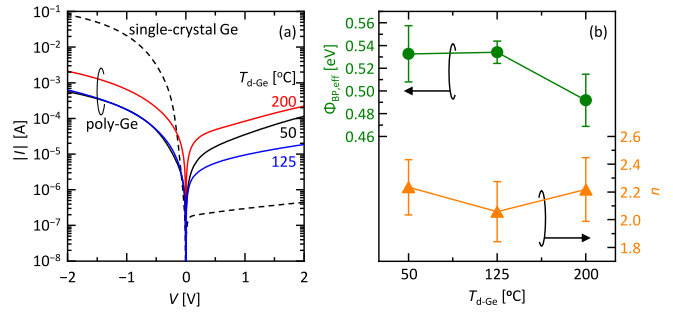


FIGURE 2. Electrical properties of ZrN/poly-Ge SBDs where $T_{d-\text{Ge}} = 50\text{--}200 \text{ }^\circ\text{C}$ and $r_1 = 75 \mu\text{m}$. $T_{d-\text{Ge}}$ dependence of (a) I - V characteristics, (b) effective hole barrier height $\Phi_{\text{BP,eff}}$ and ideality factor n .

efficient current injection by embedding a Schottky electrode. After plasma sacrificial oxidation and oxide removal, ZrN (50 nm thick) and TiN cap (15 nm thick) were sequentially deposited using a rf magnetron sputtering system at room temperature. During the deposition, sputtering power density and Ar/N_2 gas flow rate were kept $11 \text{ W}/\text{cm}^2$ and $30/0.1 \text{ sccm}$, respectively. Both ZrN and TiN targets had a stoichiometry composition (a metal/nitrogen ratio of 1:1) and a purity of 99.9%. TiN/ZrN was patterned by the photoresist removal and postmetallization annealing was performed at 350 °C. Two concentric Al (100 nm thick) electrodes were simultaneously prepared as an inner contact on TiN/ZrN and an outer ohmic contact on Ge, using a thermal evaporation system and lift-off photolithography. The distance between inner (ZrN) and outer (ohmic Al) electrodes $d = 10 \mu\text{m}$. Finally, contact annealing was performed at 300 °C, which is lower than the postmetallization annealing temperature; therefore, the effect on the ZrN/poly-Ge contact is considered negligible. Here, we note that SPC-Ge surfaces after CMP and RIE were smooth (root mean square value $\leq 1.3 \text{ nm}$). For comparison, the SBDs were also fabricated on single-crystal p-Ge (100) substrates. The Ge surfaces were not passivated.

III. RESULTS AND DISCUSSION

Table 1 summarizes the thinned SPC-Ge properties. Electron backscatter diffraction and Hall effect measurements with the Van der Pauw method have been used to determine the grain size (GS) and electrical properties. It can be observed that the $T_{d-\text{Ge}} = 125 \text{ }^\circ\text{C}$ sample shows a larger GS, higher μ , and lower p than the other samples. Conversely, the resistivity ρ at $T_{d-\text{Ge}} = 200 \text{ }^\circ\text{C}$ is lower in comparison to the other samples, reflecting the balance between μ and p . More details of $T_{d-\text{Ge}}$ -dependent SPC-Ge are discussed elsewhere in the literature [15].

The current-voltage (I - V) characteristics of ZrN/poly-Ge SBDs exhibit clear rectifying behavior for all $T_{d-\text{Ge}}$ [Fig. 2(a)]. The forward current at $V < 0$ maximizes at $T_{d-\text{Ge}} = 200 \text{ }^\circ\text{C}$. The series resistance of poly-Ge R_{Ge} in the present device structure is expressed using the following equation:

$$R_{\text{Ge}} = \frac{\rho}{2\pi t} \ln\left(\frac{r_2}{r_1}\right), \quad (1)$$

TABLE 1. Properties of poly-Ge.

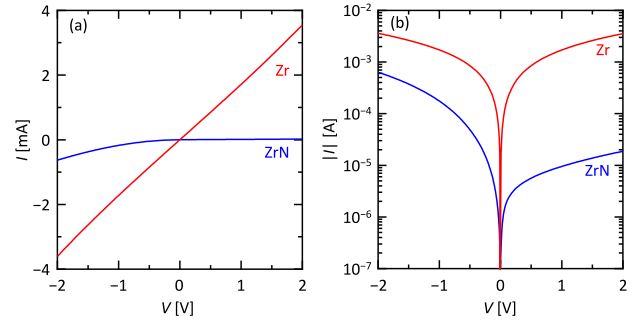
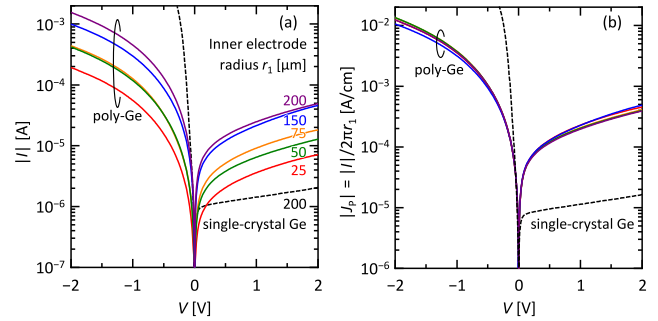
Ge depo. temp. T_{d-Ge} [°C]	GS [μm]	Hall hole mobility μ [cm^2/Vs]	Hole concentration p [cm^{-3}]	Resistivity ρ [$\Omega \text{ cm}$]
50	0.4	40	7.3×10^{17}	2.1×10^{-1}
125	3.7	170	2.2×10^{17}	1.7×10^{-1}
200	0.2	88	9.6×10^{17}	7.4×10^{-2}

where t is the Ge thickness, r_1 is the inner electrode radius (ZrN), and r_2 is the outer electrode radius (ohmic Al). The R_{Ge} is proportional to ρ under the common device dimensions (t , r_1 , and r_2) and limits the forward current of ZrN/poly-Ge SBDs. In contrast, the reverse current at $V > 0$ V is minimized at $T_{d-Ge} = 125$ °C. Reflecting the forward and reverse current, we obtained the best on/off ratio of 30 in ± 2 V bias range at $T_{d-Ge} = 125$ °C. This rectifying behavior suggests that the hole barrier height of ZrN/poly-Ge is naturally high. The effective hole barrier height $\Phi_{BP,eff}$ and the ideality factor n of ZrN/poly-Ge SBDs was estimated from the forward I - V characteristics using following equations:

$$I = I_s \exp\left(\frac{qV}{nkT}\right) \left(1 - \exp\left(-\frac{qV}{kT}\right)\right), \quad (2)$$

$$I_s = A A^* T^2 \exp\left(-\frac{q\Phi_{BP}}{kT}\right) \quad (3)$$

where I_s is the saturation current, q is the elementary charge, k is the Boltzmann constant, T is the absolute temperature, A is the contact area, and A^* is the Richardson constant of $40.8 \text{ A cm}^{-2} \text{ K}^{-2}$ for p-Ge [41]. We estimated $\Phi_{BP,eff}$ and n in the low voltage region (0.01–0.05 V) to avoid the influence of R_{Ge} . $\Phi_{BP,eff}$ and n depend on T_{d-Ge} and $T_{d-Ge} = 125$ °C exhibits the highest performance ($\Phi_{BP,eff} = 0.53$ eV and $n = 2.1$) at $T_{d-Ge} = 125$ °C [Fig. 2(b)]. This high $\Phi_{BP,eff}$ likely reflect higher poly-Ge quality, i.e., larger GS (lower GB density) and fewer defect-induced p . The effective electron barrier height $\Phi_{BN,eff}$ has been calculated as $\Phi_{BN,eff} + \Phi_{BP,eff} = E_g$, where E_g is the energy band gap of Ge (0.66 eV) [14] and is found to be as small as 0.13 eV at $T_{d-Ge} = 125$ °C. The estimated $\Phi_{BP,eff}$ and $\Phi_{BN,eff}$ are comparable to those on the single-crystal Ge substrates [39]. On the other hand, we should consider the dominant current conduction mechanism because the evaluated n s are high (>2). Our former study about Schottky contact on single crystalline Ge with the same carrier density as the present study ($\sim 6 \times 10^{17} \text{ cm}^{-3}$) showed a low n of 1.1 [42]. It means the dominant conduction mechanism is thermionic emission. However, the present study (poly-Ge) shows a high n (2–2.2) even though they have a similar carrier concentration. We think the reason for the large n is grain boundary-related leakage current. For further electrical characterization of poly-Ge, we should estimate Schottky barrier heights from capacitance-voltage (C - V) measurement and compare the I - V results. However, it is difficult in the present structure because of the high series resistance of the

**FIGURE 3.** I - V characteristics of poly-Ge SBDs using Zr and ZrN contacts with (a) linear and (b) logarithm scales in I , where $T_{d-Ge} = 125$ °C and $r_1 = 75$ μm .**FIGURE 4.** Electrode radius dependence of ZrN/poly-Ge SBD properties where $T_{d-Ge} = 125$ °C. (a) I - V characteristics and (b) Peripheral current density J_p .

poly-Ge layer mentioned above. In the next study, we will increase Ge thickness and/or improve the device structure from lateral to vertical one [43] for successful C - V measurement and in detail discussion to clarify the grain boundary properties.

Identically, when we calculate electron or hole barrier heights using (2) and (3), we should carefully consider the effective current flow area, particularly lateral sample structure like this study. We confirmed that the geometrical electrode area can be used for barrier height calculation for our samples. Its details are described in the Appendix section.

To investigate the effect of the contact metal on the rectifying behavior in poly-Ge SBDs, we studied Zr as a non-nitride metal using the same process and structure as for ZrN [Fig. 1]. Figs. 3(a) and 3(b) show that the Zr contact exhibits ohmic behavior, whereas the ZrN contact exhibits rectifying behavior. This suggests a strong FLP at the Zr/poly-Ge interface near the valence band edge, while it is alleviated toward the conduction band side at the ZrN/poly-Ge interface. These results are consistent with a previous study comparing Ti and TiN contacts on a single-crystal Ge substrate and further support the role of N-containing a-IL in alleviating FLP [38]. The higher forward-current in the Zr contacts is possibly because the interfacial reaction in the Zr/Ge structure, i.e., Zr_xGe_y germanide formation [44]

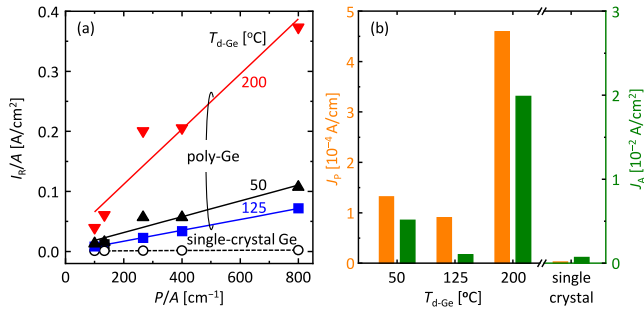


FIGURE 5. (a) Areal current density I_R/A versus electrode perimeter/area ratio P/A obtained from ZrN/poly-Ge and ZrN/single-crystal Ge SBDs with different areas and (b) Areal and peripheral components of current (J_A and J_P), where reverse bias $V_R = 0.3$ V.

and the lateral diffusion of Zr through the GB in Ge [45], provides lower resistance, whereas ZrN is a stable material.

To understand the current behavior in ZrN/poly-Ge SBDs, we prepared the electrodes with different r_1 (25–150 μm) on the same substrate. Fig. 4(a) shows that both forward and reverse currents increase with increasing r_1 . The electrode perimeter $2\pi r_1$ normalizes these currents [Fig. 4(b)]. This phenomenon is discussed separately for the forward and reverse currents. The R_{Ge} given by (1) limits the forward current, as mentioned in Fig. 2(a). Since the distance between inner and outer electrodes is constant in this study ($r_2 - r_1 = d$ (10 μm)) and the t and ρ are constant on the same substrate, (1) is expressed as a function of r_1 substituting $r_2 = r_1 + d$ into (1). Using a Maclaurin expansion up to the primary term, (1) is approximated as

$$R_{Ge} \approx \frac{\rho}{2\pi t} \frac{d}{r_1}. \quad (4)$$

Therefore, we can conclude that the forward current is proportional to r_1 and is normalized by the electrode perimeter $2\pi r_1$. Similarly, in the ZrN/single-crystal p-Ge SBDs, the electrode perimeter normalizes the reverse current, indicating that the surface-state generation current dominates the reverse leakage current [37]. We broke down the total reverse current into its perimeter and area components. The reverse current I_R at a certain reverse bias V_R is generally given by

$$I_R = AJ_A + PJ_P, \quad (5)$$

where A is the contact area, P is the contact perimeter, J_A (A/cm²) and J_P (A/cm) are the areal and peripheral current densities. Thus, J_A and J_P can be estimated from the intercept and slope of the I_R/A - P/A plot shown in Fig. 5(a), respectively. Fig. 5(b) shows that the J_P s for the all T_{d-Ge} s of poly-Ge is significantly higher than that for single-crystal Ge. This relationship is consistent with the reverse J_P shown in Fig. 4(b). These results suggest that the GB-generation current unique to poly-Ge dominates the reverse current in addition to the surface state. Furthermore, both J_P and J_A of $T_{d-Ge} = 50$ and 200 °C are larger than that of $T_{d-Ge} = 125$ °C and bulk-Ge. These likely suggest larger J_P and J_A due to

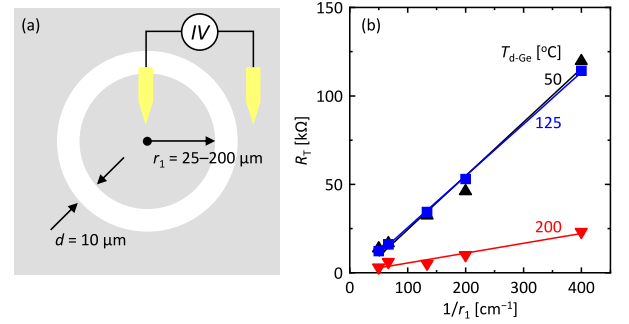


FIGURE 6. (a) Measurement configuration of CTLM structure and (b) R_T/C versus $1/r_1$ plots.

the small GS (high GB density) and the high p (high defect density), respectively. These results are consistent with the GS and p (Table 1).

For a more accurate estimation of Schottky barrier height and a successful application of the Schottky contact with TFTs, the leakage current and n should be reduced. These can be reduced by surface passivation with an insulating layer such as SiO₂/GeO₂ or Y₂O₃ [14], [37] and GS enlargement (GB reduction across the electrode) using Sn incorporation [46], [47], [48] and GeO_x underlayer insertion [16].

IV. CONCLUSION

We first demonstrated a rectifying behavior on poly p-Ge using the FLP-alleviating ZrN contact. This characteristic depends on the poly-Ge quality (GS and defect-induced p). In contrast, the Zr contact exhibits ohmic behavior, suggesting the importance of ZrN in alleviating FLP. In the ZrN/poly-Ge SBDs, R_{Ge} limits the forward current, and the GB-generation current dominates the reverse leakage current. These results will help to understand the physics of FLP in metal/poly-Ge interfaces and expand the range of poly-Ge-based electronic device applications, including n-channel TFTs.

APPENDIX

We used (2) and (3) to estimate the $\Phi_{BP,eff}$ shown in Fig. 2(b) from the forward I - V characteristics. These equations are valid when the current flows through the entire area of the Schottky junction. To clarify the current flow area in the ZrN/poly-Ge junction, we estimated the transfer length L_T , which indicates how long the current spreads from the electrode edge, based on a circular transmission line model (CTLM) [49]. The total resistance R_T of the CTLM structure, shown in Fig. 6(a) used in this study, is expressed as follows:

$$R_T = \frac{R_{sh}}{2\pi r_1} (d + 2L_T)C, \quad (6)$$

$$C = \frac{r_1}{d} \ln\left(1 + \frac{d}{r_1}\right), \quad (7)$$

where R_{sh} is the sheet resistance of Ge and C is the correction factor. R_T/C - d plots are generally used to determine L_T

and R_{sh} with different d and constant r_1 . Conversely, our structure shown in Fig. 6(a) has constant d and different r_1 . Therefore, we draw $R_T/C-1/r_1$ plots. From the slope of these plots shown in Fig. 6(b), we can obtain the L_T using R_{sh} , where R_{sh} is obtained by the 4-probe van der Pauw method. L_T is estimated to be $387 \mu\text{m}$ for $T_{d-Ge} = 50 \text{ }^\circ\text{C}$, $464 \mu\text{m}$ for $T_{d-Ge} = 125 \text{ }^\circ\text{C}$, and $184 \mu\text{m}$ for $T_{d-Ge} = 200 \text{ }^\circ\text{C}$. These values are larger than the electrode radius $r_1 = 75 \mu\text{m}$, indicating that the current flows through almost the whole poly-Ge/ZrN junction area. Therefore, we conclude that the $\Phi_{BP,eff}$ estimated from forward I - V characteristics, shown in Fig. 2(b), is reasonable.

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REFERENCES

- [1] T. Sadoh, H. Kamizuru, A. Kenjo, and M. Miyao, "Low-temperature formation ($500 \text{ }^\circ\text{C}$) of poly-Ge thin-film transistor with NiGe Schottky source/drain," *Appl. Phys. Lett.*, vol. 89, no. 19, Nov. 2006, Art. no. 192114, doi: [10.1063/1.2387136](https://doi.org/10.1063/1.2387136).
- [2] K. Toko, I. Nakao, T. Sadoh, T. Noguchi, and M. Miyao, "Electrical properties of poly-Ge on glass substrate grown by two-step solid-phase crystallization," *Solid State Electron.*, vol. 53, no. 11, pp. 1159–1164, Nov. 2009, doi: [10.1016/j.sse.2009.08.002](https://doi.org/10.1016/j.sse.2009.08.002).
- [3] Y. Kamata et al., "Superior cut-off characteristics of $L_g=40\text{nm}$ $W_{fin}=7\text{nm}$ poly Ge junctionless Tri-gate FET for stacked 3D circuits integration," in *Proc. Symp. VLSI Technol.*, Aug. 2013, pp. T94–T95.
- [4] S. Kabuyanagi, T. Nishimura, K. Nagashio, and A. Toriumi, "Impacts of oxygen passivation on poly-crystalline germanium thin film transistor," *Thin Solid Films*, vol. 557, pp. 334–337, Apr. 2014, doi: [10.1016/j.tsf.2013.11.133](https://doi.org/10.1016/j.tsf.2013.11.133).
- [5] A. Hara, Y. Nishimura, and H. Ohsawa, "Self-aligned metal double-gate junctionless p-channel low-temperature polycrystalline-germanium thin-film transistor with thin germanium film on glass substrate," *Jpn. J. Appl. Phys.*, vol. 56, no. 3S, Dec. 2016, Art. no. 3BB01, doi: [10.7567/JJAP.56.03BB01](https://doi.org/10.7567/JJAP.56.03BB01).
- [6] W.-H. Huang et al., "Enabling n-type polycrystalline Ge junctionless FinFET of low thermal budget by in situ doping of channel and visible pulsed laser annealing," *Appl. Phys. Exp.*, vol. 10, no. 2, Jan. 2017, Art. no. 26502, doi: [10.7567/APEX.10.026502](https://doi.org/10.7567/APEX.10.026502).
- [7] B. Hekmatshoar, S. Mohajerzadeh, D. Shahrjerdi, and M. D. Robertson, "Thin-film tunneling transistors on flexible plastic substrates based on stress-assisted lateral growth of polycrystalline germanium," *Appl. Phys. Lett.*, vol. 85, no. 6, pp. 1054–1056, Aug. 2004, doi: [10.1063/1.1779946](https://doi.org/10.1063/1.1779946).
- [8] K. Toko, R. Numata, N. Oya, N. Fukata, N. Usami, and T. Suemasu, "Low-temperature ($180 \text{ }^\circ\text{C}$) formation of large-grained Ge (111) thin film on insulator using accelerated metal-induced crystallization," *Appl. Phys. Lett.*, vol. 104, no. 2, Jan. 2014, Art. no. 22106, doi: [10.1063/1.4861890](https://doi.org/10.1063/1.4861890).
- [9] T. Suzuki, B. M. Joseph, M. Fukai, M. Kamiko, and K. Kyuno, "Low-temperature ($330 \text{ }^\circ\text{C}$) crystallization and dopant activation of Ge thin films via AgSb-induced layer exchange: Operation of an n-channel polycrystalline Ge thin-film transistor," *Appl. Phys. Exp.*, vol. 10, no. 9, Aug. 2017, Art. no. 95502, doi: [10.7567/APEX.10.095502](https://doi.org/10.7567/APEX.10.095502).
- [10] H. Higashi et al., "Electrical properties of pseudo-single-crystalline Ge films grown by Au-induced layer exchange crystallization at $250 \text{ }^\circ\text{C}$," *J. Appl. Phys.*, vol. 123, no. 21, Jun. 2018, Art. no. 215704, doi: [10.1063/1.5031469](https://doi.org/10.1063/1.5031469).
- [11] A. Nayfeh, C. O. Chui, T. Yonehara, and K. C. Saraswat, "Fabrication of high-quality p-MOSFET in Ge grown heteroepitaxially on Si," *IEEE Electron Device Lett.*, vol. 26, no. 5, pp. 311–313, May 2005, doi: [10.1109/LED.2005.846578](https://doi.org/10.1109/LED.2005.846578).
- [12] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," *Nature*, vol. 479, no. 7373, pp. 324–328, Nov. 2011, doi: [10.1038/nature10678](https://doi.org/10.1038/nature10678).
- [13] S. Takagi et al., "III-V/Ge channel MOS device technologies in nano CMOS era," *Jpn. J. Appl. Phys.*, vol. 54, no. 6S1, Jun. 2015, Art. no. 6FA01, doi: [10.7567/JJAP.54.06FA01](https://doi.org/10.7567/JJAP.54.06FA01).
- [14] A. Toriumi and T. Nishimura, "Germanium CMOS potential from material and process perspectives: Be more positive about germanium," *Jpn. J. Appl. Phys.*, vol. 57, no. 1, Jan. 2018, Art. no. 10101, doi: [10.7567/JJAP.57.010101](https://doi.org/10.7567/JJAP.57.010101).
- [15] K. Toko, R. Yoshimine, K. Moto, and T. Suemasu, "High-hole mobility polycrystalline Ge on an insulator formed by controlling precursor atomic density for solid-phase crystallization," *Sci. Rep.*, vol. 7, no. 1, pp. 1–7, Dec. 2017, doi: [10.1038/s41598-017-17273-6](https://doi.org/10.1038/s41598-017-17273-6).
- [16] T. Imajo, T. Ishiyama, N. Saitoh, N. Yoshizawa, T. Suemasu, and K. Toko, "Record-high hole mobility germanium on flexible plastic with controlled interfacial reaction," *ACS Appl. Electron. Mater.*, vol. 4, no. 1, pp. 269–275, Jan. 2022, doi: [10.1021/acsaelm.1c00997](https://doi.org/10.1021/acsaelm.1c00997).
- [17] D. Takahara, K. Moto, T. Imajo, T. Suemasu, and K. Toko, "Sb-doped crystallization of densified precursor for n-type polycrystalline Ge on an insulator with high carrier mobility," *Appl. Phys. Lett.*, vol. 114, no. 8, pp. 1–5, Feb. 2019, doi: [10.1063/1.5084191](https://doi.org/10.1063/1.5084191).
- [18] M. Saito, K. Moto, T. Nishida, T. Suemasu, and K. Toko, "High-electron-mobility ($370 \text{ cm}^2/\text{Vs}$) polycrystalline Ge on an insulator formed by As-doped solid-phase crystallization," *Sci. Rep.*, vol. 9, no. 1, Dec. 2019, Art. no. 16558, doi: [10.1038/s41598-019-53084-7](https://doi.org/10.1038/s41598-019-53084-7).
- [19] K. Moto, K. Yamamoto, T. Imajo, T. Suemasu, H. Nakashima, and K. Toko, "Polycrystalline thin-film transistors fabricated on high-mobility solid-phase-crystallized Ge on glass," *Appl. Phys. Lett.*, vol. 114, no. 21, pp. 1–4, May 2019, doi: [10.1063/1.5093952](https://doi.org/10.1063/1.5093952).
- [20] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Appl. Phys. Lett.*, vol. 89, no. 25, pp. 1–3, Dec. 2006, doi: [10.1063/1.2410241](https://doi.org/10.1063/1.2410241).
- [21] T. Nishimura, K. Kita, and A. Toriumi, "Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface," *Appl. Phys. Lett.*, vol. 91, no. 12, pp. 1–3, Sep. 2007, doi: [10.1063/1.2789701](https://doi.org/10.1063/1.2789701).
- [22] R. R. Lieten, S. Degroote, M. Kuijk, and G. Borghs, "Ohmic contact formation on n-type Ge," *Appl. Phys. Lett.*, vol. 92, no. 2, pp. 1–3, Jan. 2008, doi: [10.1063/1.2831918](https://doi.org/10.1063/1.2831918).
- [23] Y. Zhou et al., "Investigating the origin of Fermi level pinning in Ge Schottky junctions using epitaxially grown ultrathin MgO films," *Appl. Phys. Lett.*, vol. 96, no. 10, Mar. 2010, Art. no. 102103, doi: [10.1063/1.3357423](https://doi.org/10.1063/1.3357423).
- [24] J.-Y. J. Lin, A. M. Roy, A. Nainani, Y. Sun, and K. C. Saraswat, "Increase in current density for metal contacts to n-germanium by inserting TiO_2 interfacial layer to reduce Schottky barrier height," *Appl. Phys. Lett.*, vol. 98, no. 9, Feb. 2011, Art. no. 92113, doi: [10.1063/1.3562305](https://doi.org/10.1063/1.3562305).
- [25] B.-Y. Tsui and M.-H. Kao, "Mechanism of Schottky barrier height modulation by thin dielectric insertion on n-type germanium," *Appl. Phys. Lett.*, vol. 103, no. 3, Jul. 2013, Art. no. 32104, doi: [10.1063/1.4813834](https://doi.org/10.1063/1.4813834).
- [26] S. Gupta, P. P. Manik, R. K. Mishra, A. Nainani, M. C. Abraham, and S. Lodha, "Contact resistivity reduction through interfacial layer doping in metal-interfacial layer-semiconductor contacts," *J. Appl. Phys.*, vol. 113, no. 23, Jun. 2013, Art. no. 234505, doi: [10.1063/1.4811340](https://doi.org/10.1063/1.4811340).
- [27] H. Liu et al., "Ohmic contact formation of metal/amorphous-Ge/n-Ge junctions with an anomalous modulation of Schottky barrier height," *Appl. Phys. Lett.*, vol. 105, no. 19, Nov. 2014, Art. no. 192103, doi: [10.1063/1.4901421](https://doi.org/10.1063/1.4901421).
- [28] G.-S. Kim et al., "Effective Schottky barrier height lowering of metal/n-Ge with a $\text{TiO}_2/\text{GeO}_2$ interlayer stack," *ACS Appl. Mater. Interfaces*, vol. 8, no. 51, pp. 35419–35425, Dec. 2016, doi: [10.1021/acsaami.6b10947](https://doi.org/10.1021/acsaami.6b10947).
- [29] A. Suzuki, O. Nakatsuka, M. Sakashita, and S. Zaima, "Alleviation of Fermi level pinning at metal/n-Ge interface with lattice-matched $\text{Si}_x\text{Ge}_{1-x-y}\text{Sn}_y$ ternary alloy interlayer on Ge," *Jpn. J. Appl. Phys.*, vol. 57, no. 6, May 2018, Art. no. 60304, doi: [10.7567/JJAP.57.060304](https://doi.org/10.7567/JJAP.57.060304).
- [30] J.-R. Wu, Y.-H. Wu, C.-Y. Hou, M.-L. Wu, C.-C. Lin, and L.-L. Chen, "Impact of fluorine treatment on Fermi level depinning for metal/germanium Schottky junctions," *Appl. Phys. Lett.*, vol. 99, no. 25, Dec. 2011, Art. no. 253504, doi: [10.1063/1.3666779](https://doi.org/10.1063/1.3666779).

- [31] G.-S. Kim et al., "Surface passivation of germanium using SF₆ plasma to reduce source/drain contact resistance in germanium n-FET," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 745–747, Aug. 2015, doi: [10.1109/LED.2015.2440434](https://doi.org/10.1109/LED.2015.2440434).
- [32] K. Kasahara, S. Yamada, K. Sawano, M. Miyao, and K. Hamaya, "Mechanism of Fermi level pinning at metal/germanium interfaces," *Phys. Rev. B, Condens. Matter*, vol. 84, no. 20, Nov. 2011, Art. no. 205301, doi: [10.1103/PhysRevB.84.205301](https://doi.org/10.1103/PhysRevB.84.205301).
- [33] Y. Deng, O. Nakatsuka, J. Yokoi, N. Taoka, and S. Zaima, "Epitaxial formation and electrical properties of Ni germanide/Ge(110) contacts," *Thin Solid Films*, vol. 557, pp. 84–89, Apr. 2014, doi: [10.1016/j.tsf.2013.10.017](https://doi.org/10.1016/j.tsf.2013.10.017).
- [34] T. Nishimura, T. Yajima, and A. Toriumi, "Reexamination of Fermi level pinning for controlling Schottky barrier height at metal/Ge interface," *Appl. Phys. Exp.*, vol. 9, no. 8, Aug. 2016, Art. no. 81201, doi: [10.7567/APEX.9.081201](https://doi.org/10.7567/APEX.9.081201).
- [35] T. Nishimura, X. Luo, S. Matsumoto, T. Yajima, and A. Toriumi, "Almost pinning-free bismuth/Ge and /Si interfaces," *AIP Adv.*, vol. 9, no. 9, 2019, Art. no. 95013, doi: [10.1063/1.5115535](https://doi.org/10.1063/1.5115535).
- [36] M. Iyota, K. Yamamoto, D. Wang, H. Yang, and H. Nakashima, "Ohmic contact formation on n-type Ge by direct deposition of TiN," *Appl. Phys. Lett.*, vol. 98, no. 19, May 2011, Art. no. 192108, doi: [10.1063/1.3590711](https://doi.org/10.1063/1.3590711).
- [37] K. Yamamoto, K. Harada, H. Yang, D. Wang, and H. Nakashima, "Fabrication of TiN/Ge contact with extremely low electron barrier height," *Jpn. J. Appl. Phys.*, vol. 51, no. 7R, Jun. 2012, Art. no. 70208, doi: [10.1143/JJAP.51.070208](https://doi.org/10.1143/JJAP.51.070208).
- [38] K. Yamamoto et al., "Role of an interlayer at a TiN/Ge contact to alleviate the intrinsic Fermi-level pinning position toward the conduction band edge," *Appl. Phys. Lett.*, vol. 104, no. 13, Mar. 2014, Art. no. 132109, doi: [10.1063/1.4870510](https://doi.org/10.1063/1.4870510).
- [39] K. Yamamoto et al., "Electrical and structural properties of group-4 transition-metal nitride (TiN, ZrN, and HfN) contacts on Ge," *J. Appl. Phys.*, vol. 118, no. 11, Sep. 2015, Art. no. 115701, doi: [10.1063/1.4930573](https://doi.org/10.1063/1.4930573).
- [40] K. Yamamoto et al., "Wide range control of Schottky barrier heights at metal/Ge interfaces with nitrogen-contained amorphous interlayers formed during ZrN sputter deposition," *Semicond. Sci. Technol.*, vol. 33, no. 11, Oct. 2018, Art. no. 114011, doi: [10.1088/1361-6641/aae4bd](https://doi.org/10.1088/1361-6641/aae4bd).
- [41] S. M. Sze, *Physics of Semiconductor Devices*. 2nd ed. New York, NY, USA: Wiley, 1981, p. 257.
- [42] T. Maekura et al., "Effect of n-type doping level on direct band gap electroluminescence intensity for asymmetric metal/Ge/metal diodes," *Semicond. Sci. Technol.*, vol. 32, no. 10, Aug. 2017, Art. no. 104001, doi: [10.1088/1361-6641/aa827f](https://doi.org/10.1088/1361-6641/aa827f).
- [43] H. Schaber, D. Cutter, and W. M. Werner, "Laser annealing study of the grain size effect in polycrystalline silicon Schottky diodes," *J. Appl. Phys.*, vol. 53, no. 12, pp. 8827–8834, Dec. 1982, doi: [10.1063/1.330434](https://doi.org/10.1063/1.330434).
- [44] S. Gaudet, C. Detavernier, A. J. Kellock, P. Desjardins, and C. Lavoie, "Thin film reaction of transition metals with germanium," *J. Vac. Sci. Technol. A*, vol. 24, no. 3, pp. 474–485, May 2006, doi: [10.1116/1.2191861](https://doi.org/10.1116/1.2191861).
- [45] P. H. Holloway, "Grain boundary diffusion of phosphorus in polycrystalline silicon," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron.*, vol. 21, no. 1, pp. 19–22, May 1982, doi: [10.1116/1.571713](https://doi.org/10.1116/1.571713).
- [46] T. Sadoh, Y. Kai, R. Matsumura, K. Moto, and M. Miyao, "High carrier mobility of Sn-doped polycrystalline-Ge films on insulators by thickness-dependent low-temperature solid-phase crystallization," *Appl. Phys. Lett.*, vol. 109, no. 23, Dec. 2016, Art. no. 232106, doi: [10.1063/1.4971825](https://doi.org/10.1063/1.4971825).
- [47] K. Moto, R. Yoshimine, T. Suemasu, and K. Toko, "Improving carrier mobility of polycrystalline Ge by Sn doping," *Sci. Rep.*, vol. 8, no. 1, Oct. 2018, Art. no. 14832, doi: [10.1038/s41598-018-33161-z](https://doi.org/10.1038/s41598-018-33161-z).
- [48] K. Moto, N. Saitoh, N. Yoshizawa, T. Suemasu, and K. Toko, "Solid-phase crystallization of densified amorphous GeSn leading to high hole mobility (540 cm²/V s)," *Appl. Phys. Lett.*, vol. 114, no. 11, Mar. 2019, Art. no. 112110, doi: [10.1063/1.5088847](https://doi.org/10.1063/1.5088847).
- [49] D. Schroeder, *Semiconductor Material and Device Characterization*, 3rd ed. New York, NY, USA: Wiley, 1998, p. 144.