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Compact Modeling of Parasitic Capacitances in GAAFETs for Advanced Technology Nodes

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ABSTRACT In this work, a compact model for parasitic capacitances is proposed for Gate-All-Around silicon nanosheet FET (GAAFET). For 3 stack GAAFET, all possible parasitic capacitance components are included according to the electric field lines and geometric structure of this device. Conformal mapping and Schwarz Christoffel transforms as well as elliptic integral methods are used to model the perpendicular capacitance as well as coplanar plate capacitance. We have also used fundamental capacitance modeling to calculate the corner capacitance. The validity of the proposed model is calibrated and verified with the 3D TCAD simulations. Evaluation is also done of how different device physical parameters affect the total parasitic capacitance. The results demonstrate that the proposed model is capable of accurately estimating the parasitic capacitance of the GAAFET device. The proposed model is also implemented in the BSIM-CMG framework to verify the model's accuracy and application of it in the circuit simulation.

INDEX TERMS GAAFET, parasitic capacitance, conformal mapping, BSIM-CMG.

I. INTRODUCTION

Due to the scaling of transistors, numerous benefits including high density, high speed, and low power consumption have already been reported [1], [2], [3], [4], [5], [6], [7], [8], [9]. Gate-All-Around Nanosheet Field Effect Transistors (GAAFETs) have recently emerged as the device of choice for upcoming technology nodes due to their better gate control capability [10], [11], [12], [13], [14], [15], [16], [17].

On the other hand, parasitic capacitance has emerged as a significant performance-limiting factor in modern devices, particularly at high frequency. The parasitic capacitance may deteriorate the *RC* delay and provide an adverse impact to device operation [19], [20]. The contribution of the parasitic capacitance in the total capacitance of the device is quite significant, which is why it has non-negligible impact on the device as well as IC design and we can not disregard it [21], [22]. Hence, it is crucial to analyze and optimize the parasitic component of capacitance. An accurate compact model to quantify these capacitance values is of significant importance. A few models have been reported already. Dong et al. [23] developed an analytical model for parasitic gate capacitance for the gate-all-around (GAA) silicon nanowire MOSFET (SNWT), where top and bottom gates are asymmetrical. Zou et al. [22] developed a parasitic gate capacitance analytical model for gate-all-around cylindrical silicon nanowire MOSFETs (SNWTs) by equivalent transformation and inversion of Schwarz-Christoffel mapping with various device parameters. An and Kim [24] came up with an analytical model for fringe gate capacitance in gate-all-around cylindrical silicon nanowire MOSFETs (SNWTs) using conformal mapping, integral, and non-dimensionalization. However, none of them addressed realistic stacked FETs including corner rounding. The enhanced strategy presented by Kim et al. [20] employed a fringe capacitance model for nanoplate FET considering circular channel using conformal mapping. Nevertheless, the capacitance when the two capacitor plates are in the same plane is not captured by the model. Furthermore, they made no mention of the accuracy of their model in comparison to the industry standard BSIM-CMG model. Recently

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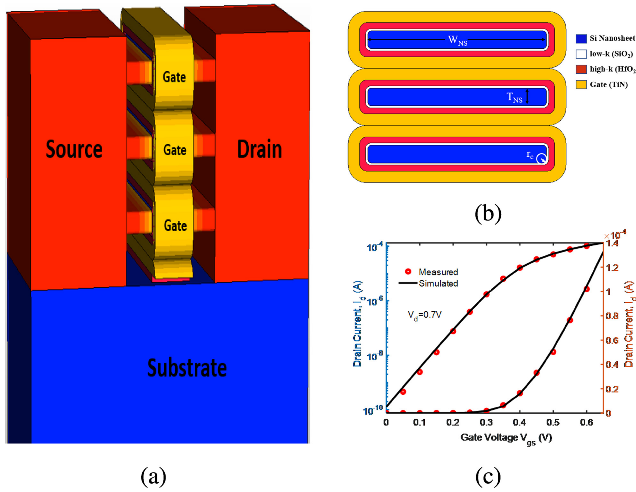

FIGURE 1. (a) 3D Schematic of GAAFET structure, (b) 2D cross-section of 3 nanosheet structure, and (c) Calibrated I_d-V_g with experimental data [18].

Suk et al. [25] and Sharma et al. [26] have presented updated models for parasitic capacitances in GAAFETs. However, both of these works do not include a physical model to account for the corner rounding and related capacitance components. Sharma et al. [26] captures it implicitly through other components which results in a loss of accuracy. Both the models are slightly shy of the accuracy usually required from industry (error $< 1\%$).

In this work, an accurate analytical parasitic capacitance model is proposed using the conformal mapping as well as Schwarz Christoffel transform [21], [28], [29], [32]. The proposed model is then verified with the 3D TCAD simulation, and the effect of important device parameters on the parasitic capacitance is investigated as well. Additionally, the suggested analytical model is implemented in the BSIM-CMG framework and validated through circuit simulation.

The rest of the paper is arranged as follows: Section II describes the device structure and simulation setup, Section III explains the parasitic capacitance modeling, and Section IV discusses the results and discussions followed by the conclusion in Section V.

II. DEVICE STRUCTURE AND SIMULATION SETUP

Fig. 1 (a) shows the 3D schematic of GAAFET created using the TCAD simulation tool, and the 2D cross-sectional view of the three stacked nanosheets is delineated in Fig. 1(b). The GAAFET structure is taken into consideration that has source/drain extension regions between a lightly doped channel and a strongly doped source/drain. The corner radius of the nanosheet is denoted by r_c. The length of the gate, source, and drain are L_g, L_s, and L_d. The equivalent oxide thickness (EOT) is 0.9nm, where thickness of SiO_2 and HfO_2 are 0.6nm and 1.7nm respectively. The physical device parameters that have been used for the simulation are shown in Table 1. The I_d-V_g of the simulated structure has been calibrated with experimental data [18], as shown in Fig. 1(c).

TABLE 1. Geometric device parameters of 3 stack nanosheet GAAFET.

Parameters	Description	Value
L_g	Gate Length	12 nm
W_g	Gate width	61 nm
H_g	Gate height	Vary with T_s and t_m
W_s	Width of the nanosheet	10 to 50 nm
T_s	Thickness of the nanosheet	2 to 5 nm
r_c	Corner rounding radius	0 to $T_s/2$ nm
L_{sd}	Source or drain length	30 nm
W_{sd}	Source or drain width	10 to 50 nm
H_{sd}	Source or drain height	Vary with T_s
EOT	Effective oxide thickness	0.9 nm
T_{ox}	Gate oxide thickness	2.3 nm
T_{sp}	Inner spacer thickness	8 to 20 nm
ε_{sp}	Inner spacer k-value	3 to 10
t_m	Metal thickness	2.7 to 5.2 nm
T_{gs}	Gate stack	Vary with T_{ox} and t_m
NNS_{sep}	Separation between nanosheets	2.5 to 5.5 nm
NNS	Number of nanosheet	3

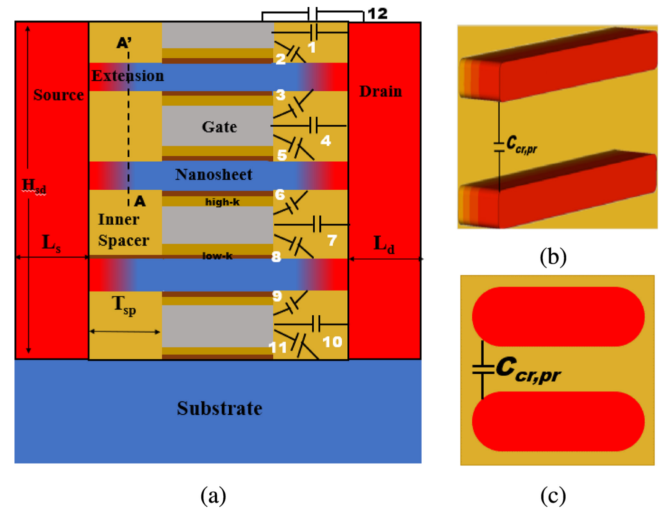

FIGURE 2. (a) 2D cross sectional view with parasitic capacitance components of 3 nanosheet GAFET structure, (b) Corner capacitance in the extrinsic part of nanosheet in 3D view, and (c) Cross section along the cut line *AA′* for extrinsic nanosheet corner capacitance.

III. PARASITIC CAPACITANCE MODELING

In order to calculate the capacitance of complex GAAFET structure, we separate the intricate structure into several sections according to the field lines observed from 3D TCAD simulations and assign numbers to them as shown in Fig. 2 (a). Along with this, corner capacitance has also been included, as depicted in Fig. 2(b) and (c). As shown in Fig. 2, the parasitic capacitances of the GAAFETs can be divided into gate-to-S/D extension capacitance (C_{gsdex}), gate-to-bulk capacitance (c_{gsb}), gate-to S/D electrode capacitance (C_{gsdo}), and corner capacitance of the extrinsic part of the nanosheet ($C_{cr,pr}$) [Fig. 2(b) and (c)]. According to Fig. 2, for three nanosheet GAAFETs, the extension capacitances (C_{gsdex}) are 2, 3, 5, 6, 8, and 9, where all are perpendicular capacitances. Additionally, according to structure and field lines, gate to bulk capacitance (C_{gsb}) also exists and denoted with 11, which is also perpendicular capacitance. There are two kinds of C_{gsdo}, one is parallel plate capacitance ($C_{gsdo,pr}$) denoted with 1, 4, 7, 10 and

TABLE 2. Different components of parasitic capacitance.

Types	Perpendicular	Parallel	Coplanar	Corner
C_{gsdex}	C_2,C_3, C_5 C_6, C_8, C_9			
C_{gsb}	C_{11}			
C_{gsdo}		C_1, C_4, C_7, C_{10},	C_{12}	
C_{cr}				$(N_{GAA}-1)$

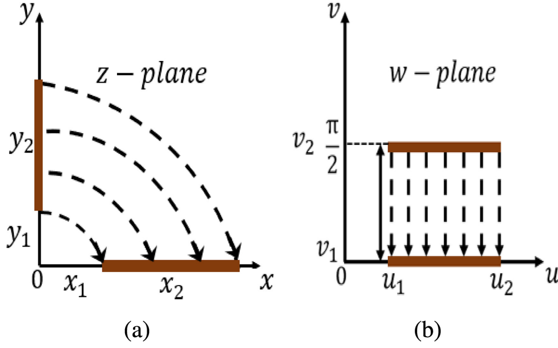

FIGURE 3. (a) Perpendicular plate capacitor in *z*-plane, and (b) transformed parallel capacitor using conformal mapping in *w*-plane.

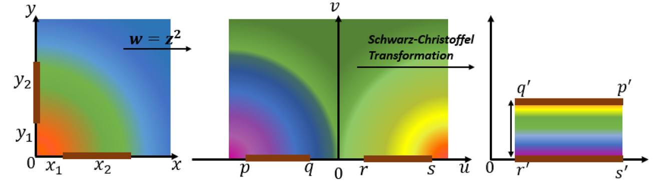

FIGURE 4. Transformation of perpendicular plate to parallel plate using conformal mapping and Schwarz-Christoffel techniques.

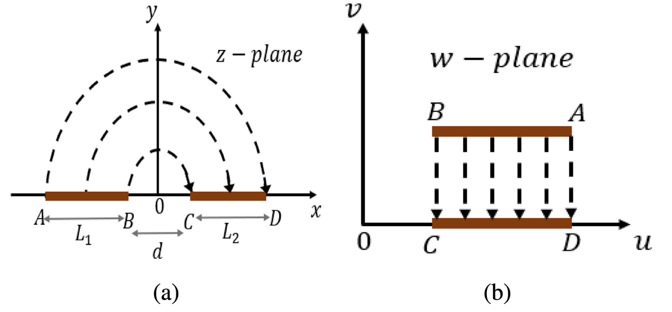

FIGURE 5. (a) Coplanar plate capacitor in *z*-plane, and (b) transformed parallel capacitor using conformal mapping in *w*-plane.

another is gate-to-S/D electrode top coplanar plate capacitance ($C_{gsdo,cop}$) denoted with 12. All capacitances are shown in Table 2. The total parasitic capacitance of GAAFET can be written as

$$\begin{aligned} C_pS/D &= C_{gsdex} + C_{gsb} + C_{gsdo} + (N_{GAA}-1)C_{cr,pr} \\ &= C_{gsdex,pp2} + C_{gsdex,pp3} + C_{gsdex,pp5} \\ &\quad + C_{gsdex,pp6} + C_{gsdex,pp8} + C_{gsdex,pp9} \\ &\quad + C_{gsb,pp11} + C_{gsdo,pr1} + C_{gsdo,pr4} + C_{gsdo,pr7} \\ &\quad + C_{gsdo,pr10} + C_{gsdo,cop12} + (N_{GAA}-1)C_{cr,pr} \end{aligned} \tag{1}$$

where N_{GAA} is the number of sheets.

To determine the above-mentioned perpendicular and coplanar plate capacitance, conformal mapping and Schwarz Christoffel transforms are used. The corner capacitance is calculated using the fundamental capacitance modeling of two circular plates. Along with this, parallel plate capacitances of different parts are calculated using a basic parallel plate equation. In Section III-A, the fundamental models of capacitance for perpendicular, coplanar, and corner plates are determined. Each capacitance component according to the device structure in Fig. 2 is discussed in Section III-B.

A. BASIC CAPACITANCE MODEL

(1) Perpendicular Plate Capacitance: Fig. 3(a) shows the perpendicular plate capacitor, where the electric field lines are illustrated by the outermost edges of concentric ellipses. Bansal et al. [27] introduced that a collection of confocal ellipses can be used to model the electric field lines.

Using conformal mapping and Schwarz-Christoffel theorem to map perpendicular plate to parallel plate [Figs. 3 and 4], which is determined by [29], [30], [31] with relative error of 3×10^{-6} and considering the width of the capacitor plate, we can write

$$\begin{aligned} C_{pp} &= \epsilon \frac{W}{\pi} \ln\left[2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right], \; for, \; \frac{1}{\sqrt{2}} < k < 1 \\ &= \epsilon \frac{\pi W}{\ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]'}, \; for, \; 0 < k < \frac{1}{\sqrt{2}} \end{aligned} \tag{2}$$

The detailed methodology is described in the Appendix.

(2) Coplanar Plate Capacitance: Capacitance between the coplanar plane is also modeled using the conformal mapping technique. Fig. 5(a) shows the coplanar plate in the z-plane and 5(b) shows the equivalent parallel plate capacitor in w-plane [28]. The coplanar plate is also transformed into parallel plate using the coordinate transformation technique [30] and it can be written as

$$C_{cop} = \epsilon \frac{1}{\pi} W \ln\left(1 + \frac{2L}{d}\right) \tag{3}$$

After taking ζ to account for plate area mismatch [22], the equation (3) can be written as

$$C_{cop} = \epsilon \frac{1}{\pi} W_1 \sqrt{\frac{W_2 L_2}{W_1 L_1}} \ln\left(1 + \frac{2L_1}{d}\right) \tag{4}$$

where,

$$\zeta = \sqrt{\frac{\int dS_2}{\int dS_1}} = \sqrt{\frac{W_2 L_2}{W_1 L_1}} \tag{5}$$

(3) Corner Radius Capacitance: Fig. 6 shows the corner rounding plates, which is considered as one fourth of the circle. The capacitance between two plates is estimated using the fundamental capacitance modeling of two circular plates.

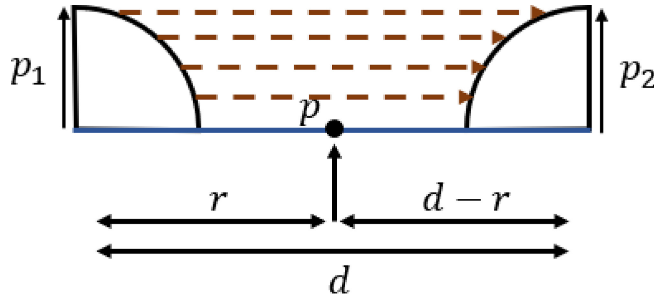

FIGURE 6. Corner rounding plates of nanosheet GAAFET.

TABLE 3. Device parameters for GAAFET perpendicular parasitic capacitance.

Capacitance	x_1	x_2	y_1	y_2	W	ϵ_{sp}
$C_{gsdex,pp3}$	0	T_{sp}	T_{ox}	H_g	P	ϵ_{sp}
$C_{gsdex,pp2}$	0	T_{sp}	T_{ox}	$H_g + h_{top}$	P	ϵ_{sp}
$C_{gsb,pp11}$	0	T_{sp}	T_{ox}	$T_{ox} + T_{FR}$	P	ϵ_{sp}

Taking into account one-fourth of the circle, the surface area of the plate can be written as

$$A_{crp} = \frac{2\pi r}{4} = \frac{\pi r l}{2} \tag{6}$$

where r is the radius of the circle and l is the length.

The potential difference between two plates as

$$\Delta V = \frac{2Q}{\epsilon_0 \pi l} \ln\left[\frac{(d-p_1)(d-p_2)}{p_1 p_2}\right] \tag{7}$$

The capacitance per unit length can be expressed as

$$c = \alpha k \frac{1}{\ln\left[\frac{(d-r)^2}{r^2}\right]} \tag{8}$$

where,

$$k = \frac{\epsilon_0 \pi}{2} \tag{9}$$

$$p_1 = p_2 = r \tag{10}$$

A fitting parameter α is introduced as the plate is not perfectly circular. The value of α is extracted to be 0.42 for the device geometry considered.

B. INDIVIDUAL CAPACITANCE COMPONENT MODELING

(1) Perpendicular Capacitance, $C_{gsdex,pp3}$: It is one of the middle-located gate-to-source/drain extension perpendicular plate capacitances according to Fig. 2. The $C_{gsdex,pp3}$ can be modeled using equation (2) and the corresponding physical parameters are listed in Table 3. Where T_{ox} is the gate oxide thickness, H_g is the gate height. T_{sp} is the spacer thickness, ϵ_{sp} is the dielectric constant of the spacer, and P is the integral perimeter [30]. P can be written as follows

$$P = N_{GAA} \times (\pi T_s + 2(W_s - T_s)) \tag{11}$$

where N_{GAA} is the number of nanosheets. W_s and T_s are the width and thickness of the nanosheet respectively. We can model $C_{gsdex,pp5}$, $C_{gsdex,pp6}$, $C_{gsdex,pp8}$, and $C_{gsdex,pp9}$ using the same device parameters.

TABLE 4. Device parameters for GAAFET coplanar plate parasitic capacitance.

Capacitance	W_1	L_1	W_2	L_2	d	ϵ
$C_{gsdo,cop12}$	W_g	$L_g/2$	W_{sd}	L_{sd}	T_{sp}	ϵ_{top}

(2) Perpendicular Capacitance, $C_{gsdex,pp2}$: $C_{gsdex,pp2}$ is the top gate-to-source/drain extension perpendicular plate capacitance as mentioned in Fig. 2. $C_{gsdex,pp2}$ is likewise modeled by using the device parameters claimed in Table 3 in equation (2), where, h_{top} is the top height of gate.

(3) Perpendicular Capacitance, $C_{gsb,pp11}$: $C_{gsb,pp11}$ is the lower parasitic FinFET perpendicular plate capacitance. As the bottom part of the device is formed as a parasitic FinFET, so the physical parameters for this component are different from others, as mentioned in Table 3. $C_{gsb,pp11}$ has also been computed using equation (2), where T_{FR} is the fringe thickness.

(4) Coplanar Plate Capacitance, $C_{gsdo,cop12}$: $C_{gsdo,cop12}$ is the coplanar plate capacitance between the gate and the source/drain electrode top side. It is modeled using equation (4) and the corresponding physical parameters are listed in Table 4. ϵ_{top} is the dielectric constant of the top layer, where, W_g and L_g are the width and the length of the gate, respectively. W_{sd} and L_{sd} are the width and the length of the S/D electrode, respectively.

(5) Corner Capacitance, $C_{cr,pr}$: $C_{cr,pr}$ is the corner capacitance between corner rounding of the extrinsic part of two nanosheet plates. It has been considered between two surrounded exterior nanosheet plates for this work, as illustrated in Fig. 2(b) and (c). Equation (8) is used to model corner capacitance. Where r_c is the corner radius of the plate and d is the distance between the centers of a circle.

(6) Parallel Plate Capacitance, $C_{gsdo,pr4}$: $C_{gsdo,pr4}$ is the parallel plate capacitance between gate-to-S/D electrode. We can model it using a simple parallel plate capacitance equation. Equation (5) has been used to compensate for the plate area mismatch. Additionally to model this, source or drain extension has not been considered. After considering all of the things, the model can be approximated as

$$C_{gsdo,pr4} = \lambda \frac{\epsilon_{sp}\sqrt{A_{sd}A_{fgsd}}}{T_{sp}} \tag{12}$$

where A_{sd} is the source or drain electrode area and A_{fgsd} is the effective facing area between the gate and S/D electrode [32], and λ is an empirical fitting parameter that will be decided by the numerical simulation and depends on the particular instances. Throughout this work, the value of λ is assumed to be 0.5 following the numerical verification.

We can further write considering corner radius of nanosheet,

$$A_{sd} = H_{sd}W_{sd} - N_{GAA}\left(W_s T_s - 4r_c^2 + \pi r_c^2\right) \tag{13}$$

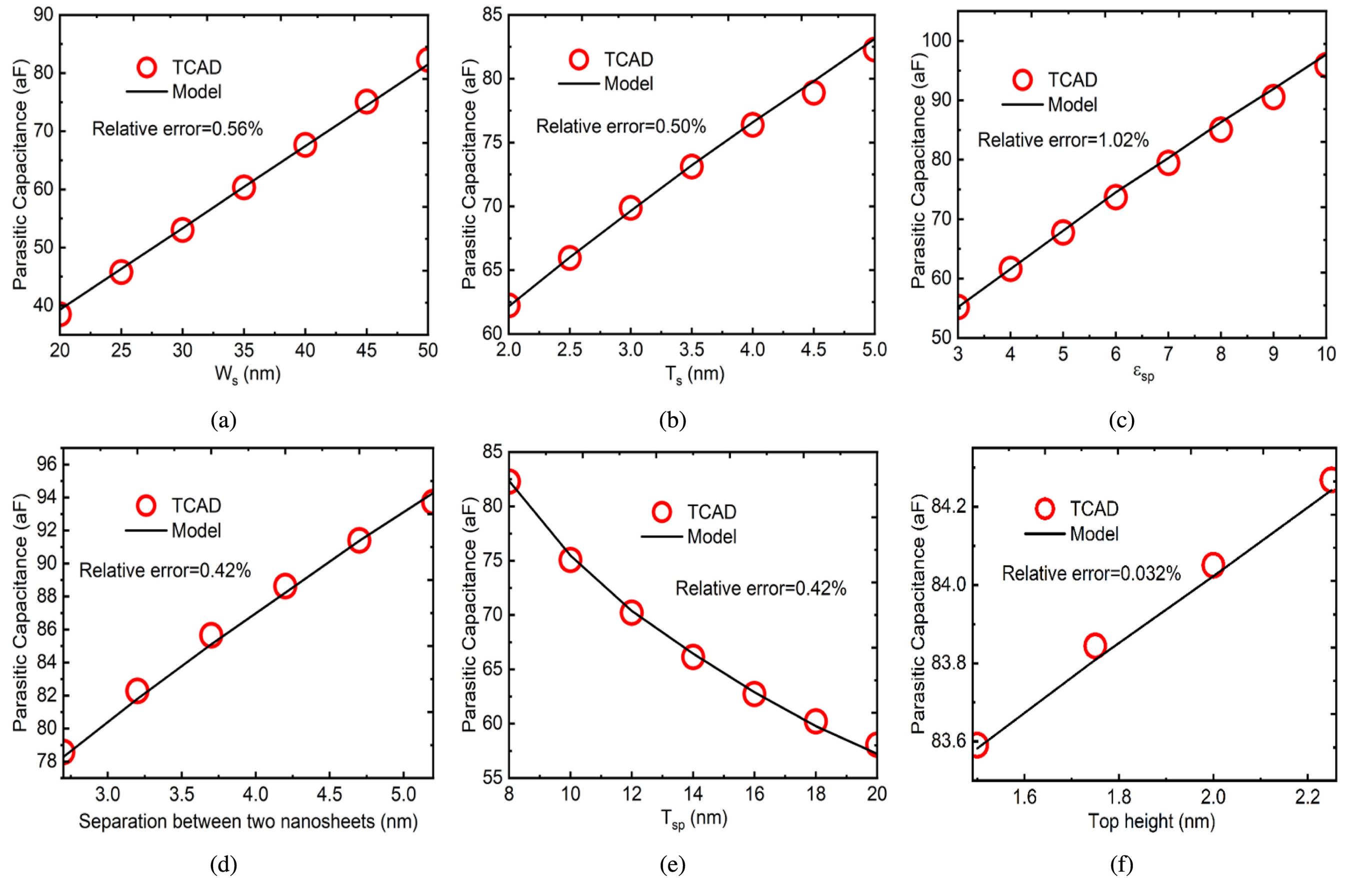

FIGURE 7. Comparison of parasitic capacitance of GAAFET between compact model (lines) and 3D TCAD simulation (symbols) with various (a) Nanosheet Width (W_s), (b) Nanosheet thickness (T_s), (c) Spacer-*k* value (ϵ_{sp}), (d) Separation between two nanosheets, (e) Spacer thickness (T_{sp}), and (f) Gate top height. The minimum relative error of model is 0.032% and the maximum is 1.02%.

or,

$$A_{sd} = H_{sd}W_{sd} - N_{GAA}\left(W_sT_s - T_s^2 + \frac{\pi}{4}T_s^2\right) \tag{14}$$

$$A_{fgsd} = H_{sd}W_{sd} - N_{GAA}\left[\pi\left(\frac{T_s}{2} + T_{FR}\right)^2 + (W_s - T_s)(T_s + 2T_{FR})\right] \tag{15}$$

where H_{sd} is the source or drain height and T_{FR} is the fringe thickness. We can model $C_{gsdo,pr7}$, and $C_{gsdo,pr10}$ in similar way. $C_{gsdo,pr1}$ has to be slightly modified. h_{top} has to be added with S/D height H_{sd} and the modified height will be $H_{sd,mod}= H_{sd} + h_{top}$.

IV. RESULTS AND DISCUSSION

The accuracy of the proposed parasitic capacitance model is validated through the 3D TCAD numerical simulation results. The following sections evaluate the impact of device parameters such as nanosheet width (W_s), nanosheet thickness (T_s), spacer k-value (ϵ_{sp}), separation between two nanosheets, spacer thickness (T_{sp}), and gate top height (h_{top}).

A. VERIFICATION OF THE PARASITIC CAPACITANCE MODEL

Fig. 7 shows the parasitic capacitance for various device geometries. Where the proposed model illustrates excellent agreement with 3D TCAD simulation results. The total parasitic capacitance increases as the nanosheet width (W_s) increases, as depicted in Fig. 7(a). With increasing W_s, S/D width also increased, leading to an increase of parallel capacitance $C_{gsdo,pr}$. Concurrently, gate-to-S/D extension capacitance also rises as the extension area increases, the reason behind this channel area increases with increasing nanosheet width. The capacitance of the top plate of the gate to the S/D electrode is also raised slightly. The relative error is only 0.56%. With increasing nanosheet thickness, S/D height also increases, so it only impacts parallel capacitance C_{gsdo}. The remaining parasitic elements are unchanged. The model and simulation results are illustrated in Fig. 7(b), where the relative error is 0.50%. The dielectric constant of the spacer (ϵ_{sp}) has a direct impact on the capacitances as it serves as the dielectric for all perpendicular ($C_{gsdex,pp}$), parallel ($C_{gsdo,pr}$,), and corner capacitances ($C_{cr,pr}$). All capacitance values have risen with increasing spacer dielectric, resulting in total capacitance increases, as shown in Fig. 7(c). The accuracy is more for lower dielectric constant

in comparison to higher dielectric and it is crucial when designing devices for low-delay circuits and requires the use of low-k spacers [33], [34]. The relative error is 1.02%. All parallel plate capacitances, with the exception of the top parallel plate, are affected by the separation of two nanosheets, whether other parasitic components are unchanged. S/D height increases as gate height does with increasing separation between two nanosheets. Hence, the area of S/D electrode increase leads to an increase in parallel capacitance, which in turn causes an increase in total capacitance, as mentioned in Fig. 7(d). The relative error is 0.42%. The spacer thickness T_{sp} has a significant impact on all parallel and coplanar capacitances. Since T_{sp} serves as the denominator for both parallel ($C_{gsdo,pr}$) and coplanar capacitances ($C_{gsdo,cop}$), the capacitance value decreases as T_{sp} increases. Subsequently, the total parasitic capacitance decreases as the T_{sp} increases, as illustrated in Fig. 7(e). The relative error is 0.42%. The top-located parallel ($C_{gsdo,pr1}$) capacitance is the only component of capacitance that is affected by gate top height (h_{top}), whereas the other components are unchanged. Since h_{top} increases, the area of the S/D electrode likewise rises, leading to rising $C_{gsdo,pr1}$ and so does the total capacitance, as mentioned in Fig. 7(f). Hence, it is rising very slightly which is also evident from 7(f). The minimum relative error is obtained here with 0.032%.

B. COMPARISON WITH REPORTED WORKS

In comparison to recently published related works, the proposed compact model for parasitic capacitance is more sophisticated due to the following aspects: 1) The proposed model includes corner capacitance which is crucial to practical GAAFET, as opposed to [25], [26], where explicit physics-based model for corner rounding capacitance was not included. 2) The proposed model showed good comparison considering specific geometry parameters of GAAFET with respect to industry standard BSIM-CMG. 3) As just two fitting parameters are employed in the proposed model compared to five in [25], the complexity of the recommended model is less than that of the [25]. 4) The proposed model shows better accuracy in comparison to [25], [26]. The worst case accuracy is ≈ 99% for proposed model, while it is ≈ 97% and ≈ 96% for [25], and [26] respectively. The detailed comparisons are demonstrated in tabular form in Table 5.

C. CIRCUIT PERFORMANCE

To verify the accuracy of the proposed parasitic capacitance model, we have also performed circuit simulation. The proposed parasitic model has been implemented in the latest industry-standard BSIM-CMG framework using Verilog-A. Following that, this framework has been calibrated with 3D TCAD simulation results for a particular geometry [W_s=50nm, T_s=5nm]. Additionally, the default BSIM-CMG framework has also been calibrated with simulation results for the same geometry. The effects of parasitic capacitance on *RF* and the 17-stage ring oscillator are then demonstrated using these calibrated configurations. The circuit performance metrics, although identical at the calibrated point, deviate significantly for different geometries due to the inaccuracy of the existing BSIM model.

TABLE 5. Comparison with recently released related works.

Criteria	Recently Released Related Works [25]	Recently Released Related Works [26]	Proposed Work
Physics-based corner-rounding component	Not included	Not included (implicit approx)	Included explicit model for the corner capacitance
Industry-standard BSIM-CMG	Compared	No comparison	Compared
Accuracy (worst case)	≈ 97%	≈ 96%	≈ 99%
Accuracy (best case)	≈ 99.6%	≈ 98%	≈ 99.97%

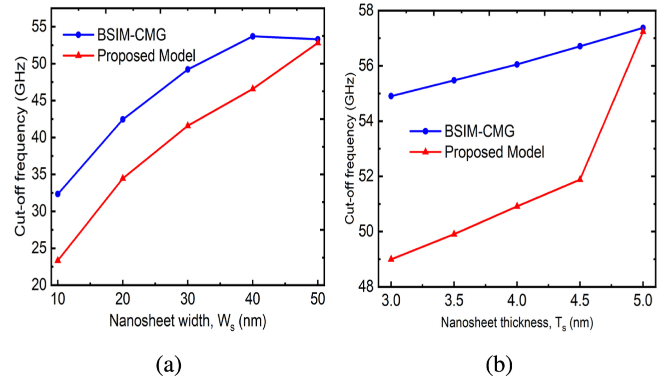

FIGURE 8. Comparison of cut-off frequency using proposed parasitic capacitance model and default BSIM-CMG for variation of (a) Nanosheet width (W_s), and (b) thickness (T_s).

(1) RF Performance: The *RF* performance is demonstrated by analyzing the Cut-off frequency. It is also regarded as a performance metric for high-frequency devices. The equation can be used to determine the cut-off frequency f_T as follows

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{16}$$

The cut-off frequency for nanosheet width and thickness is shown in Fig. 8 based on both the default BSIM-CMG and the proposed capacitance model. The default BSIM-CMG model predicts greater f_T than those of the proposed model for both width and thickness variation. This is because the existing BSIM-CMG does not capture the impact of W_s and T_s on parasitic capacitances accurately.

(2) Ring Oscillator Delay: The impacts of parasitic capacitance on the 17-stage ring oscillator are also demonstrated in this section. Fig. 9(a) and (b) show the delay variation with respect to W_s and T_s. As can be seen from Fig. 9, the delay based on the suggested model is larger with respect to W_s and T_s by 13% and 18.37%, respectively, as compared to the default BSIM-CMG capacitance model. This is due to the inaccuracy of the existing parasitic model in BSIM-CMG.

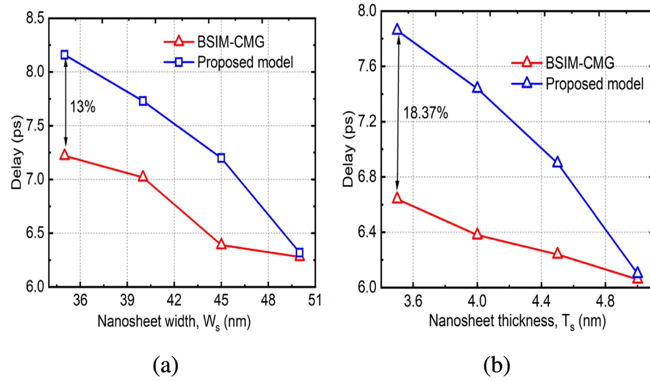

FIGURE 9. Delay per stage of a 17-stage ring oscillator using proposed capacitance model and default BSIM-CMG for variation of (a) Nanosheet width (W_S), and (b) thickness (T_S).

V. CONCLUSION

A complete compact model of the entire parasitic capacitance network for stacked Gate-all-around nanosheet FETs (GAAFETs) is proposed in this paper. Various methods such as conformal mapping, elliptic integral, and Schwarz-Christoffel transforms are used to calculate each capacitance component of different parts. The total parasitic capacitance exhibits excellent agreement with 3D TCAD numerical simulation results for different device parameters. The model has been implemented in Verilog-A and incorporated in the industry standard BSIM-CMG framework. Circuit simulation results show significant impact of the parasitic capacitance model on device and circuit performance. This makes the proposed model indispensable for efficient first-pass design.

APPENDIX

According to Fig. 3(a), the innermost ellipse gives the common focus

$$f^2 = x^2 - y^2 \tag{17}$$

where f is the focus of the innermost ellipse. The perpendicular plate capacitance can now be mapped into the corresponding parallel plate capacitance using conformal mapping, as shown in Fig. 3(b), and the transformation from xy coordinates to uv coordinates is as follows:

$$u + jv = F(x + jy) \tag{18}$$

From [26], we find that $F = cos^{-1}$ is an appropriate function to transform from elliptical geometry to linear geometry, which offers

$$x = f\, cos\, u\, cosh\, v \tag{19}$$

$$y = -f\, sin\, u\, sinh\, v \tag{20}$$

Since the fringing capacitance inside the perpendicular plate is not accounted for in this instance, so this component of capacitance must be taken into account separately. Apart from the confocal elliptical model, subsequent transformations employing the elliptic integral must be performed [20], as shown in Fig. 4. Initially the perpendicular plate is transformed to collinear plate by using the conformal mapping technique

$$w = z^2 = (x + jy)^2 \tag{21}$$

solving the above equation, we get

$$u = x^2 - y^2 \tag{22}$$

$$v = 2xy \tag{23}$$

After solving the above equations and putting the previous coordinate values we get the updated plate endpoint coordinates in the (u, v) coordinate system as

$$\begin{aligned} p &= -(y_1 + y_2)^2 \\ q &= -y_1^2 \\ r &= x_1^2 \\ s &= (x_1 + x_2)^2 \end{aligned} \tag{24}$$

In the following step, another transformation technique named Schwarz-Christoffel theorem is applied to convert collinear plate to parallel plate, which is determined by [29], [30]

$$C_{pp} = \epsilon \frac{|p'q'|}{|q'r'|} = \epsilon \frac{K(k)}{K(k')} = \epsilon \frac{K(k)}{K\left(\sqrt{1-k^2}\right)} \tag{25}$$

where ϵ is the dielectric constant of the considered material, and $k' = \sqrt{1-k^2}$ and $k = \sqrt{(\frac{q-p}{r-p})(\frac{s-r}{s-q})}$.

By taking approximation of equation (29) from [29], with relative error of 3×10^{-6}, we can write

$$\begin{aligned} C_{pp} &= \epsilon \frac{W}{\pi} \ln\left[2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right], \; for, \; \frac{1}{\sqrt{2}} < k < 1 \\ &= \epsilon \frac{\pi W}{\ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]}, \; for, \; 0 < k < \frac{1}{\sqrt{2}} \end{aligned} \tag{26}$$

REFERENCES

[1] S. E. Thompson and S. Parthasarathy, "Moore's law: The future of Si microelectronics," *Materialstoday*, vol. 9, no. 6, pp. 20–25, Jun. 2006
[2] *International roadmap for devices and systems moremoore white paper*. 2020. [Online]. Available: https://irds.ieee.org/images/files/pdf/2020/2020IRDS MM.pdf
[3] Y. Taur, "CMOS design near the limit of scaling," *IBM J. Res. Develop.*, vol. 46, nos. 2–3, pp. 213–222, Mar. 2002, doi: 10.1147/rd.462.0213.
[4] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012, doi: 10.1109/TED.2012.2193129.
[5] P. Ye, T. Ernst, and M. V. Khare, "The last silicon transistor: Nanosheet devices could be the final evolutionary step for Moore's law," *IEEE Spectrum*, vol. 56, no. 8, pp. 30–35, Aug. 2019, doi: 10.1109/MSPEC.2019.8784120.
[6] J. Ryckaert et al., "From design to system-technology optimization for CMOS," in *Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, Apr. 2021, pp. 1–2. doi: 10.1109/VLSI-TSA51926.2021.9440115.
[7] S. B. Samavedam et al., "Future logic scaling: Towards atomic channels and deconstructed chips,"in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2020, pp. 1–10, doi: 10.1109/IEDM13553.2020.9372023.
[8] A. Mocuta, P. Weckx, S. Demuynck, D. Radisic, Y. Oniki, and J. Ryckaert, "Enabling CMOS scaling towards 3nm and beyond,"in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 147–148.
[9] J. Ryckaert et al., "Enabling sub-5nm CMOS technology scaling thinner and taller," in *IEDM Tech. Dig.*, Dec. 2019, pp. 685–688.
[10] Y.-C. Huang, M.-H. Chiang, S.-J. Wang, and J. G. Fossum, "GAAFET versus pragmatic FinFET at the 5nm Si-based CMOS technology node,"*IEEE J. Electron Devices Soc.*, vol. 5, no. 3, pp. 164–169, May 2017, doi: 10.1109/JEDS.2017.2689738.

[11] U. K. Das et al., "Limitations on lateral nanowire scaling beyond 7-nm node," *IEEE Electron Devices Lett.*, vol. 38, no. 1, pp. 9–11, Jan. 2017, doi: 10.1109/LED.2016.2629420.
[12] X. Yin et al., "Vertical sandwich gate-all-around field-effect transistors with self-aligned high-k metal gates and small effective-gate-length variation," *IEEE Electron Devices Lett.*, vol. 41, no. 1, pp. 8–11, Jan. 2020, doi: 10.1109/LED.2019.2954537.
[13] S.-G. Jung, J.-K. Kim, and H.-Y. Yu, "Analytical model of contact resistance in vertically stacked nanosheet FETs for sub-3-nm technology node,"*IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 930–935, Mar. 2022, doi: 10.1109/TED.2022.3143473.
[14] A. Dasgupta et al., "BSIM compact model of quantum confinement in advanced nanosheet FETs," *IEEE Trans. Electron Devices*, vol. 67, no. 2, pp. 730–737, Feb. 2020, doi: 10.1109/TED.2019.2960269.
[15] A. Agrawal et al., "Gate-all-around strained Si0.4Ge0.6 nanosheet PMOS on strain relaxed buffer for high performance low power logic application", in *IEEE Int. Electron Devices Conf. Tech. Dig. (IEDM)*, 2020, pp. 15–18.
[16] A. Dasgupta, P. Rastogi, A. Agarwal, C. Hu, and Y. S. Chauhan, "Compact modeling of cross-sectional scaling in gate-all-around fets: 3-D to 1-D transition," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 1094–1100, Mar. 2018, doi: 10.1109/TED.2018.2797687.
[17] G. Bae et al., "3nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications", in *IEEE Int. Electron Devices Conf. Tech. Dig. (IEDM)*, 2018, pp. 656–659.
[18] N. Loubet et al., "Stacked nanosheet gate-all-around transistor to enablescaling beyond FinFET," in *Proc. Symp. VLSI Technol.*, 2017, pp. T230–T231, doi: 10.23919/VLSIT.2017.7998183.
[19] K. Nayak et al., "CMOS logic device and circuit performance of Si gate all around nanowire MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3066–3074, Sep. 2014. doi: 10.1109/TED.2014.2335192.
[20] J. Kim, M. Kang, J. Jeon, and H. Shin, "Fringe capacitance modeling in nanoplate MOSFET using conformal mapping," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2446–2449, May 2019, doi: 10.1109/TED.2019.2903546.
[21] B. Sun et al., "Analytical model of CFET parasitic capacitance for advanced technology nodes," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 936–941, Mar. 2022, doi: 10.1109/TED.2022.3144648.
[22] J. Zou, Q. Xu, J. Luo, R. Wang, R. Huang, and Y. Wang, "Predictive 3-D modeling of parasitic gate capacitance in gate-all-around cylindrical silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3379–3387, Oct. 2011, doi: 10.1109/TED.2011.2162521.
[23] X. Dong et al., "Impact of gate asymmetry on gate-all-around silicon nanowire transistor parasitic capacitance,"in *Proc. IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, Oct. 2018, pp. 1–3, doi: 10.1109/icsict.2018.8565686.
[24] T. An and S. Kim, "3-D modeling of fringing gate capacitance in gate-all-around cylindrical silicon nanowire MOSFETs," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, Glasgow, U.K., 2013, pp. 256–259, doi: 10.1109/SISPAD.2013.6650623.
[25] J. Suk et al., "Analytical parasitic resistance and capacitance models for nanosheet field-effect transistors," *IEEE Trans. Electron Devices*, vol. 70, no. 6, pp. 2941–2946, Jun. 2023, doi: 10.1109/TED.2023.3270398.
[26] S. Sharma, S. Sahay, and R. Dey, "Parasitic capacitance model for stacked gate-all-around nanosheet FETs," *IEEE Trans. Electron Devices*, early access, Jun. 12, 2023, doi: 10.1109/TED.2023.3281530.
[27] A. Bansal, B. C. Paul, and K. Roy, "Modeling and optimization of fringe capacitance of nanoscale DGMOS devices," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 256–262, Feb. 2005, doi: 10.1109/TED.2004.842713.
[28] A. Bansal, B. C. Paul, and K. Roy, "An analytical fringe capacitance model for interconnects using conformal mapping," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 12, pp. 2765–2774, Dec. 2006, doi: 10.1109/TCAD.2006.882489.
[29] G. Hiblot, Q. Rafhay, F. Boeuf, and G. Ghibaudo, "Refined conformal mapping model for MOSFET parasitic capacitances based on elliptic integrals," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 972–979, Mar. 2015, doi: 10.1109/TED.2015.2388788.
[30] Y. Xiang, "The electrostatic capacitance of an inclined plate capacitor,"*J. Electrostatics*, vol. 64, no. 1, pp. 29–34, Jan. 2006, doi: 10.1016/j.elstat.2005.05.002.
[31] W. Hilberg, "From approximations to exact relations for characteristic impedances," in *IEEE Trans. Microw. Theory Techn.*, vol. 17, no. 5, pp. 259–265, May 1969, doi: 10.1109/TMTT.1969.1126946.
[32] X. Yang, Y. Sun, Z. Liu, Y. Liu, X. Li, and Y. Shi, "3-D modeling of fringe gate capacitance in complementary FET (CFET)," *IEEE Trans. Electron Devices*, vol. 69, no. 11, pp. 5978–5984, Nov. 2022, doi: 10.1109/TED.2022.3207974.
[33] T. Yamashita et al., "A novel ALD SiBCN low-k spacer for parasitic capacitance reduction in FinFETs," in *Proc. Symp. VLSI Technol. (VLSI Technology)*, Kyoto, Japan, 2015, pp. T154–T155, doi: 10.1109/VLSIT.2015.7223659.
[34] A. B. Sachid, M.-C. Chen, and C. Hu, "Bulk FinFET with low-k spacers for continued scaling," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1861–1864, Apr. 2017, doi: 10.1109/TED.2017.2664798.