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A Low Loss and High Selectivity GaN-on-Si On-Chip Bandpass Filter

GUANGHAO GUAN[1], JINGXIONG CHEN[2], XIAOYI LIU[2], AND HONG WANG[1,3]

1 Engineering Research Center for Optoelectronics of Guangdong Province, School of Physics and Optoelectronics, South China University of Technology, Guangzhou 510640, China
2 Engineering Research Center for Optoelectronics of Guangdong Province, School of Electronics and Information Engineering, South China University of Technology, Guangzhou 510640, China
3 Zhongshan Institute of Modern Industrial Technology, South China University of Technology, Zhongshan 528437, China

CORRESPONDING AUTHOR: H. WANG (e-mail: phhwang@scut.edu.cn)

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ABSTRACT We propose a low loss and high selectivity bandpass filter with defected structure on GaN-on-Silicon. GaN-on-Si exhibits a high insertion loss due to the presence of parasitic channels at the AlN/Si interface. It is necessary to strengthen the coupling between the resonators to achieve a low loss. However, this results in weaker suppression of adjacent channels and lower selectivity of frequencies. The designed filter consists of square spiral defect structure resonators and a step impedance resonator, which provides tunable transmission zero and facilitates the adjustment of pass band. With an interdigitated capacitor, at a frequency span from 3.3 to 4.9 GHz, the proposed filter has a low insertion loss of 2.71dB and improves the suppression of adjacent channel (5.8 GHz) by 11.2 dB compared to the traditional SIR filter. The out-of-band suppression of the filter is better than 15.93 dB at 20 GHz. Compared to the traditional SIR filter, the proposed filter achieves a steep transition zone, and an out-of-band rejection reduction by at least 6.6 dB.

INDEX TERMS Bandpass filter (BPF), coplanar waveguide, defect structure, GaN-on-Si, on-chip.

I. INTRODUCTION

With the rapid development of wireless communications, WiFi 5G applications urgently need to integrate radio frequency (RF) devices into system-on-chip (SoC) or system-in-package (SiP) in to achieve a cost-effective system-level solution [1], [2]. GaN has a higher electron drift saturation speed and a relatively strong breakdown field [3], [4]. Currently, GaN-based RF devices have significant advantages in satellite communication, 5G communication, and microwave radar [5]. Chip-to-chip interconnectivity is a common cause of unnecessary parasitic losses in lumped element devices, which reduces the overall RF performance. The integration of GaN-on-Si RF devices into SoC will greatly avoid this loss. Moreover, numerous studies have been conducted on the potential of active devices in current GaN-on-Si technology [6]. Because GaN active device processes, such as HEMT, are still in development, and are not suitable for fabricating passive devices with complex processes due to process incompatibility and interconnect insertion losses. Single-metal layer CPW is easy to realize series and parallel circuit, grounding does not need through direct perforation, characteristic impedance range is more comprehensive, easy to identify the on-wafer test.

Some works on on-chip bandpass filters (BPFs) have been published in the literature, designed with standard silicon-based technologies [7], [8], [9], or GaAs [10], [11], focusing on in-band flatness [12], and improving out-of-band suppression [13]. However, the issue of insertion loss has not been addressed in previous studies. According to published literature, it is extremely challenging to design an on-chip BPF with superior insertion loss over 2 dB in a standard silicon process [14]. When GaN films are grown on Si substrate, AlN, AlGaN, and other films are first grown on the Si substrate due to lattice and thermal mismatch. However, the presence of a parasitic channel at the AlN/Si interface results in a higher insertion loss of the GaN-on-Si [15], [16]. It is necessary to strengthen the coupling between the resonators to achieve a low loss. However, this results in weaker

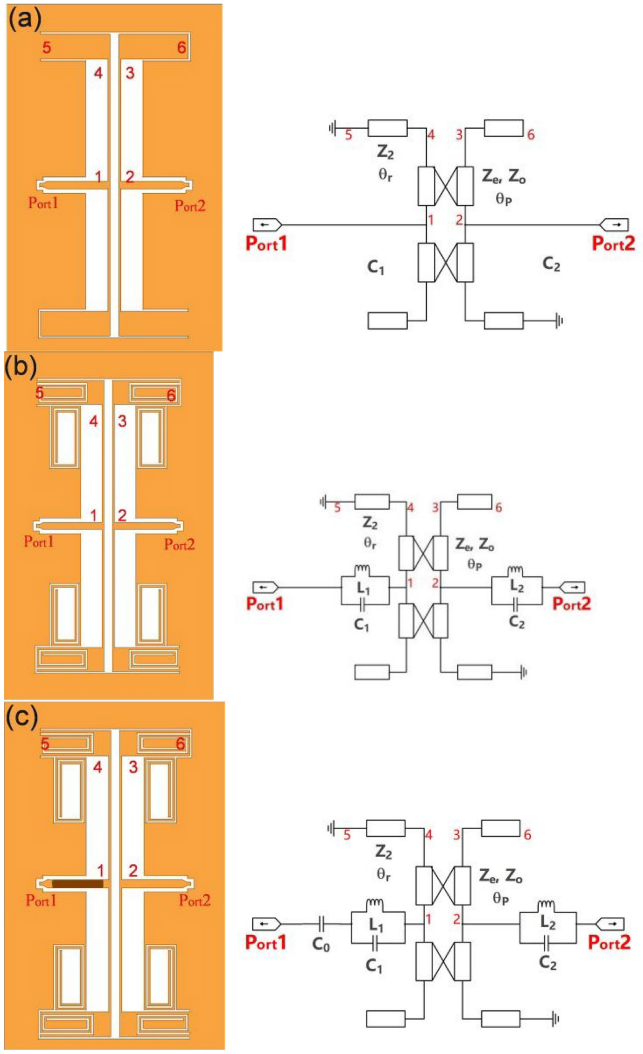

FIGURE 1. The structure and the equivalent circuit of (a) the conventional filter [7], BPF0 and the proposed (b) BPF1 (c) BPF2.

suppression of neighboring channels and lower selectivity for frequency. To our knowledge, there was a small amount of on-chip passive BPF of similarly structured GaN-on-Si. Achieving a low-loss and high-selectivity BPF on a lossy substrate (GaN-on-Si) is challenging.

We propose a low-loss and high-selectivity bandpass filter with defect structure on GaN-on-Si. The insertion loss within the passband is about 2.71 dB, with the second harmonic suppression being higher than 15 dB. It also has a great suppression effect on the adjacent channels (5.8 GHz), at 23.1dB.

II. RESONATOR AND BPF DESIGNS

A. COUPLED LINE RESONATORS

As shown in Fig. 1, where Z_2 is the impedance of the low-impedance line with the length of θ_r, Z_o, and Z_e are the odd-mode and even-mode impedances of high-impedance lines with the length of θ_p. The proposed resonator can be simplified as a pair of anti-coupled lines. The straight end is open and the coupling end is short circuit. And Z2: $\sqrt{Z_eZ_o}$ =1:3, can be considered as a SIR.

We can let the port impedance of conventional resonator, Z_0=50 ohm and Z_{lump}=0, while the Z_{lump} tuned by the proposed structure will be discussed in Part B and C. The circuit in Fig. 1(a) can be bisected into two halves along the central plane due to the symmetry. And then the odd- and even-mode analysis method can be adopted.

$$Z_{in1e} = jZ_e * \frac{Z_e \tan(\theta_p) \tan(\theta_r) - Z_2}{Z_e \tan(\theta_r) + Z_2 \tan(\theta_p)} \tag{1}$$

$$Z_{in2e} = jZ_e * \frac{Z_e \tan(\theta_p) + Z_2 \tan(\theta_r)}{Z_e - Z_2 \tan(\theta_p) \tan(\theta_r)} \tag{2}$$

$$Z_{in1o} = jZ_o * \frac{Z_o \tan(\theta_p) \tan(\theta_r) - Z_2}{Z_o \tan(\theta_r) + Z_2 \tan(\theta_p)} \tag{3}$$

$$Z_{in2o} = jZ_o * \frac{Z_o \tan(\theta_p) + Z_2 \tan(\theta_r)}{Z_o - Z_2 \tan(\theta_p) \tan(\theta_r)} \tag{4}$$

$$Z_u = \frac{1}{2}\begin{bmatrix} Z_{in1e} + Z_{in1o} & Z_{in1e} - Z_{in1o} \\ Z_{in2e} - Z_{in2o} & Z_{in2e} + Z_{in2o} \end{bmatrix} \tag{5}$$

$$Z_d = \frac{1}{2}\begin{bmatrix} Z_{in2e} + Z_{in2o} & Z_{in2e} - Z_{in2o} \\ Z_{in1e} - Z_{in1o} & Z_{in1e} + Z_{in1o} \end{bmatrix} \tag{6}$$

where Z_{in1o}, and Z_{in1e} are odd-mode input impedance and even-mode input impedance at node 1, respectively. Z_{in2o}, and Z_{in2e} are odd-mode input impedance and even-mode input impedance at node 2. Z_u and Z_d are the Z parameters of the structures of the left part and right part of Fig. 1.

Converting the Z parameters to Y parameters solves the Y_u from Z_u, and similarly, find Y_d, let $Y = (Y_u + Y_d)$, and then converts the Y parameters to S parameters, so

$$S_{21} = \frac{Z_{in1e} + Z_{in2e} - Z_{in1o} - Z_{in2o}}{2Z_0} / \times \left(\frac{\left(1 + \frac{Z_{lump}}{2}\right)(Z_{in1e} + Z_{in2e} + Z_{in1o} + Z_{in2o})}{2Z_0} + \frac{(Z_{in1e}Z_{in2o} + Z_{in1o}Z_{in2e})}{(2Z_0)^2} + \frac{(1 + Z_{lump})(Z_{in1e} + Z_{in2e})(Z_{in1o} + Z_{in2o})}{Z_{in1e}Z_{in2o} + Z_{in1o}Z_{in2e}} \right) \tag{7}$$

On the other hand, SIR can move the resonant frequency to a lower frequency [7], making the same transmission stop-band in a smaller size. Therefore, it is desirable to have a more significant step impedance ratio, but is limited by the size of the coplanar waveguide with huge dimensions of W2 and G1. Z2 =28.5, $\sqrt{Z_eZ_o}$=85.5, Z2:$\sqrt{Z_eZ_o}$ is near 1:3. Even though the best suppression can achieve with θ_r=θ_p=1/18 λ, as shown in Fig. 2 (b). To make the size smaller, θ_r=1/27 λ and θ_p=2/27 λ were chosen.

B. SPIRAL DEFECTIVE STRUCTURES RESONATORS

Defective ground structures (DGS) are widely used in filter design, especially in chip filters [17]. DGS spiral resonator

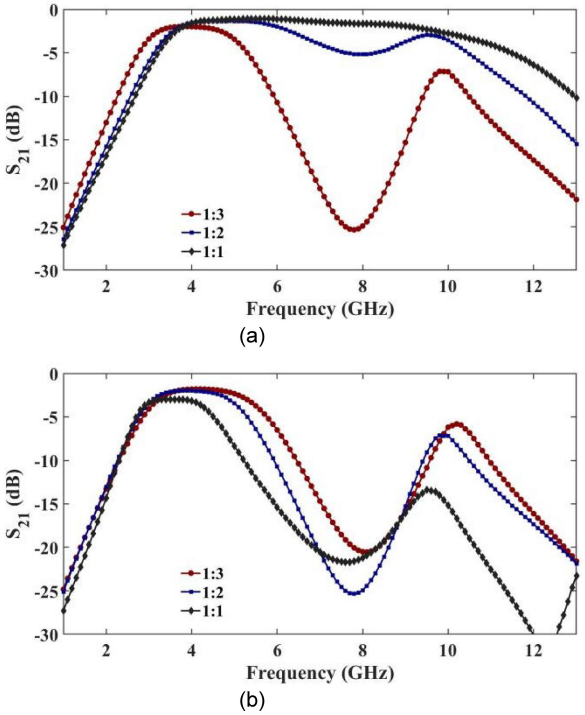

FIGURE 2. S21 under (a) different Z2: $\sqrt{Z_e Z_o}$ and (b) different $\theta_r : \theta_p$.

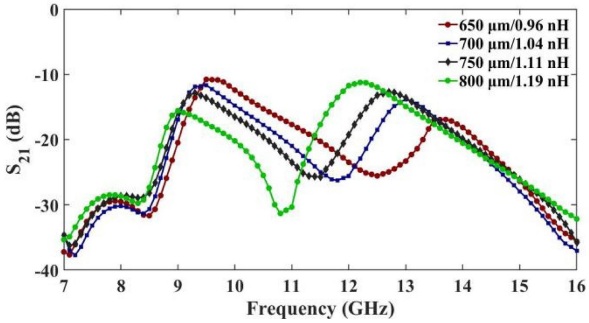

FIGURE 3. The length of the defective structure/ L_2 in relation to S_{21}.

TABLE 1. Relationships between parameters and transmission zeros (TZs) or transmission poles (TPs).

Symbol	C_0	C_1L_1	$Z_2/\sqrt{Z_eZ_o}$	θ_p/θ_r	Z_e/Z_o
f_{p1}	→	-	→	-	→
f_{p2}	-	-	→	-	-
f_{p3}	-	←	→→	-	←
f_{z1}	-	-	→→	-	→
f_{z2}	-	←	-	-	-

'→'means a positive correlation between the two, and '→→'means that multiple TZs or TRs are positively correlated, but this one is more sensitive;
'-'means that there is no obvious correlation between the two.

can be used as a notch filter to provide transmission zeros (TZs). By loading the DGS structure, TZs can be provided flexibly for the filter, not only to adjust the working bandwidth but also to provide a steeper transition band.

CPW transmission lines, a kind of double conducting wires, were added spiral defect structure for signal and ground in this work. Its low-frequency equivalent circuit can be simplified to a LC parallel resonant network with the inductance value L_1 and the capacitance value C_1. Also, there are complementation spiral-resonators in the low impedance section of the step impedance resonator, with an inductance value of L_2 and a capacitance value of C_2. ω_{01} and ω_{02} are resonant frequency, ω_{3dB1} and ω_{3dB2} are compressed by 3dB from the resonant frequency, and Z_{sr} is the impedance of the resonant network. ω_0, ω_{3dB}, and Z_{sr} can be obtained by EM simulation.

$$L_i * C_i = 1/\omega_{0i}^2 \tag{8}$$

$$\mathrm{Im}(Z_{sr}) * \omega = L_i * \left(\omega_{3dBi}^2 - \omega_{0i}^2\right) \tag{9}$$

C. INTERDIGITATED CAPACITOR AND FILTERS

In this work, we need a capacitor close to 1pF, so we simply etch the conductor wires of the input or/and output transmission lines into an interdigitated shape to form capacitor. The capacitance value is C_0.

$$Z_{ic} = \frac{1}{j\omega C_0} \tag{10}$$

Z_{ic} can be obtained by EM simulation. We can change the value of equivalent circuit like: C_0, C_1, C_2 and L_1, L_2 to change Z_{lump} and S_{21}

$$Z_{lump} = \frac{1}{j\omega C_0} + \frac{1}{\frac{1}{j\omega L_1} + j\omega C_1} + \frac{1}{\frac{1}{j\omega L_2} + j\omega C_2} \tag{11}$$

In this work, the SIR has a TZ located at f_{z1}, as the spiral-resonators, and complementation spiral-resonators located at f_{z2} and f_{z3}. We let $\omega_{01} = 2\pi f_{z2}$ slightly smaller than $2\pi f_{z1}$ to get a steeper transition zone. Moreover, f_{z3} is set between the fundamental passband and the 2nd passband to obtain broad stopband suppression, as shown in Fig. 3.

D. IMPROVEMENT OF THE PROPOSED FILTERS

The design requires achieving a passband in the frequency range of 3.3-4.9 GHz and rejecting adjacent channels in the frequency of 5.8 GHz, meaning that the upper edge of the passband attenuates rapidly. For the traditional structure of BPF0, the bandwidth needs to be further compressed to ensure that the adjacent 5.8 GHz channel is not disturbed. Simulation results show that BPF0 for S_{21} is only −10.3 dB at 5.8 GHz, while BPF1 and BPF2 are optimized to −21.5 dB and −23.1 dB, and the suppression of adjacent channels is compressed by 11.2 dB and 12.8 dB, respectively. The improvement has more than doubled. However, if the method proposed here is not applied, the bandwidth is compressed only weakly coupled by increasing the distance between the resonators, thus increasing the rejection rate at 5.8 GHz. As shown in Fig. 4, S_{21} is not only compressed to −17.1 dB, less than 20 dB, but also its in-band insertion

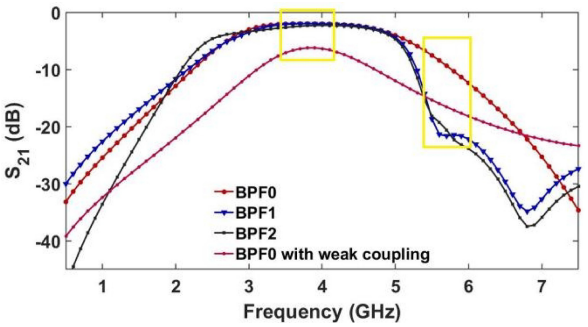

FIGURE 4. S21 of different structures. classical SIR filter (BPF0), BPF1, and BPF2.

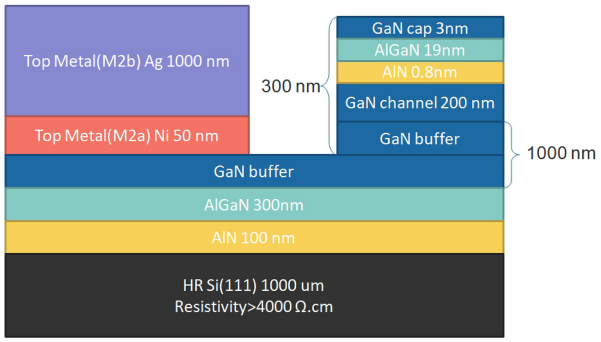

FIGURE 5. Structure of the passive device process.

loss reaches −6.2 dB. The shows that for the lossy substrate of GaN-on-Si, the method proposed maintains low insertion loss of the passband and achieves suppression of adjacent channels.

III. THE PASSIVE DEVICES TECHNOLOGY PROCESS AND MEASUREMENT

A. TECHNOLOGY PROCESS

The passive device technology is developed for integration and high performance in microwave applications. The process would begin with GaN on HR silicon wafer cleaning, and then 300nm in total GaN cap, AlGaN, AlN, and GaN channel was etched for MESA. Then, the top interconnection metallization (M2) was implemented by using a Ni/Ag metal layer with a thickness of 50 nm/1000 nm. A cross-sectional schematic of the passive device technology is shown in Fig. 5.

The proposed BPF is constructed on a top metal layer (M2) with a thickness of 50/1000 nm and was achieved by e-beam evaporation deposition. The input and output ports are realized with ground-signal-ground (GSG) probes for measurement convenience.

Two 50 ohm single-metal layer coplanar waveguide transmission lines of 1 mm and 0.5 mm in length were measured using the ENA Network Analyzer P9375A (1-26.5 GHz). Using the L-2L method to de-embed, we obtained the S of a 1mm 50 ohm CPW transmission line.

Based on the Helmholtz equation [18], the plane electromagnetic wave propagating in the same homogeneous medium can be expressed as

$$\nabla^2 E - \gamma^2 E = 0 \tag{12}$$

$$\gamma = j\omega\sqrt{\mu\varepsilon_{\text{eff}}}\left(1 + \frac{\sigma}{j\omega\varepsilon_{\text{eff}}}\right)^{1/2} \tag{13}$$

where γ is the propagation constant, σ, and ε_{eff} are the conductivity electrical conductance and relative permittivity of CPW transmission lines.

We measured the S-parameters of CPW transmission lines to get γ, then based equation (12) and (13), we get $\sigma = 0.090$ S/m and $\varepsilon_{\text{eff}} = 6.694$.

Therefore, we can use a uniform medium to replace Wafer for EM simulation.

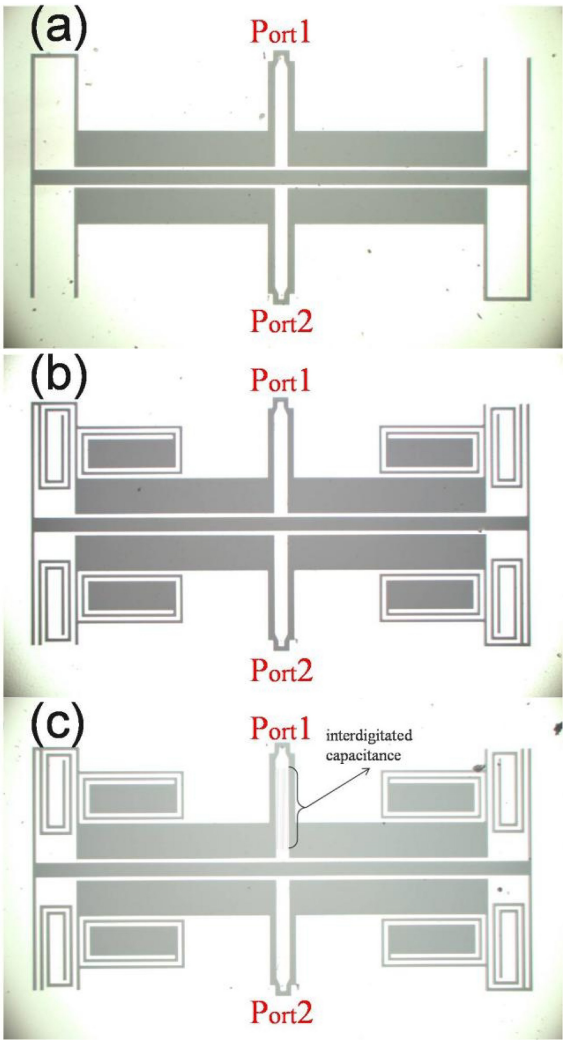

FIGURE 6. The microphotograph of the fabricated (a) classical SIR filter (b) BPF1 and (c) BPF2.

B. SIMULATION AND MEASUREMENT

To verify the proposed filter, three BPFs were designed with a center frequency of 4.1 GHz and a bandwidth of 1.6 GHz. The layout of the filters was designed and optimized by the HFSS. The size of the BPF, including the pads, is 2.203 mm × 4.510 mm.

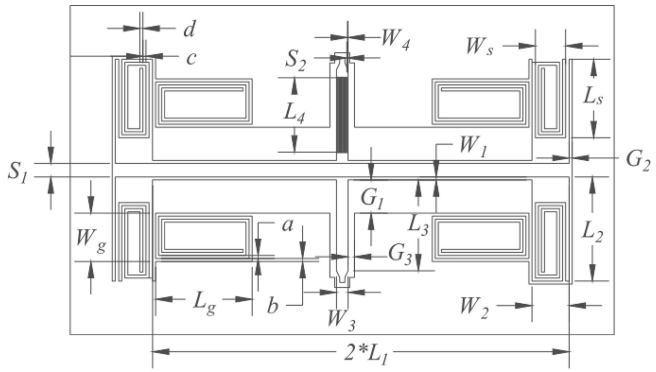

FIGURE 7. The structure and dimensions of the proposed filter.

TABLE 2. The dimensions of the fabricated filter.

Symbol	Value (μm)	Symbol	Value (μm)	Symbol	Value (μm)
W1	30	L1	2070	G1	330
W2	370	L2	1035	G2	30
W3	114	L3	903.5	G3	65
W4	6	L4	738	S1	133
Ws	300	Ls	780	S2	6
Wg	480	Lg	960	a	30
b	30	c	30	d	30

Fig. 8 and Fig. 9 show the measured S-parameters of the proposed filter using on-wafer probes with a network analyzer.

The designed layout was based on σ=0.052 S/m, ε_{eff} = 6.755. The simulation results for comparison were performed after the experiment according to σ=0.090 S/m, ε_{eff} = 6.694. Since the interdigital capacitors are very sensitive to errors.

The BPF1 has a return loss of less than 20 dB from 3.510 to 4.905 GHz, with the maximum value of 12.67 dB (@3.285 GHz) in the passband. The BPF2 has a return loss of less than 15 dB from 3.150 to 4.635 GHz, with the maximum value of 12.57 dB (@ 4.905 GHz) in the passband. The minimum and maximum insertion loss of BPF1 in the passband are 2.34 dB (@3.645GHz) and 4.78 dB (@4.905GHz), respectively, and BPF2 drops slightly to 2.71 dB (@3.645GHz) and 4.62 dB (@4.905GHz). The minimum insertion loss of BPF2 outside the passband (under 20 GHz) is 15.93 dB (@16.43 GHz). The second harmonic was measured at 18.42 GHz, and the S_{21} of BPF2 is 22.05 dB, meaning that the second harmonic passband is suppressed to around 20 dB.

Group delay is also an important parameter for measuring the linearity of the filter. As can been seen in Fig. 10, the in-band group delay of BPF0 is monotonically decreasing from 260 ps at 3.3 GHz to 168 ps at 4.9 GHz, which is not flat. Due to the introduction of the spiral defect structure, BPF1 rises sharply by about 5 GHz, while the $|S_{11}|^2+|S_{21}|^2$ also drops sharply, but the in-band group delay flattening,

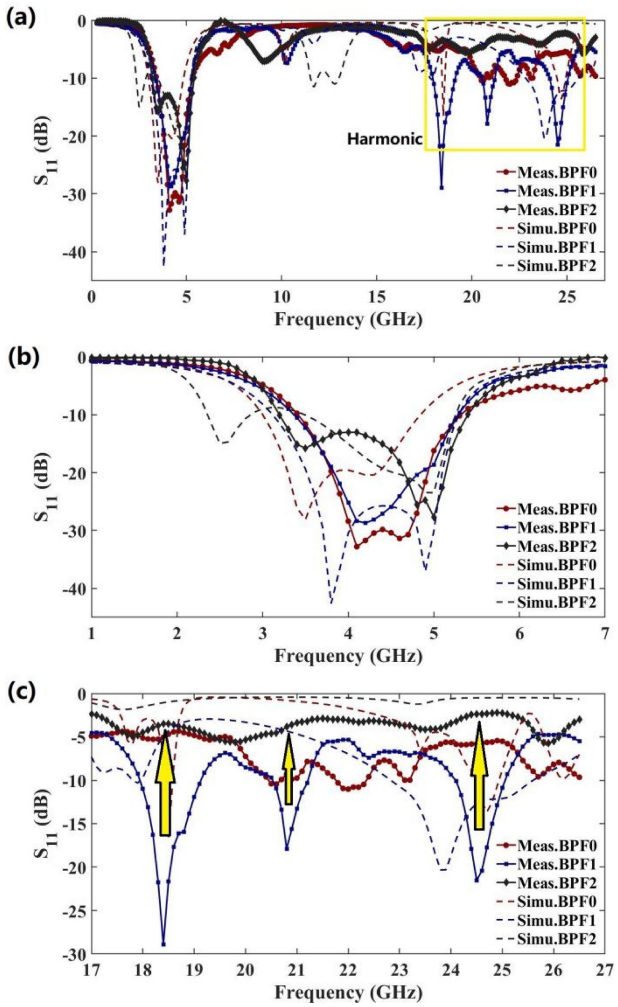

FIGURE 8. S_{11} of classical SIR filter (BPF0), BPF1, and BPF2 (a)1-26.5 GHz, (b) passband (1-7 GHz), (c) harmonic (17-26.5 GHz).

most of the frequency points are around 250 ps, with a maximum of 278 ps and a minimum of 244 ps. However, for interdigitated capacitor, BPF2 rises sharply around 3 GHz, with a smaller center frequency, and larger upper and lower edge frequencies, with a minimum of 241 ps and a maximum of 306 ps. Compared with BPF0, BPF1and BPF2 have a 92 ps difference in group delay, with a 63% and 30% reduction, respectively.

Operating frequency is slightly higher than the simulated results. It may be that the fabrication errors caused the difference and the difference between the measured and simulated results is acceptable in this design. It may also be that the interfacial defects of the wafers used to design the simulations cannot be easily attributed to the conductivity of the medium, or inhomogeneity of the wafer. Based on the test sample, the simulated conductivity, σ =0.052 S/m, which is smaller than the chip fabrication. And the effective dielectric constant, ε_{eff} =6.755, which is larger than the chip fabrication. A smaller ε_{eff} lead to a higher center frequency, and a bigger σ lead to a smaller $|S_{11}|^2 + |S_{21}|^2$.

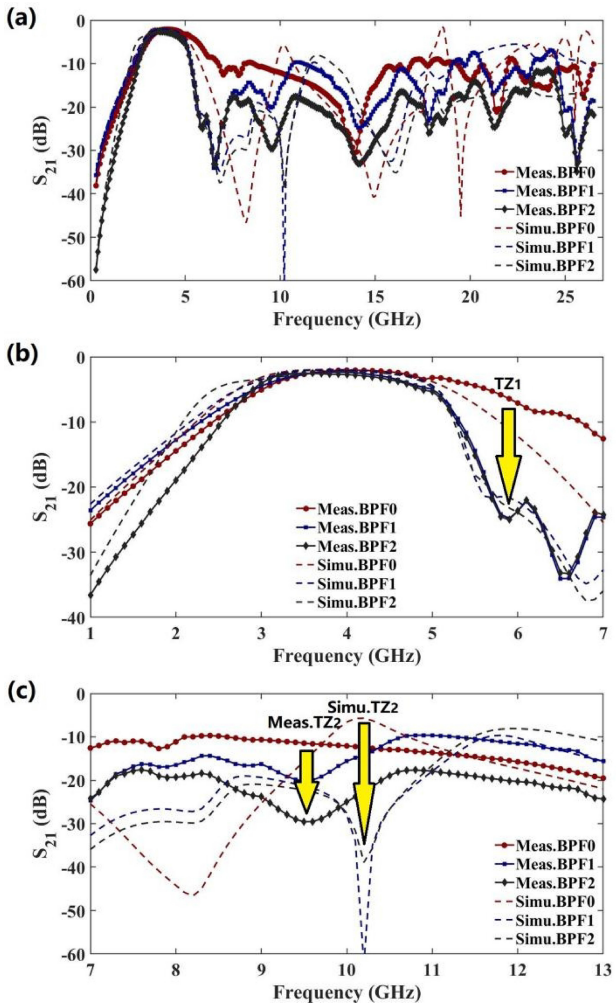

FIGURE 9. S_{21} of classical SIR filter (BPF0), BPF1, and BPF2 (a)1-26.5 GHz, (b) passband (1-7 GHz), (c) stopband (7-13 GHz).

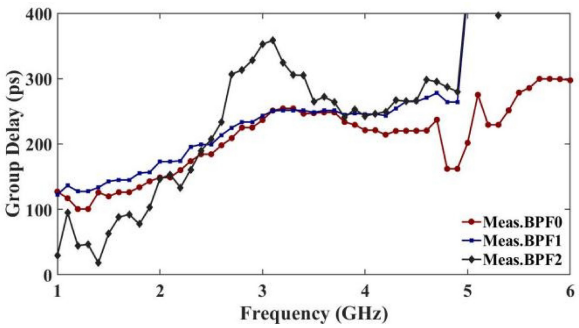

FIGURE 10. Measured group delay over the passband.

IV. CONCLUSION

We present two on-chip BPFs of 3.3-4.9 GHz using the 1-μm GaN-on-Silicon technology in the paper. Based on SIRs with defect structures, which can be seen as L-C equivalent circuit models, exhibit a wide stopband. The simulation results agree well with the measured results. This structure is only placed on the top metal layer, not only reducing the size, manufacturing steps and costs of mass production, but also being flexible to integrate with active circuits. The proposed filters have a compact size of 2.203 × 4.510 mm (0.075 λg x 0.154 λg, with λg = 29.3 mm). The insertion loss of BPF1 was 2.34 dB, improving the suppression of adjacent channel (5.8 GHz) compressed by 11.2 dB. When the insertion loss is 2.71dB, the return loss of BPF2, ranging from 3.15 to 4.65 GHz, is less than 15 dB. The maximum S21 outside the passband (below 20 GHz) is 15.93 dB (@16.43 GHz). Not only improved frequency selectivity but also reduced the maximum value of S21 by 6.6 dB in the 5.8-20 GHz range, achieving a wide stopband rejection.

It is difficult to implement filter below 2 dB on Si substrate. There are parasitic channels at the AlN/Si interface of GaN-on-Si. Achieving insertion losses below 2.5 dB is challenging. However, BPF1 was achieved and showed better and flatter return losses. The BPF2 exhibited a wide stop band. The filters had good RF performance and used only one metal layer, making it a good choice in GaN-on-Si radio frequency integrated circuit (RFIC) design.

TABLE 3. Performance of bandpass filters for SOC or SIP.

	Technology	Freq. span (GHz)	R.L. (dB)	I.L. (dB)	TPs	Size(mm2)	Area (λg2)
[19]	Roger RT/Duroid 6002	30.5-32.5	#5	3.5-10	3	2.45*1.46	0.47*0.28
[7]	0.18μm CMOS	57-64	<15	>3.5	1	##	##
[8]	0.13-μm CMOS	22.5-30.5	#4	2.5-5.5	2	0.8*0.35	0.06*0.16
[9]	0.13-μm CMOS	9.5-13.5	#3-4	3.2-7	2	0.88*0.54	0.04*0.066
[10]	0.5-μm GaAs	31.3-45	13.3	1.25-2.92	5	1.24*0.8	0.46*0.3
[11]	GaAs MMIC	27.3-32.7	<12	1.2	2	1.16	##
BPF0	GaN on Si	3.3-4.9	<9.23	2.04-3.19	3	2.203*4.510	0.075*0.154
BPF1	GaN on Si	3.3-4.9	<12.67	2.23-4.78	3	2.203*4.510	0.075*0.154
BPF2	GaN on Si	3.3-4.9	<12.57	2.41-4.62	3	2.203*4.510	0.075*0.154

#estimated from the data shown in the paper;
not described in the paper

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