Received 21 April 2023; accepted 26 August 2023. Date of publication 4 September 2023; date of current version 22 September 2023.
The review of this article was arranged by Editor K. Cheng.

Digital Object Identifier 10.1109/JEDS.2023.3311763

Simulation of In-Situ Training in Spike Neural Network Based on Non-Ideal Memristors

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This work was supported by the Shanghai Aerospace Science and Technology Innovation Fund.

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ABSTRACT In this paper, we proposed a multilayer supervised training method based on Multi-Resume and memristor synaptic properties. We use a new differential equation describe the dynamic of Pt/HfO_2/Al_2O_3/Ti devices and update weights based on present conductance. Specifically, the weight update is achieved by applying just one pulse to the device, which will simplify the peripheral circuits. In addition, the algorithm training method, asymmetric nonlinear weight update and synaptic variation measured from experiments are investigated for the impact on network accuracy. Our results show that the nonlinearity of devices does not much affect the network accuracy; The hybrid training is a better method for ensuring the accuracy; The spiking neural network (SNN) shows remarkable high tolerance to the variation of the device. This work will lay the foundation for later on-chip learning of SNN based on memristors. (Optdigits dataset: http://archive.ics.uci.edu/ml)

INDEX TERMS Memristor, synaptic plasticity, nonlinearity, asymmetry, spike neural network.

I. INTRODUCTION

Memristors have broad application prospects in low power consumption and embedded computing devices due to their advantages such as non-volatility, low energy consumption and low area cost [1], [2], [3]. Nowadays, many scholars suggest using RRAM to perform matrix-vector multiplication operations efficiently at neuromorphic computing and artificial neural network. However, the non-idea conductance modulation mechanism of RRAM will significantly affect the accuracy of learning, making it very challenging to apply to neuromorphic chips [4], [5], [6], [7].

On the other hand, the main goal of neuromorphic chips is to develop biomimetic artificial systems that can reduce power consumption and improve computing speed. Compared with Artificial Neural Networks (ANNs) [1], [2], SNNs is not only a high degree of bionics, but also a discrete spikes-based model in time, with less energy consumption, which is more conducive to edge calculation [7], [9].

Generally, the current in memristors undergoes a continuous gradual change with continuous pulse. It should be noted that the majority of memristors suffer from the non-ideal issues. Such non-ideal issues will affect the performance of memristive network. Through previous research, innovation in structure mechanism and operation method can alleviate non-ideal problems. However, it is apparent that ideal device will cause low process reliability and complex peripheral circuits [10], [11]. Furthermore, some works have made great progress on the asymmetric nonlinear update weights of RRAM in ANNs, [12], [13], [14], [15], [16], [17] but for the SNNs, there is only few research on no-ideal devices. For previous SNN work on memristors, the key factor of the time dynamics of the neurons is still lack, [18] or adopting an unsupervised learning with STDP methods [19]. Here, the asymmetric nonlinear weight updating method is used to investigate the influence of device non-ideal factors on SNN in-situ training.

This work focused on the SNN design employing Pt/HfO_2/Al_2O_3/Ti synaptic devices deposited by atomic layer deposition (ALD). Firstly, the electrothermal coupling model established by COMSOL is used to explain the switching mechanism of the device. Next, the synaptic plasticity of the device is verified, and then we propose the multilayer supervised STDP based on Multi-Resume and memristor synaptic properties. In the process of in-situ learning, we not only

use the differential kinetic equation to describe the synaptic behavior of the device, but also update the weights according to the present state of the synaptic conductance. It is worth mentioning that the weight update is accomplished by applying only one pulse at a time. Then, these characteristics are incorporated into the network to explore the impact of non-ideal devices and network training methods on accuracy. The results show that although the non-ideal characteristics of RRAM reduce the speed of training, the accuracy will not be greatly affected. Meanwhile, the equation form proposed in this article provides a basis for designing the waveform to avoid non-ideal characteristics. This work may lead to the development of on-chip learning based on memristor neural networks.

II. EXPERIMENTAL

The devices were fabricated in the following process. Firstly, Ti/Pt (3nm/50nm) were deposited on a SiO_2/Si substrate by e-beam evaporation with Ti as an adhesion layer. Subsequently, 7nm HfO_2 and 5nm Al_2O_3 dielectric layer were deposited by atomic layer deposition (ALD) at 250°C using Tetrakis (ethylmethylamido) hafnium (TEMAH) as the Hf source, H_2O as the oxygen source, and Trimethylaluminum ($Al(CH_3)_3$) as the Al source. The photoresist (AZ-5214) was spin-coated on the dielectric layer and heated at 95°C, followed by photolithography. The Ti/Pt (45nm/50nm) film was deposited on the dielectric layer by electron beam evaporation, and then the lift-off process was performed to form the top electrode. Finally, an Agilent B1500A semiconductor device analyzer with bottom electrode (BE) grounded and top electrode (TE) biased was used to test the electrical characteristics.

III. RESULTS AND DISCUSSION

A. DC CHARACTERISTIC

The *I-V* curves of a typical bipolar switching for the Pt/HfO_2/Al_2O_3/Ti device are shown in Figure 1(a-b). The device can be switched from a high resistance state (HRS) to a low resistance state (LRS) at 0.65V with analogue switching features, and a −1 V sweeping voltage is required to switch the device back to HRS. During 1000 repetitive tests, the set/reset voltages and the resistance ratio barely changed. It shows the excellent cyclic repeatability of the device. In Figure 1(c), the multi-level storage characteristics of the device can be observed by controlling the compliance current during the set process. What's more, under 0.1V read voltage, the ten selected resistance states can keep for 10^4 s time at 85°C, as shown in Figure 1(d). The high reliability of the memristors can well support the online-learning in the SNN.

B. COMSOL MODEL

According to the Gauss theorem of parallel plate capacitors, the electric field is mainly concentrated in the low-k layer [20]. In the Pt/HfO_2/Al_2O_3/Ti laminated device, since the dielectric constant of Al_2O_3 is much smaller than that of HfO_2, the fracture and generation of conductive filaments

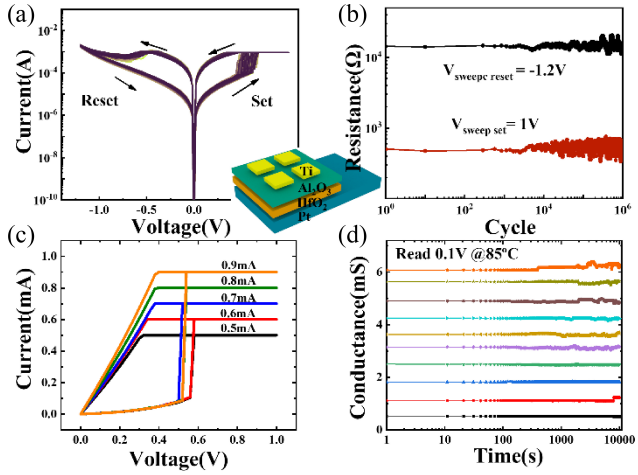

FIGURE 1. (a) The I-V characteristics of Pt/HfO_2/Al_2O_3/Ti devices in 1000 continuous DC sweeps. (b) Endurance characteristics of the device under the 1V and -1.2V write and erase voltages operation in ambient conditions. (c) The multi-resistance state test of the device is achieved by changing the compliant currents. (d) Long-term retention characteristic test of 10 average selection states under 85°C.

mainly occur in the Al_2O_3 layer. Compared with the monolayer devices, the stability of this device can be improved. The COMSOL Multiphysics software is used to construct an electrothermal coupling model to demonstrate the switching mechanism of the device. Figure 2(a) shows the establishment of a two-dimensional axisymmetric geometric structure, in which the thickness of HfO_2 (7nm) /Al_2O_3(5nm). The simulation, which is started immediately after the reset process, features a continuous conductive filament (CF) that connects the top and bottom electrodes. The set and reset processes are described through V_o migration induced by the local electric field and temperature due to Joule heating. Therefore, a drift/diffusion continuity equation ($\frac{\partial n_D}{\partial t} = \nabla\cdot(Dn_D - vn_D)$) for *Vo* transport, a current continuity equation for electrical conduction ($\nabla\cdot\sigma\nabla\varphi = 0$), and a Fourier equation for Joule heating ($-\nabla\cdot k_{th}\nabla T = J\cdot E = \sigma|\varphi|^2$) are solved in the COMSOL to simulate the switching mechanism of the three partial differential equations (PDEs) [21], [22]. The comparison between simulation and experimental data is shown in Figure 2(b). Figure 2(c) shows the various stages changes of oxygen vacancies and potentials in the device's set process. A positive voltage is applied to the device during the set process. Joule heat causes the temperature of the device to rise. At the same time, the concentration of oxygen vacancies in the Al_2O_3 layer increases, which in turn causes the electric field at the gap to decrease. When the voltage reaches 0.65V, the CF layer is formed, and the device changes to low resistance. At this time, the electric field at CF is uniformly distributed. In general, the device can be used in neuromorphic calculations with multi-value storage.

C. SYNAPTIC SIMULATION

Long-term potentiation (LTP) and long-term depression (LTD) are the crucial features of electronic synapses in

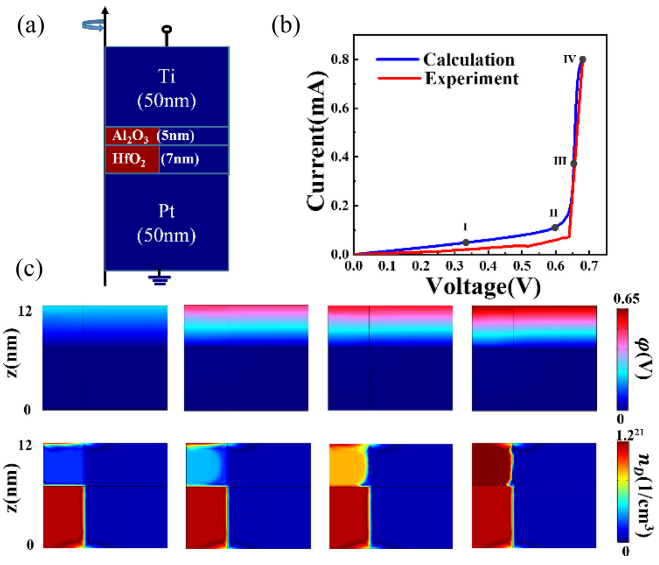

FIGURE 2. **(a) The structure of the Pt/HfO_2/Al_2O_3/Ti device used in the COMSOL simulation model. (b) *I-V* characteristic curves under positive sweep voltage in simulation and experiment. (c) Calculate the graph of the potential φ and the dopant concentration *Nd* during the set process in (b).**

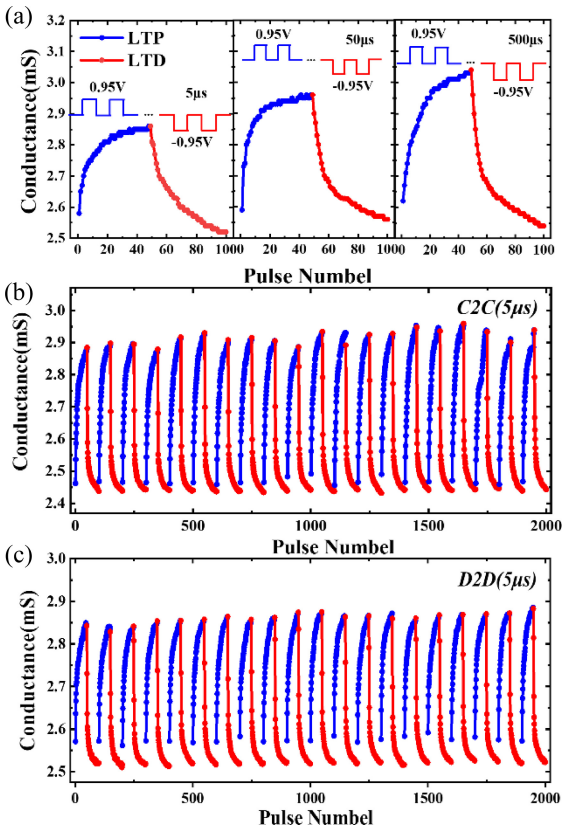

FIGURE 3. **Long-term synaptic plasticity of the devices with various pulse widths under different pulse widths stimuli. (a) LTP with 0.95V and LTD with -0.95 V, the pulse width is fixed at 5μs, 50μs and 500μs, respectively. (b) Cycle to cycle (C2C) characteristics of LTP and LTD of the synaptic device. (c) Device to device (D2D) characteristics of LTP and LTD of the synaptic device.**

neuromorphic computing systems, which can be used in real-time coding and image recognition and *in-situ* corrections of network weights [23], [24]. To demonstrate the synaptic properties of LTP and LTD, the impulse response characteristics of the device are tested, as shown in Figure 3(a-b). The conductance weight of the device can be changed gradually stimulated at different pulse widths (5μs,50μs,500μs). When the sequential positive write pulses (0.95V) biased on the presynaptic terminal of the artificial synapse, the post-synaptic currents would increase exponentially. Inversely, the post-synaptic currents can be continuously degraded under sequential negative write pulses (-0.95V) stimuli. During the whole process, the read pulse amplitude 0.1V. In addition, the post-synaptic current changes faster as the pulse width increases. Applying a string of constant-amplitude pulses to devices is the process of forming and breaking the conductive filaments. Therefore, the larger the pulse used to the device, the more conductive wires are formed or broken, which results in higher enhancing or inhibiting behaviors of the synaptic devices [25], [26]. The consistency of the electronic synapse is verified by applying continuous pulses to the one device repeatedly. The results show that the range of conductance obtained by pulse number modulation is stable, which ensures that the conduction of the memristor arrays can be modulated by the number of pulses, as shown in Figure 3(b). In addition, Figure 3(c) shows the device - to - device variation, which is also important for memristor arrays.

Spike timing dependent plasticity (STDP) is the key learning mechanisms in biological synapses. Specifically, the synapse weight of the device is updated according to the time difference between the peak value the post-neuron and the pre-neuron ($\delta_t = t_{post} - t_{pre}$). When the time of the post-synaptic pulse is earlier than the pre-synaptic, it is recorded as $\delta_t > 0$. In addition, when the time of the pre-synaptic pulse is earlier than the post-pulse, it can be expressed as $\delta_t < 0$. In this work, the 10μs -wide pulse voltage is applied to the pre and post synapse. As is shown in Fig. 4, the Pt/HfO_2/Al_2O_3/Ti synapse can stimulate the STDP successively for a given voltage. It can be seen that the weight will increases as δ_t increases ($\delta_t > 0$) and the weight decreases as δ_t decreases ($\delta_t < 0$).

D. SPIKE NEURAL NETWORK

STDP is an essential learning rule for SNN [27], [28]. However, it is an unsupervised training algorithm which limited the network structure. At present, there have been many methods to sovle the problem of STDP, we proposed a multi-layer STDP training method based on Multi-ReSuMe and the synapsis characteristics of memristor to train a two-layer fully connected network to classify handwritten digits, which does not require the classifiers used in standard STDP. Meanwhile, the algorithm can decline the amount of pulses used to tune the conduction of devices, which facilitates the application of memristors.

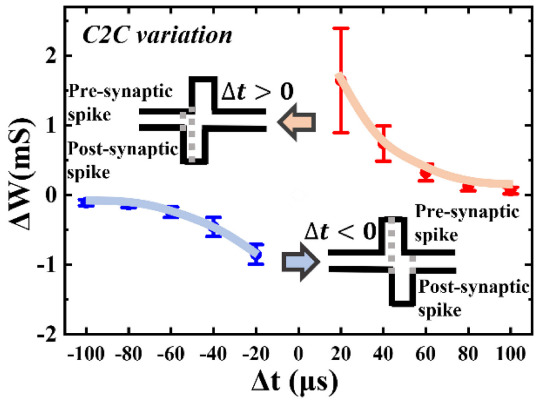

FIGURE 4. The C2C characteristics of the STDP behaviors of the devices. (the line represents the range of the test value, and the circle represents the median value).

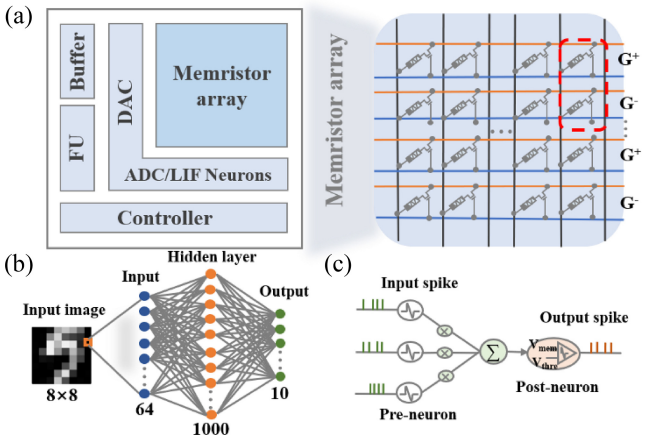

FIGURE 5. (a) Structure of SNN based on synapse arrays in simulation. (b) Two-layer SNN network. (c) A neural network composed of post-neurons driven by input pre-neurons. The pre-neuronal spikes, V_i is adjusted by the synaptic weight, W_i to produce a resultant at a given time $\sum_i V_i \times W_i$ (equivalent to dot-product operation). The resulting current affects the membrane potential of post-neuron. When V_{mem} exceeds the threshold, post-neurons will generate a pulse, and V_{thre} will have a refractory period after the spike is generated.

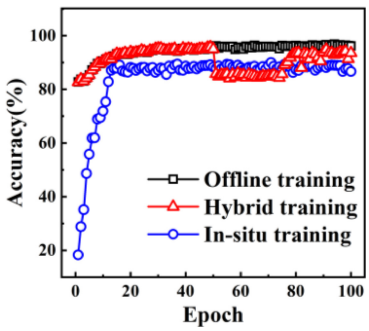

FIGURE 6. Comparison of the accuracy of handwriting recognition between offline training, hybrid training and in-situ training.

In this paper, the learning method includes two parts. First, the differential *eq.* (1), (2) are used to describe the LTP and LTD characteristics of the memristor. The fitted curve with different pulse widths is shown in Figure 7 (a).

$$r_{n+1} = r_n + \dot{r} \tag{1}$$

$$\dot{r} = \frac{a * (b - c * r_n)^d}{(i + \exp(f * r_n + g))^h} \tag{2}$$

where r_n is the conductance at present, $\dot{r}$ represents the corresponding change of conductance, and r_{n+1} is the conductance at next moment. In addition, *a, b, c, d, i, f, g,* and *h*, the equation coefficients, these parameters have different values in LTP and LTD. Besides the nonlinear asymmetric curves, this function can also be used to fit common variations such as linear symmetric and nonlinear symmetric.

On the other hand, it is important to judge whether changes the weight. To complete the operation, we transform the multi-ReSuMe from *eq.* (3) to *eq.* (4) first to calculate the change of weight [29]:

$$dw_n = \int [S_d(t) - S_0(t)] \left[\int_0^{\infty} W(s) S_i(t-s) ds \right] dt \tag{3}$$

$$dC_n = dw_n + \alpha * \sum_{n-1} \mathrm{dw} \tag{4}$$

where, $W(\cdot)$ represents the STDP function and n is the times of weight modification. Combining *eq.* (2) and (4), the final weight change can be calculated as *eq.* (5).

$$r_{n+1} = r_n + f(dC_n) * \dot{r} \tag{5}$$

The $f(\cdot)$ is used to produce a pulse to change the weight, which can be described as *eq.* (6).

$$f(dC_n) = \begin{cases} 0 & dC_n < \theta \\ \mathrm{sgn}(dC_n) & dC_n > \theta \end{cases} \tag{6}$$

To verify the validity of our algorithm, a simple three-layer network is performed to UCI (University of California, Irvine). Note that, the images need to be converted to Poisson pre-spike trains based on the pixel intensity. The synaptic system architecture and mapping scheme in Figure 5 (a) are adopted. In the architecture shown in Figure 5(b), it contains 64, 1000 and 10 neurons in the input, the hidden and output layer, respectively. And all of the neurons are LIF (Leaky Integrate and Fire) model and the structure is shown in Figure 5(c) in detail. Subsequently, the influence on accuracy of the algorithm training method, asymmetric nonlinear weight update and synaptic variation measured from experiments are explored.

The SNN based on the memristor is built to simulate the off-training, in-situ training and the hybrid training. The weights in offline training are all floating Point, and the accuracy rate can finally reach 96% after 100 training epochs. For in-situ training, the conductance of each element in the memristor array is modulated only according to the conductance variation characteristics described in *eq.* (5) and the pulses generation scheme in *eq.* (6). Finally, after 100 epoch

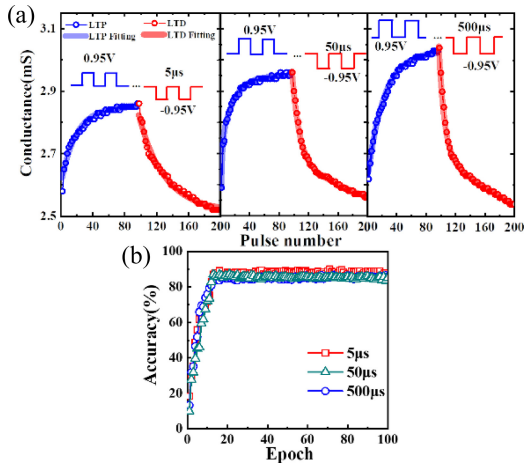

FIGURE 7. **(a) LTP and LTD fitting curve. (b) The different conductance variation trends are fitted by differential equation.**

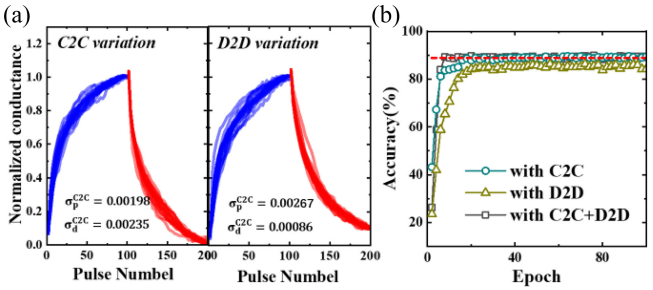

FIGURE 8. **(a) Conductance behavior of a Pt/HfO_2/Al_2O_3/Ti memristor during twenty cycles of 100 potentiation/depression voltage pulses and 20 cycles of 100 conductance states. The C2C variation (σC2C) and D2D variation (σD2D) are the mean standard deviation extracted from the experiment. The conductance is normalized to [0,1]. (b) Recognition accuracy with σC2C and σD2D Pt/HfO_2/Al_2O_3/Ti devices. Accuracy degrades significantly as D2D and C2C variation considered collectively, while D2D and C2C variation considered separately have trivial effects. (The dotted line shows the ideal in-situ accuracy).**

training, the network accuracy is more than 89%. Although, the accuracy is slightly lower than in offline training, it is still acceptable.

Obviously, it is necessary to train the network offline previously if the hybrid training method used. The final training results are shown in Figure 6. In hybrid training, the network is trained ex-situ in the previous 50 epochs. After that, the weights are quantized and mapped to the conductance of the memristors. Here, Gaussian noise is used to represent the uncertainty in the weight modulating process. Because of the noise and limited level of device conductance, the accuracy suddenly dropped to 85.77%. Then after 50 epochs of in-situ learning, the accuracy of the network becomes about 90%.

In order to explore the influence of nonlinear asymmetry on the network performance, the differential dynamics equations were used to fit the LTP and LTD of the three pulse widths of the device respectively. The final fitting results are shown in Figure 7(a). Different pulse widths affect the change trend of device conductance, so after 100 training epochs, the accuracy achieved by the network is also different, which are 85.05%, 85.59% and 86.63%, as shown in Figure 7(b).

Furthermore, the influence of synaptic variations is essential for the system performance. In general, there are two types of variation: a random distribution of conductance when the same operating voltages are applied to one device from C2C, and the conductance variation from device to device. Herein, in Pt/HfO_2/Al_2O_3/Ti devices, C2C variation is investigated by introducing conductance offset error when each update pulse is applied, and the influence of D2D variation is treated by fixing errors to the nonlinearity of each device, as shown in Figure 8(a). Then, the C2C and D2D variation are applied into the weight update in the SNN network, respectively. As shown in Figure 8(b), compared with ideal devices, the accuracy is not decreased as considering these two variations, respectively. However, the accuracy will decrease 5% when the two variations are both considered. As shown in the above results, the SNN network shows remarkable high tolerance to variation. This work can pave the way to develop SNN brain chips based on memristor arrays.

IV. CONCLUSION

In this work, the SNN bionic system based on Pt/HfO_2/Al_2O_3/Ti device is constructed. We used the differential equation to describe the synaptic behavior of the device and update the weights according to the present state. Besides, we propose a scheme that can reduce the complexity of the peripheral circuit by modulating the conductance with only one pulse at a time. Subsequently, non-ideal devices with and network training methods are explored. According to the results, the non-ideal factors does not cause a significant decrease in accuracy and the hybrid training has higher accuracy compared with online training. The differential equation presented in this work shows the potential in avoiding non-ideal features. This work could promote the development of biomimetic spiking neural network chips based on memristors.

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