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Monolithically Integrated Polysilicon/Oxide-Semiconductor Hybrid Thin-Film Transistors for Advanced Sensing

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ABSTRACT This work reports an ingenious hybrid thin-film transistor (TFT) process platform that allows monolithic integration of poly-Si and oxide-semiconductor (OS) TFT-based circuits using three-mask processes. The effectiveness of the proposed fabrication approach is demonstrated by a hybrid poly-Si/indium-gallium-zinc oxide (IGZO) TFT cell, in which source/drain (S/D) contacts of poly-Si TFTs were simultaneously formed during the fabrication of IGZO TFTs. A thin Ti layer is intentionally inserted between poly-Si and IGZO channels in order to improve the contact resistivity of the n^+ poly-Si/IGZO structure. The integrated poly-Si/IGZO TFT cells exhibit sharp transition slopes ($\sim$ –35 mV/dec) in the transfer curves. With this feature, the sensitivity of the proposed hybrid TFT cells is greatly improved in comparison to individual IGZO TFTs, as evidenced in the detection measurements of NO_2 gas.

INDEX TERMS Poly-Si, IGZO, oxide semiconductor, thin-film transistors, sensor.

I. INTRODUCTION

Among the possible material choices for channels of thin-film transistors (TFTs), polysilicon (poly-Si), and oxide-semiconductor (OS, *e.g.*, indium-gallium-zinc oxide, IGZO)) are particularly attractive for displays [1] and sensing applications [2], [3]. Low-temperature polysilicon (LTPS) TFTs are a venerable technology thanks to their superior mobility (50$\sim$200 $cm^2/V{\cdot}s$), good stability, and capability of CMOS integration [4] [5]. On the other hand, IGZO TFTs exhibit not only decent channel mobility and excellent uniformity in electrical characteristics but also extremely off-state leakage owing to the high bandgap of the OS material [6], [7]. Promising potentials for sensing [2], [3] and memory [8], [9], [10] applications have already been demonstrated by using both poly-Si and OS TFTs. Therefore, the integration of specifically designed, hybrid TFTs in a circuit unit is envisaged to boost the overall performance of application-specific integrated circuits (ASICs) and related products. A well-known example is the low-temperature polycrystalline oxide (LTPO) TFT backplane technology developed by Apple [11], enabling significant improvements in power consumption and refresh rate while retaining the driving capability. TFTs are typically fabricated on substrates other than Si wafers and demand much lower process temperatures than the manufacturing of conventional Si MOSFETs. In this regard, it is crucial to develop a feasible fabrication scheme that effectively facilitates the integration of hybrid TFTs and simplifies the overall procedure in order to broaden the spectrum of TFT emerging applications. Recently, we proposed an ingenious hybrid TFT platform for fabricating an integrated poly-Si/IGZO TFT unit [12]. Our proposed hybrid TFT approach provides the core building block for emerging biosensor cells that is analogous to the previously-reported co-integration of Si nanowires biosensors and n-MOSFETs on an SOI wafer [13]. It is important to note that our proposed scheme needs only three

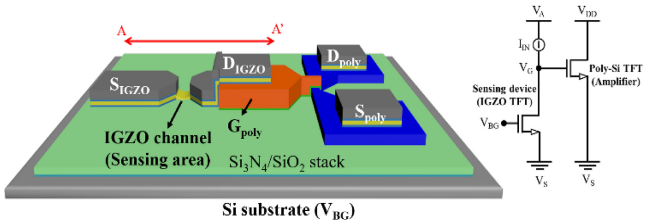

FIGURE 1. **A bird's-eye view of the hybrid poly-Si/IGZO TFT cell and the equivalent circuits. For simplicity, the suspended bridge hung over the IGZO channel is not shown.**

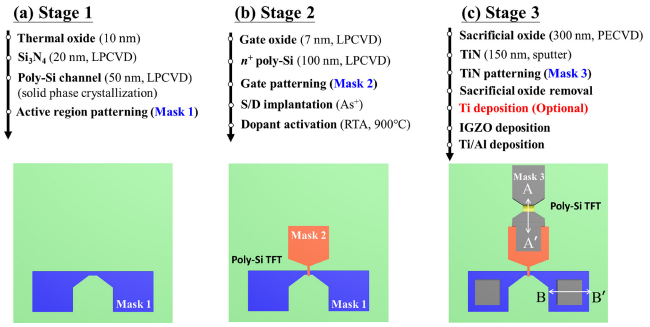

FIGURE 2. **Process flow and corresponding mask layouts for the fabrication of hybrid poly-Si/IGZO TFT cell: (a) Formation of the active region of the poly-Si channel, (b) patterning of the gate of the poly-Si TFT, and (c) fabrication of FPE IGZO TFT. In (c), S/D contact holes in the poly-Si TFT were also open to simplifying the overall fabrication.**

masks, greatly simplifying the entire fabrication process as compared with previous works on the integration of poly-Si and IGZO TFTs which demand at least five masks for the complete fabrication [11], [14], [15], [16], [17]. In this paper, detailed information about the design, fabrication, and process integration of the hybrid TFT cell is disclosed. Preliminary experimental results on the sensing of low-concentration NO_2 are also reported.

II. HYBRID POLY-SI/IGZO TFT CELL AND FABRICATION

Schematic diagrams of our proposed hybrid poly-Si/IGZO TFT cell along with the corresponding equivalent circuit are illustrated in Fig. 1. IGZO TFTs formed by using a novel film-profile engineering (FPE) scheme are used as sensing devices [18], whereas the detected signals are amplified by poly-Si TFTs with their top gates being connected to the drain of the bottom-gated IGZO TFT. The appealing advantage of FPE TFTs lies in the so-formed concave channel [18], within which an ultra-thin central channel makes the sensing device very sensitive to the change in the concentration of detected species contained within the ambient.

Figure 2 outlines the key process flow for producing hybrid TFTs, which needs only three mask processes to complete the device fabrication. We started with the deposition of a 10 nm-thick SiO_2 and a 20 nm-thick Si_3N_4 on a 6-in. *p*-type Si wafer using low-pressure chemical vapor deposition (LPCVD). Next, a 50 nm-thick undoped amorphous Si (a-Si) layer was deposited using LPCVD, followed by a solid-state crystallization (SPC) treatment at 600 °C for 24 hours to transform it into poly-Si. The mean grain size of the SPC poly-Si is about 20 nm. After the lithographic patterning of the channel region (Fig. 2(a)), gate-stacking layers of a 7 nm-thick SiO_2 and a 100 nm-thick n^+ poly-Si were sequentially deposited using LPCVD. Subsequently, lithographical and etching steps were performed to pattern the top gate of poly-Si TFTs (Fig. 2(b)) with a channel length (L) varying from 0.4 μm to 5 μm and fixed widths (W) of 10 μm. Next, source/drain (S/D) implantation (As^+) and rapid thermal annealing (RTA) activation (900 °C, 10 s) were conducted to complete the poly-Si TFT fabrication.

The following process steps involve the integration of IGZO TFTs in the cell (Fig. 2(c)), which was effectively implemented by a specifically designed FPE approach proposed by our group [18] for fabricating the OS-channel TFTs. The basic core of the FPE scheme relies upon a suspended TiN bridge hanging over the channel of the TFT, as shown in Fig. 3(a), which serves as a shadow mask for the subsequent depositions enabling the formation of a concave IGZO channel and discrete S/D metal layers. The desirable profile is achievable by selecting suitable deposition tools in combination with adjusting appropriate process conditions. The process steps for integrating FPE IGZO TFTs with poly-Si TFTs are detailed as follows. First, a 300 nm-thick SiO_2 and a 150 nm-thick TiN were deposited on top of the Si wafer using PECVD and sputtering, respectively. Next, the top TiN layer was patterned to form the S/D fan-out areas (Fig. 2(c)), followed by selectively etching the underlying SiO_2 layer in a diluted buffered oxide etch (BOE) solution to make the TiN overhanging bridge between the source and drain (Fig. 3(a)). In this step, the selective etching of SiO_2 over Si_3N_4 using BOE is effectively achieved owing to the high etch selectivity. An IGZO TFT was completely produced following the deposition of IGZO and metal (Ti/Al) S/D contacts using reactive sputtering and evaporation, respectively, as shown in Fig. 2(c) [18]. To simplify the process steps as well as to save the mask count, the contact holes of S/D for poly-Si TFTs were also opened during the formation of the suspended TiN bridge. Note in Fig. 2(c) that the 7 nm-thick gate-oxide layer deposited over the S/D regions of poly-Si TFTs was simultaneously removed away during the etching of the sacrificial oxide layer as mentioned above. After that, the n^+ poly-Si S/D regions were exposed in the contact holes while the top TiN layer overhung at the edge of the contact hole owing to the lateral etching of the oxide, as shown in Fig. 3(b). Similar to the TiN suspended bridge in the IGZO TFT area, the TiN overhang shadows the subsequent deposition of the IGZO/metal layers, forming a discrete n^+ poly-Si/IGZO/metal stack in the contact areas of S/D of the poly-Si TFT. It is important to note that to improve the contact resistivity of the n^+ poly-Si/IGZO stack at the S/D regions, we optionally deposited a 10 nm-thick Ti insertion layer before the deposition of the IGZO channel and top metal.

Typical optical microscope (OM) examination on fabricated hybrid poly-Si/IGZO TFTs was shown in Fig. 4. The poly-Si TFT located on the right side of Fig. 4 (as denoted

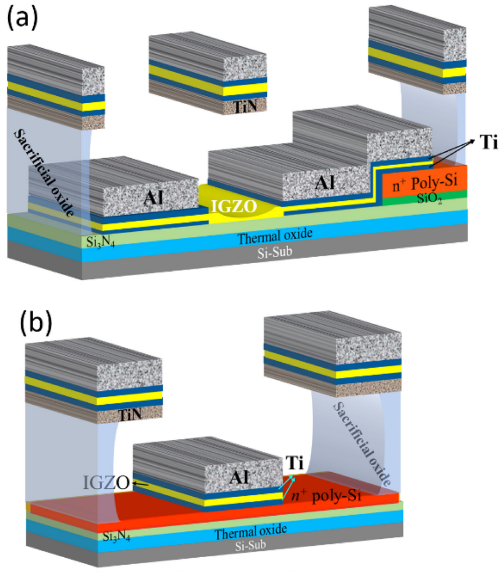

FIGURE 3. Cross-sectional schematic diagram of (a) IGZO TFT (A-A′ line in Fig. 2) and (b) S/D contacts of poly-Si TFT (B-B′ line in Fig. 2).

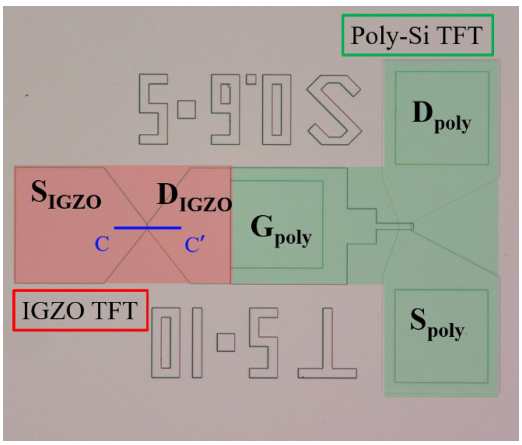

FIGURE 4. Top-view OM image of a fabricated poly-Si/IGZO TFT cell.

by the green region) serves as a signal amplifier, whereas the red region on the left side indicates the IGZO TFT whose IGZO recess channel predominates the sensing function. As mentioned above, the IGZO TFT's drain electrode connects to the gate of the poly-Si TFT. Figure 5(a) shows the cross-sectional transmission electron microscope (TEM) micrograph of fabricated FPE IGZO TFTs. The ultimate stack layers of Si_3N_4/SiO_2 following the aforementioned top-oxide etching serve as the gate dielectric of the bottom-gated TFTs. Owing to the shadow effect of the suspended TiN bridge, the thickness of the IGZO channel at the channel center (Fig. 5(b)) is much thinner than that deposited over the S/D regions (Fig. 5(c)).

III. RESULTS AND DISCUSSION

A. CHARACTERISTICS OF POLY-SI TFTS

Figure 6 compares the transfer characteristics of poly-Si TFTs with channel lengths ranging from 0.4 μm to

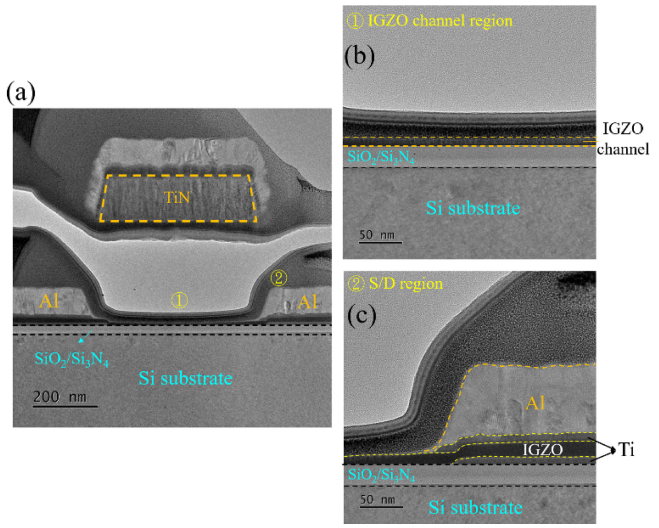

FIGURE 5. (a) Cross-sectional TEM image of a fabricated FPE IGZO TFT, and the enlarged views at (b) channel center and (c) drain.

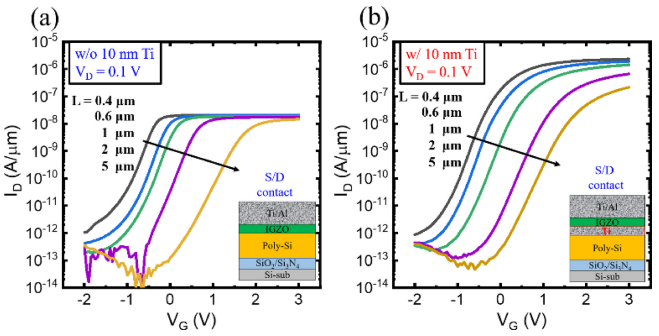

FIGURE 6. Transfer characteristics of poly-Si TFTs of various L. The S/D contacts are (a) without and (b) with the optional Ti between IGZO and n^+ poly-Si. The channel width of the tested devices is 10 μm.

5 μm in combination with various S/D contact structures. It is clearly seen in Fig. 6 that the threshold voltage (V_{TH}) decreases while subthreshold swing (SS) tends to improve with decreasing L, which are attributable to short-channel and drain-induced-grain-barrier-lowering (DIGBL) effects [19], [20]. Previous reports [21], [22] have pointed out that the DIGBL effect tends to reduce the effective defect density in the poly-Si channel as L is shortened, and thus improves SS at short channels. Another important and impactful finding of the notes is the influence of the S/D contacts. Figure 6(a) shows that independent of the channel length (L), all of the studied TFTs without the deliberately inserted Ti layer between IGZO and n^+ poly-Si in S/D contacts exhibit anomalously low on-state current (I_{ON}) pinned at approximate 2×10^{-8} A/μm. In contrast, the insertion of a 10 nm-thick Ti layer significantly improves I_{ON} which is much enhanced by decreasing L as shown in Fig. 6(b). Obviously, the improvement in I_{ON} by inserting the Ti layer between IGZO and n^+ poly-Si in S/D contacts is ascribed to a reduction in S/D series resistance (R_{SD}), which has been extracted using the total resistance method [23]. Figure 7 shows that extracted R_{SD} values for TFTs with

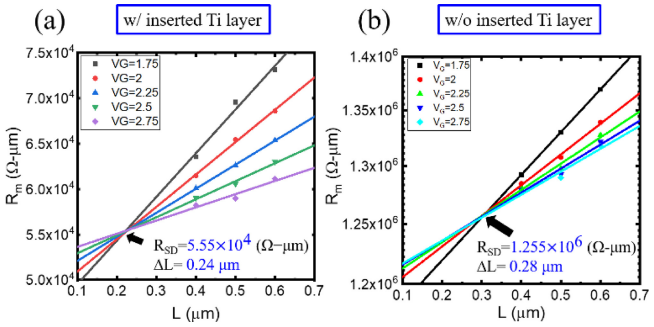

FIGURE 7. Extraction of R_{SD} from poly-Si TFTs (a) with and (b) without Ti insertion layer based on the scheme proposed in [20]. The extracted ΔL, which accounts for the sum of the diffusion lengths from the source and drain edges into the channel after the activation step, is 0.24 μm in (a) and 0.28 μm in (b).

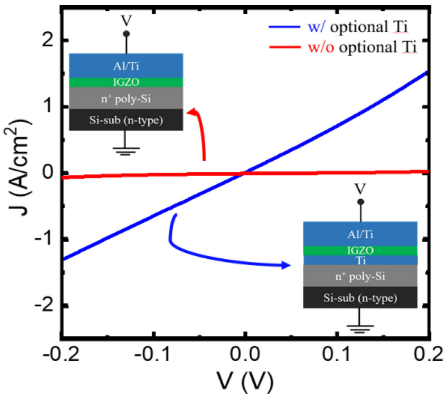

FIGURE 8. J-V characteristics of diodes with junction structures identical to the S/D contact of poly-Si TFTs with and without the Ti-inserted layer.

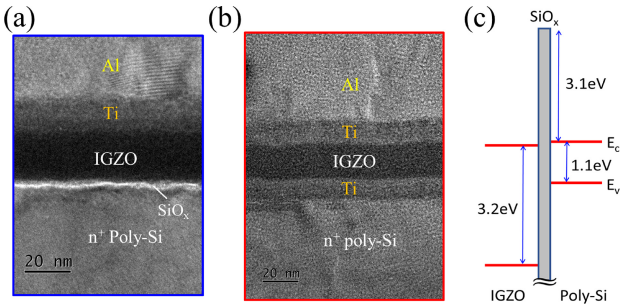

FIGURE 9. TEM images the S/D contacts of poly-Si TFTs (a) without and (b) with the Ti insertion layer. (c) The interfacial SiO_x layer between the poly-Si and IGZO in (a) acts as a barrier that impedes carrier transport and increases contact resistance.

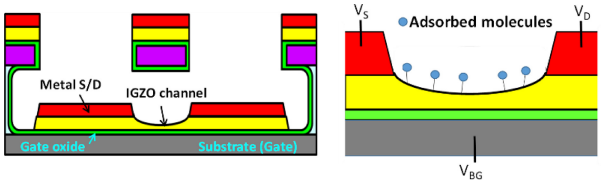

FIGURE 10. (a) Cross-sectional view of an FPE IGZO TFT with Si substrate as the bottom gate [18]. (b) Enlarged view of the channel center in the FPE device. The channel potential is sensitive to the number of charges brought by the adsorbed molecules. The ultra-thin (<10 nm) concave IGZO channel formed with sputtering deposition [18] makes the device suitable for sensing applications.

and without the Ti insertion layer are 5.55×10^4 Ω-μm and 1.26×10^6 Ω-μm, respectively.

To gain more insight, we further fabricated diodes with a structure identical to both stack structures (with and without Ti insertion layers) in the S/D contacts as mentioned above. The junction area of fabricated diodes was intentionally designed to be the same as that of the contact area of 80×80 μm^2 in the fabricated TFTs so that we are able to directly examine the electrical properties of the contacts. Typical I-V characteristics of fabricated diodes are shown in Fig. 8. Contact resistivity values extracted from the differential slope of *I-V* curves at zero bias ($V = 0$) are 8.7 $\Omega - cm^2$ and 0.15 $\Omega - cm^2$, respectively, for the diodes without and with the insertion layers of Ti between n^+ poly-Si and IGZO. The results in Fig. 8 unambiguously confirm that the anomalously high R_{SD} for the n^+ poly-Si/IGZO contact stack is due to the high contact resistance. Besides, TEM examination further reveals that the origin of the high contact resistance of n^+ poly-Si/IGZO structure is due to the presence of an interfacial SiO_x layer between n^+ poly-Si and IGZO as shown in Fig. 9(a). On the other hand, the insertion of a 10 nm-thick Ti layer effectively suppresses the formation of the interfacial oxide layer as shown in Fig. 9(b), which is attributed to the oxygen-scavenging effect of Ti [24] and thus, the contact resistivity and R_{SD} are reduced significantly.

The impact of the co-integration of IGZO TFTs on the performance and uniformity of poly-Si TFTs has also been studied [12]. The results evidence good uniformity in I-V characteristics among fabricated poly-Si TFTs and the effectiveness of the inserting Ti layer in retaining I_{ON} and SS of the devices even after the integration of IGZO TFTs.

B. CHARACTERISTICS OF IGZO TFTS

Fig. 10 shows the structures of IGZO TFTs fabricated using the FPE approach. The suspended bridge hung over the center of the TFTs (Fig. 10(a)) serves as a shadow mask, and thus the sputtered IGZO channel becomes thinner toward the channel center [18]. This also suggests that the central channel thickness decreases with increasing L. Note that the channel potential is more vulnerable to the adsorbed charging species as the channel becomes thinner.

Transfer characteristics of FPE IGZO TFTs with *L* ranging from 0.4 μm to 0.6 μm are shown in Fig. 11. The V_{TH} appears to increase with increasing L. The observed trend agrees well with the results reported in the previous work [18], [25], [26] and is mainly caused by the reduction in the channel thickness of IGZO for FPE-TFTs stated above as L becomes longer. As the oxide semiconductors studied in these works are *n*-type materials, the thicker the channel is, the larger the density of free electrons per gated area in the channel is. Therefore, a more negative gate voltage is required to fully deplete a thicker IGZO channel. The gate leakages (I_G) for studied TFTs are also plotted in

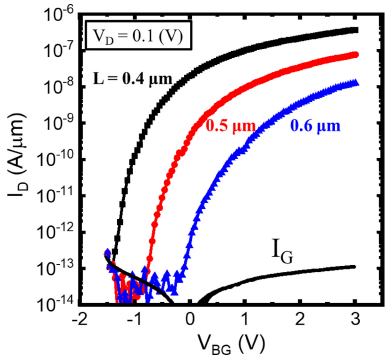

FIGURE 11. Transfer characteristics and gate leakage currents (I_G) of fabricated IGZO TFTs with different *L*. The channel width of the tested devices is 5 μm.

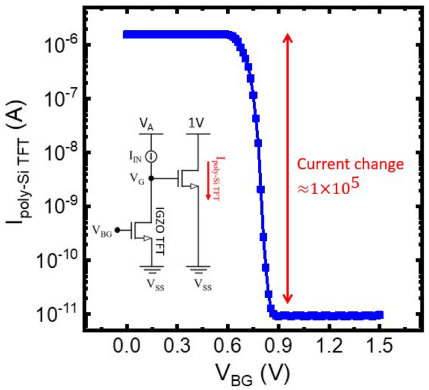

FIGURE 12. Typical transfer characteristics of a fabricated sensing cell.

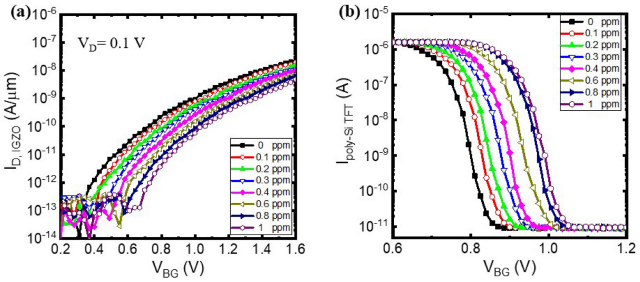

FIGURE 13. (a) Transfer characteristics of an IGZO TFT (L/W = 0.6/5 μm/μm) under various NO_2 concentrations (0.1 ~ 1 ppm). (b) Drain current of the poly-Si TFT (L/W = 5/10 μm/μm) in a hybrid sensor under various NO_2 concentrations as a function of V_{BG}.

Fig. 11 and appear to be independent of L. This indicates that I_G flows mainly through the gate-to-S/D overlapped areas. Fortunately, it is not large and affects the operation of TFTs. It is also clearly seen in Fig. 11 that the subthreshold swing (SS) of TFTs slightly increases with increasing *L*. A similar observation was reported recently and was attributed to the increase in the defect density of the IGZO channel with decreasing channel thickness [26].

C. CHARACTERISTICS OF POLY-SI/IGZO TFT CELL

Figure. 12 presents typical operating characteristics of fabricated hybrid poly-Si/IGZO TFT sensing cell with $L = 0.6$ μm for the IGZO TFT and $L = 5$ μm for the poly-Si TFT. During electrical measurement, the current source (I_{IN}) was set at 100 pA with a compliance V_G of 2V. The current of the poly-Si TFT ($I_{poly\text{-}Si\ TFT}$) as a function of V_{BG} is shown in Fig. 12. The IGZO TFT is turned off when V_{BG} is less than its V_{TH} and thus, $I_{poly\text{-}Si\ TFT}$ retains at a high-value level (1.4×10^{-6} A) as the V_G node is limited at 2V due to an extremely low channel conductance of the IGZO TFT. As V_{BG} increases to turn the IGZO TFT on, a dramatic increase in the channel conductance results in an efficient discharge of I_{IN}. Consequently, V_G quickly decreases to a low level, leading to an abrupt drop in $I_{poly\text{-}Si\ TFT}$ [13]. The characteristics of a considerable current change ($\approx10^5$) and steep swing slope (~ –35 mV/dec) evidence the promising potential of our proposed scheme for sensing applications.

D. NO_2 SENSING PERFORMANCE

Some of the fabricated devices have been employed for detecting NO_2 gas with concentrations less than 1 ppm. Fig. 13(a) and Fig. 13(b) show the transfer characteristics of an individual IGZO TFT and a hybrid TFT cell, respectively, obtained from the measurements when exposed to a NO_2 ambient. It is clearly seen that the transfer curves have positive and nearly parallel shifts with increasing NO_2 concentration. This is because when NO_2 concentration increases, more NO_2^- species tend to adsorb on the surface of the exposed IGZO channel (Fig. 10(b)) [27], resulting in an increase in the V_{TH} of the IGZO TFT as shown in Fig. 13 (a). This leads to a positive shift in the transfer curves of the hybrid TFT cell shown in Fig. 13(b) as well. To illustrate the effectiveness of the sensing structures, the ratio of current change (I/I_0 for the hybrid TFT cell and I_0/I for the IGZO TFT) as a function of NO_2 concentration is shown in Fig. 14. I_0 denotes the current measured at a specific V_{BG} (*i.e.*, 0.86V in Fig. 13(a) and Fig. 13(b)) in the transfer regime when NO_2 concentration is zero, while *I* is the current recorded at the same V_{BG} when NO_2 of various concentrations is introduced. The current of the IGZO TFT measured at the same V_{BG} tends to decrease as NO_2 concentration increases owing to a positive SS. In contrast, a negative swing slope of the transfer curve of the hybrid TFT cell causes *I* to rise with increasing NO_2 concentration. In addition, thanks to a much steeper swing slope, the current change ratios obtained from a hybrid TFT cell are much larger than those from an individual TFT. Fig. 14 shows that a current change ratio as high as 10^5 is achievable when the hybrid TFT cell is subjected to 1 ppm NO_2 exposure, which is approximately 1000 times higher than that of its IGZO TFT counterpart. Moreover, extensive data measured from different sets of testers confirm the good reproducibility of hybrid TFT sensors.

Fig. 15 shows the real-time measurement results of NO_2 sensing. with the concentration of NO_2 gas increasing sequentially from 0 to 0.1 ppm, 0.2 ppm, 0.3 ppm, 0.6 ppm,

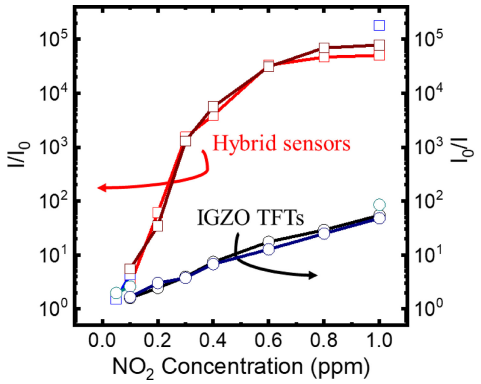

FIGURE 14. Current change ratios measured from hybrid TFT cells (square symbol) and IGZO TFTs (circle symbol) as a function of NO_2 concentration.

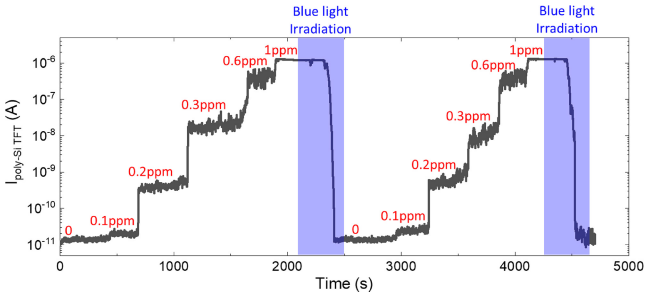

FIGURE 15. Real-time NO_2 sensing using the sensing cell. Blue light irradiation is able to restore the current to the initial condition.

and 1 ppm. It can be observed that the detection current increases with the rise in concentration, and the current remains relatively stable at each concentration level. Even after evacuating the residual NO_2 gas from the measurement chamber, the current remains unaffected, indicating strong adhesion of NO_2^- on the IGZO surface [27]. Our experiments also involved exposing the sensing cell to light sources of different wavelengths. We found that red and green lights did not affect the current. In contrast, as shown in Fig. 15, blue light with a wavelength of 457 nm could cause the attached NO_2^- to detach after a period of illumination, causing the current to drop and return to its initial value before NO_2 gas was introduced. Subsequently, repeating the procedure of sequentially increasing the concentration of NO_2 gas reproduces the results observed in the first phase (0∼2000 sec). A few previous reports [28], [29] have shown that the blue light with an energy of ∼2.7 eV is sufficient to generate holes inside the IGZO channel. The holes can then facilitate releasing the attached NO_2^- species from the IGZO surface [27], and thus the sensing can recover to its initial state.

IV. CONCLUSION

In this work, we proposed a unique hybrid TFT process platform and successfully demonstrated a basic unit consisting of a poly-Si TFT and an IGZO TFT for sensing applications. The overall fabrication is greatly simplified in a distinctive three-mask approach and facilitated by simultaneously forming the S/D contacts of poly-Si TFTs during the fabrication of the FPE IGZO TFT. In this proposed process scheme, an additional 10-nm thick Ti layer inserted between poly-Si and IGZO in the S/D contacts of poly-Si TFTs effectively reduces the high contact resistance. Our integrated poly-Si/IGZO TFT cells exhibit sharp transition slopes (∼ –35 mV/dec), enabling a highly promoted detection sensitivity as evidenced in the NO_2 gas sensing experiments. The results showcase the feasibility of this approach for advanced sensing applications.

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