3-D Self-Aligned Stacked Ge Nanowire pGAAFET on Si nFinFET of Single Gate CFET

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ABSTRACT In this study, we propose a self-aligned stacked Ge nanowire (NW) p-type gate-all-around field-effect transistor (pGAAFET) on Si nFinFET of single gate complementary FET (CFET). The self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET device is fabricated on a SOI wafer. The CFET device is fully compatible with current Si technology platform using alternating anisotropic and isotropic dry etching process. The Ge NW pGAAFET presents an on-state current (I_{ON}) of 166 μA/μm at $V_D = V_G$-$V_{TH} = -0.5$ V and shows minimum subthreshold swing (SS_{min}) of 79, 91 mV/dec, and I_{ON}/I_{OFF} of 3.03×10^5, 3.4×10^4 at $V_D = -0.05$ V and -0.5 V, respectively. The Si nFinFET presents an I_{ON} of 60.4 μA/μm at $V_D = V_G$-$V_{TH} = 0.5$ V and shows SS_{min} of 91, 101 mV/dec, and I_{ON}/I_{OFF} of 9.01×10^4, 5.62×10^5 at $V_D = 0.05$ V and 0.5 V, respectively. The proposed CFET can simplify the process and shows promising potential for extending scaling beyond the technology node.

INDEX TERMS Self-aligned, Ge nanowire (NW), Si FinFET, complementary FET (CFET), single gate.

I. INTRODUCTION

Fin field-effect transistor (FinFET) [1], [2], [3], gate-all-around (GAA) nanowire (NW) FET [4], [5], [6], [7], [8], and nanosheet (NS) FET [9], [10], [11] have been proposed for the continuous scaling down of CMOS with superior electrostatics and device performance. Currently, the structure of complementary FET (CFET) with stacked pFET and nFET can further reduce the layout area and meet the demand of performance beyond 3-nm node (N3) [12]. However, using homogeneous Si channel CFETs suffer lower on-state current (I_{ON}) of pFET [13], [14], [15].

Ge is a promising channel material owing to its high carrier mobility. Heterogeneous CFETs with high-hole-mobility Ge as pFET and Si as nFET could overcome the symmetric issues of I_{ON}. For the heterogeneous channel materials, dual work function metals [13] and wafer bonding method [16] are used to achieve symmetric threshold voltage (V_{TH}). Dual work function metal gate process is a challenge for shrinking gate length (L_G) because the top device requires the

additional replacement of work function metal. Wafer bonding method might increase the cost of Silicon-on-insulator (SOI) wafers owing to the separated pFET and nFET process. Hence, the single gate CFET is the key to address the aforementioned issues due to the simplified fabrication process and alignment complexity. On the other hand, the fabrication process of Ge MOSFETs should be kept at low temperature to suppress dopant diffusion and avoid the generation of interfacial defects. Thus, microwave annealing (MWA) with low thermal budget was used to activate the dopant in the source and drain (S/D) regions [17]. Low-temperature MWA utilizes microwave radiation with longer wavelengths to penetrate atoms directly, thereby inducing lattice vibrations and facilitating uniform heating throughout the material.

Therefore, we demonstrated a fabrication method of single gate CEFT of crystalline Ge (c-Ge) as pFET and c-Si as nFET in this study. We also performed a Sentaurus 3D TCAD simulation [18] to investigate the symmetric characteristics
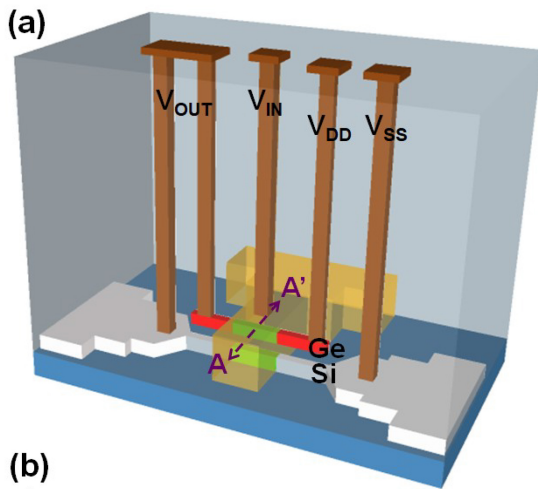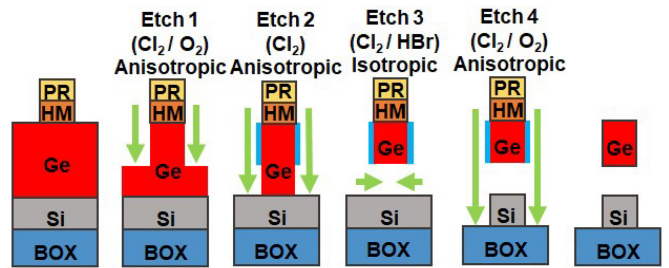
FIGURE 1. (a) A 3-D schematic diagram of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET device. **(b)** Process flow of the CFET device.

FIGURE 2. Etching sequence for the Ge NW on Si Fin. After hard mask (SiO_2) etching, anisotropic and isotropic etching were performed.

FIGURE 3. SEM image of Ge NW on Si Fin after dry etching process.
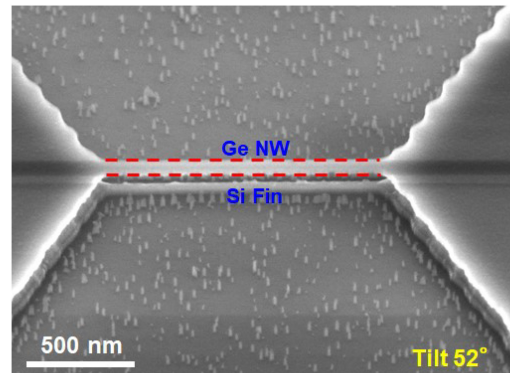
and performance of the CFET device with a suitable metal work function and undoped channels.

II. DEVICE FABRICATION

Fig. 1(a) shows the schematic diagram of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET. Fig. 1(b) illustrates the process flow. The devices were fabricated on an 80-nm-thick Ge epitaxial growth on a SOI wafer. The Ge layer was grown on the monocrystalline Si layer with (100) surface orientation through ASM Epsilon 2000 low-pressure chemical vapor deposition (LPCVD) system. After LPCVD epitaxy, SiO_2 as hard mask was deposited by plasma-enhanced chemical vapor deposition (PECVD). The active regions of Ge NW on Si Fin were fabricated through e-beam lithography (EBL) and reactive-ion etching (RIE). Fig. 2 shows the schematic top-down etching sequence for the vertically stacked Ge NW on Si Fin formation. In Etch 1, after hard mask opening, the anisotropic etching with Cl_2/O_2 gases was applied to form the straight Ge sidewall. Following, an O_2 plasma step was carried out

forming germanium oxide on Ge surface, which provides a protection for the subsequent isotropic etching. In etch 2, the anisotropic etching with Cl_2 was performed to etch down the Ge. Next, Etch 3 was performed with Cl_2 and HBr gases for isotropic etching to form the top Ge NW. Finally, anisotropic etching was repeatedly performed to form the Si Fin in Etch 4.

Fig. 3 shows the scanning electron microscope (SEM) image (tilt angle of 52°) of top Ge NW without bending under an appropriate fabrication process. The chemical cleaning process was performed with HCl and diluted HF, then the *in-situ* ozone treatment in a standard atomic layer deposition (ALD) system at 390 °C was carried out forming an interfacial layer (IL), followed by high-k dielectric of Al_2O_3 deposition through ALD. Next, a stacked 30-nm-thick TaN (bottom)/60-nm-thick TiN (top) as single gate electrode was deposited by physical vapor deposition (PVD). The 30-nm-thick TaN is the work function metal in the CFET device and the 60-nm-thick TiN is used to reduce contact resistance. After single gate patterning, a 20-nm-thick Al_2O_3 layer deposited through ALD was used to prevent Ge NW bending from subsequent etching process. The upper Ge was then implanted with ^{11}B ions (1E15 cm^{-2} dosage at 10 keV) for p-type Ge S/D regions. Following that, a 20-nm-thick SiO_2 was deposited by PECVD. Then, the Ge S/D regions were necessary to be partially removed for bottom Si S/D regions implantation. Ge layer on Si can be easily etched with good selectivity using a H_2O_2 solution. Following Ge
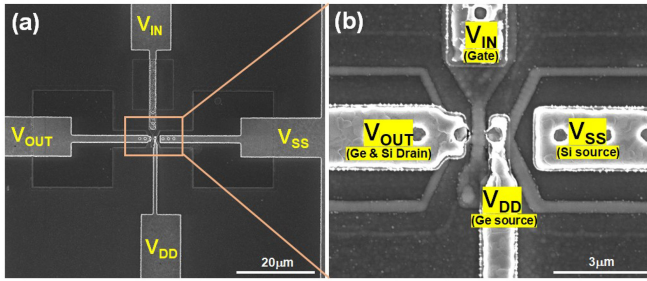
FIGURE 4. (a) SEM and (b) zoom-in images of the CFET device with V_{IN}, V_{OUT}, V_{DD}, and V_{SS}.
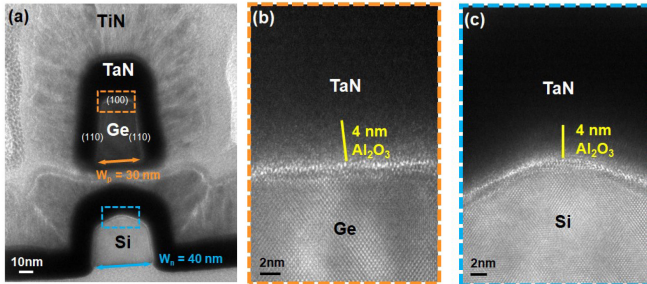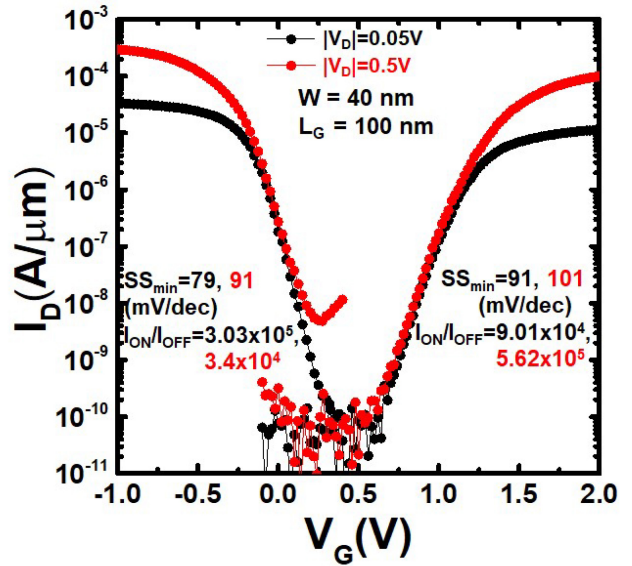

FIGURE 5. (a) Cross-section TEM image and (b)-(c) enlarged images of the gate stack of Ge and Si. (d)-(h) EDS mapping of the distribution of elements: Ge, Si, Al, Ti, and Ta.

FIGURE 6. I_D-V_G characteristics of the Ge NW pGAAFET and Si nFinFET at $|V_D| = 0.05$ V and 0.5 V.

S/D regions partially removed, ion implantation was performed with ^{31}P ions (1E15 cm^{-2} dosage at 10 keV) for n-type Si S/D regions. Low-temperature MWA was applied with 1650 W for 100 seconds to simultaneously activate the dopants in Ge and Si S/D regions. Finally, PECVD SiO_2 was deposited as a passivation layer, contact holes were defined, followed by metallization processes. Fig. 4(a) and (b) display the top-view and zoom-in SEM images of the CFET device with separate contacts of V_{IN}, V_{OUT}, V_{DD}, and V_{SS}.

III. RESULTS AND DISCUSSION

Fig. 5(a) presents the cross-sectional transmission electron microscopy (TEM) image of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET device matching Fig. 1(a) A-A' with a width of pGAAFET (W_p) of 30 nm and a width of nFinFET (W_n) of 40 nm. The sidewalls of Ge are (110) surface orientation. Fig. 5(b) and (c) show the enlarged images of the gate stack with TaN/Al_2O_3/Ge and TaN/Al_2O_3/Si, respectively. Fig. 5(d)–(h) show the energy

dispersive spectroscopy (EDS) elements mapping of Ge, Si, Al, Ti, and Ta distributions.

Fig. 6 shows the I_D-V_G characteristics of the Ge NW pGAAFET and Si nFinFET with gate length (L_G) of 100 nm at $|V_D| = 0.05$ V and 0.5 V, respectively. The Ge NW pGAAFET presents (1) $I_{ON} = 1.66 \times 10^{-4}$ A/μm at $V_D = V_G$-$V_{TH} = -0.5$ V, (2) minimum subthreshold swing (SS_{min}) = 79, 91 mV/dec, and (3) $I_{ON}/I_{OFF} = 3.03 \times 10^5$, 3.4×10^4 at $V_D = -0.05$ V and -0.5V, respectively. The Si nFinFET presents (1) $I_{ON} = 6.04 \times 10^{-5}$ A/μm at $V_D = V_G$-$V_{TH} = 0.5$ V, (2) $SS_{min} = 91$, 101 mV/dec, and (3) $I_{ON}/I_{OFF} = 9.01 \times 10^4$, 5.62×10^5 at $V_D = 0.05$ V and 0.5 V, respectively. The drain current is normalized by the largest channel width of 40 nm among the stacked channels.

Fig. 7 shows the I_D-V_D characteristics of the Ge NW pGAAFET and the Si nFinFET measured from $|V_G$-$V_{TH}| = 0$ to 0.8 V. The Ge NW pGAAFET has significant enhancement of I_{ON} because the (110) surfaces of the Ge NW sidewalls exhibit higher hole mobility [19]. Table 1 presents the comparison of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET with previous self-aligned CFET reports. The I_{ON} of the Ge NW pGAAFET has improvement. Although the I_{ON} of the Si nFinFET in this study is lower, its I_{ON} may be improved by adjusting the structure and size of the Si nFinFET.

Due to the limitation of our laboratory equipment, TaN gate metal was selected in our experiment with the most appropriate work function. However, TaN still could not adjust the symmetric V_{TH} between Ge NW pGAAFET and Si nFinFET. The Ge NW pGAAFET and Si nFinFET are symmetric around $V_G = 0.4$ V. Using Al incorporation into the TiN layer could reduce the effective work function [20].
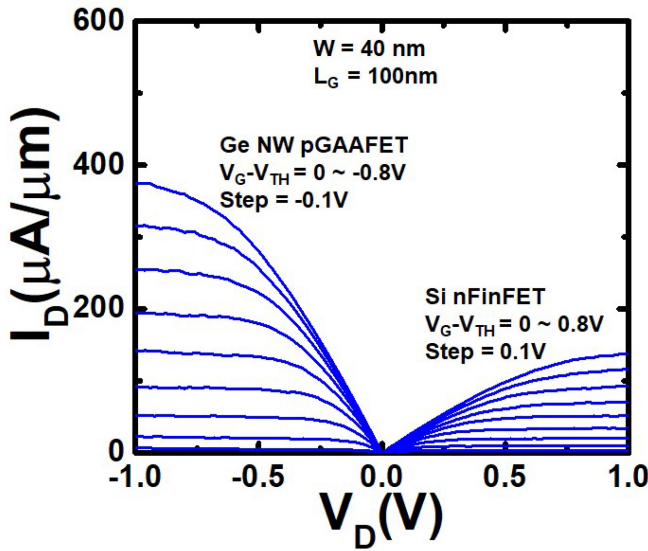
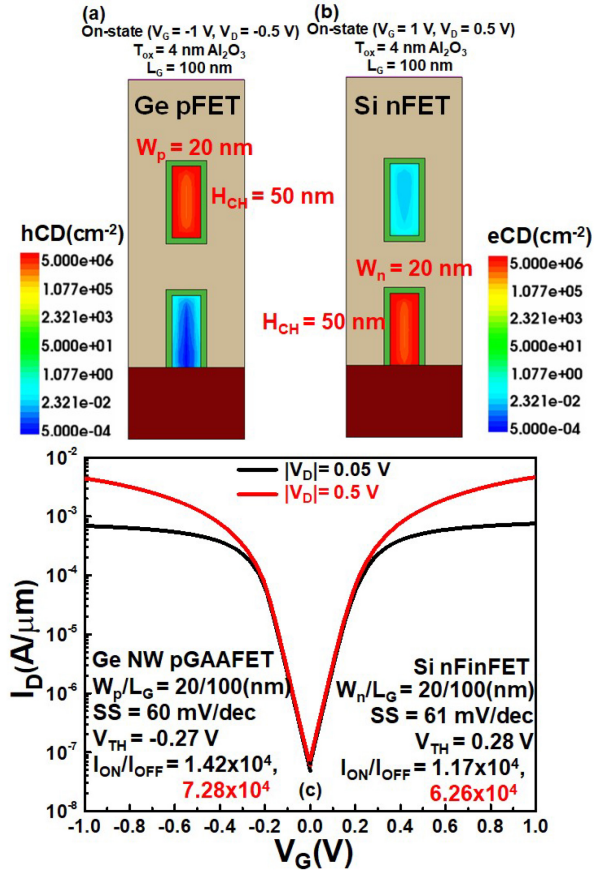**FIGURE 7.** I_D-V_D characteristics of the Ge NW pGAAFET and Si nFinFET at $|V_G$-$V_{TH}| = 0 \sim 0.8$ V.

TABLE 1. Comparison with previous self-aligned CFETs.

		This work	[13]	[14]	[15]
Method		Self-aligned CFET	Self-aligned CFET	Self-aligned CFET	Self-aligned CFET
Single metal shared gate		Yes	No	Yes	Yes
Top device		Ge NW pMOS	Si 2NRs nMOS	Si NS nMOS	Si JL NS pMOS
Bottom device		Si Fin nMOS	Si 3NRs pMOS	Si Fin pMOS	Si JL NS nMOS
Channel material		Single crystal Si and Ge	Single crystal Si	Single crystal Si	Amorphous Si
L_G (nm)		100	75	20	150
SS (mV/dec)	pFET	79 @V_D= -0.05V	65 @V_D= -0.65V	>100 @V_D= -0.8V	62 @V_D= -0.1V
	nFET	91 @V_D= 0.05V	69 @V_D= 0.65V	>100 @V_D= 0.8V	62 @V_D= 0.1V
I_{ON} (μA/μm)	pFET	166 @V_D=V_G-V_{TH}= -0.5V	180 @V_D=V_G-V_{TH}= -0.65V	~3 @V_D=V_G= -0.8V	~5 @V_D=V_G-V_{TH}= -1V
	nFET	60.4 @V_D=V_G-V_{TH}= 0.5V	406 @V_D=V_G-V_{TH}= 0.65V	~30 @V_D=V_G= 0.8V	~5 @V_D=V_G-V_{TH}= 1V

FIGURE 8. (a) hCD and (b) eCD of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET at On-state ($|V_G| = 1$ V, $|V_D| = 0.5$ V). (c) I_D-V_G characteristics of the Ge NW pGAAFET and the Si nFinFET by 3D TCAD simulation at $|V_D| = 0.05$ V and 0.5 V.

Therefore, the V_{TH} of Ge NW pGAAFET and Si nFinFET might be more symmetric. Although the symmetric V_{TH} and I_{ON} were not obtained in this work, the fabrication method of the single gate CFET is demonstrated. Thus, we used the 3D TCAD simulation with a proper metal work function of 4.38 eV to prove the performance of this proposed structure of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET.

IV. SIMULATION
The simulating parameters of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET is designed based on our fabricated device. It includes channel width of Ge NW pGAAFET ($W_p = 20$ nm), channel width of Si nFinFET ($W_n = 20$ nm), gate length ($L_G = 100$ nm), channel height ($H_{CH} = 50$ nm), gate oxide thickness ($T_{ox} = 4$-nm-thick Al_2O_3), Ge and Si S/D regions doping concentration ($N_{S/D} = 1 \times 10^{20}$ cm^{-3}), Ge channel doping

concentration ($N_{CH, Ge} = 8 \times 10^{16}$ cm^{-3}, undoped channel), and Si channel doping concentration ($N_{CH, Si} = 1.6 \times 10^{15}$ cm^{-3}, undoped channel). The following physical models were considered in the simulation: (1) the drift-diffusion model, (2) the density gradient model, (3) the doping-concentration-dependent Shockley–Read–Hall (SRH) recombination model, (4) the transverse field dependence, and high-field saturation mobility models, (5) the Slotboom bandgap narrowing model, and (6) the ballistic mobility model.

Fig. 8(a) and (b) show the simulated hole current density (hCD) and electron current density (eCD) of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET with an appropriate metal work function of 4.38 eV at On-state ($|V_G| = 1$ V and $|V_D| = 0.5$ V), respectively. Fig. 8(c) shows the simulated I_D-V_G curves of the Ge NW pGAAFET and Si nFinFET, which show ideal SS values and achieve the symmetric $|V_{TH}| = 0.27$ V and 0.28 V. Fig. 9(a) shows the simulated voltage transfer characteristic (VTC) of the CFET device under various supply voltages (V_{DD}) of 0.5 V, 0.75 V, and 1 V. The symmetric VTC curves were achieved due to the matching I_{ON} and V_{TH}. Fig. 9(b)
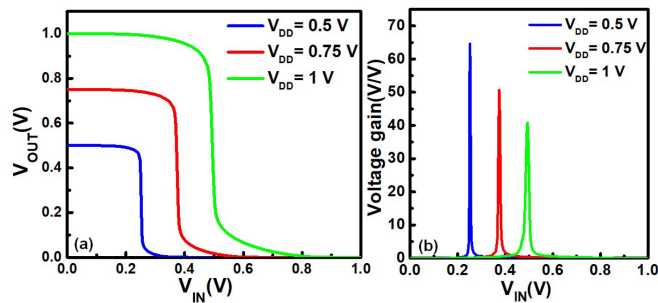
FIGURE 9. Simulated (a) VTC and (b) voltage gains of the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET at V_{DD} = 0.5 V, 0.75 V, and 1 V.

depicts that the higher peak voltage gain of 64.6 V/V can be obtained at lower V_{DD} = 0.5 V. Therefore, it is essential to find an appropriate metal work function value for symmetric V_{TH} and I_{ON} for heterogeneous channel materials of single gate CFET.

V. CONCLUSION

A method to fabricate the self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET is proposed and demonstrated using simple top-down dry etching techniques that are compatible with current CMOS platform. The Ge NW pGAAFET exhibits a higher I_{ON} of 166 µA/µm. This self-aligned stacked Ge NW pGAAFET on Si nFinFET of single gate CFET exhibits a simplified fabrication process and provides a promising transistor architecture to continue Moore's law scaling towards N2 and beyond.

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