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Effectiveness of *c*-Axis Aligned Crystalline IGZO FET as Selector Element and Ferroelectric Capacitor Scaling of 1T1C FeRAM

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ABSTRACT Aiming to reduce the area of a ferroelectric random access memory (FeRAM), we fabricated an FeRAM having a 1T1C configuration by using a *c*-axis aligned crystalline In-Ga-Zn-O field-effect transistor, which we call OSFET, with a high breakdown voltage. A combination of the OSFET with L/W of 60 nm/60 nm and a single damascene ferroelectric capacitor (FE-Cap) attained FE-Cap area reduction to 0.06 μm^2 per cell. The FeRAM achieved a write time of 10 ns, a rewriting endurance of 10^9 cycles, and a data retention time of 100 min at 85°C. The OSFET is an optimal selector element for emerging memories.

INDEX TERMS *C*-axis aligned crystalline In-Ga-Zn-O (CAAC-IGZO), 1T1C, FeRAM, single damascene.

I. INTRODUCTION

Memories are required to have higher performance, e.g., higher-speed operation, higher density, and higher endurance [1]. For such high performance, ferroelectric random access memory (FeRAM) is currently a subject of active research [2], [3], [4], [5]. Hf-based materials are promising ferroelectric materials for FeRAMs because films of the Hf-based materials can be thinner than those of lead zirconate titanate (PZT). However, FeRAMs have a problem of a high operating voltage of approximately 3 MV/cm [6]. In addition, memories must have a high density, and it is necessary to increase breakdown voltages and density of selector elements in the FeRAMs. A *c*-axis aligned crystalline In-Ga-Zn-O (CAAC-IGZO) field-effect transistor (FET), which we call OSFET, has attracted attention as a transistor that can be monolithically stacked over a SiFET [7]. The CAAC-IGZO has a wider band gap than Si [8]; thus, the OSFET has a high breakdown voltage. In addition, the OSFET has a feature of a low off-state current [9] and is suitable for memories. On the other hand, the applications of the OSFETs not only to displays but also to memories and image sensors have been proposed [10], [11]. In particular, memories combined with ferroelectrics have been increasingly reported [12]. In view of the above, we fabricated and evaluated an OS FeRAM using a scaled OSFET and a ferroelectric capacitor (FE-Cap). To confirm that both a high breakdown voltage and a high density are achieved with the OSFETs, the OSFET with a scaled channel length was subjected to breakdown voltage evaluation. To prevent leakage at the edge of the capacitor, the FE-Cap whose bottom electrode does not have a step at the edge was examined, and fine patterns for the FE-Cap were formed. The evaluation results of the OS FeRAM combining the OSFET and the single damascene FE-Cap demonstrate that the OSFET is a promising selector element for emerging memories. This paper is the extension of the previous paper [13] and focuses on the effectiveness of the OSFET as a selector element and the scalable FE-Cap. Additionally, this paper provides the

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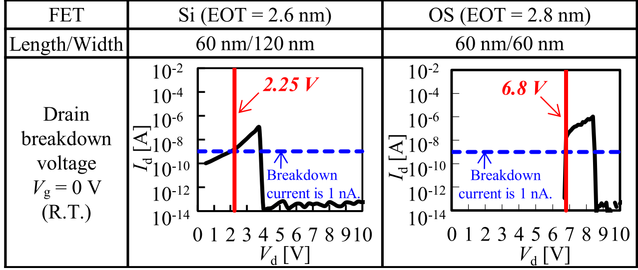
TABLE 1. Comparison of drain breakdown voltages between OSFET and SiFET.



FET	Si (EOT = 2.6 nm)	OS (EOT = 2.8 nm)
Length/Width	60 nm/120 nm	60 nm/60 nm
Drain breakdown voltage $V_g = 0$ V (R.T.)	2.25 V; Breakdown current is 1 nA. (I_d [A] vs. V_d [V])	6.8 V; Breakdown current is 1 nA. (I_d [A] vs. V_d [V])

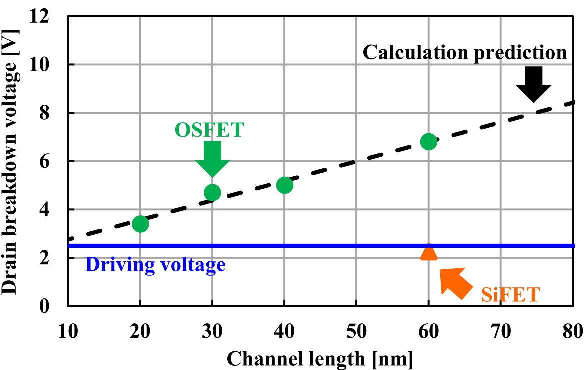


FIGURE 1. **Drain breakdown voltages of OSFETs with different channel lengths.**

updated evaluation results of the OS FeRAM of the previous paper [13].

II. CHARACTERISTICS OF COMPONENTS

A. BREAKDOWN VOLTAGES OF OSFET AND SIFET

To confirm that the OSFET is effective as a selector element, the drain breakdown voltages of the SiFET and the OSFET were measured under the conditions where V_g was 0 V, drain-source voltage V_d was from 0 V to 10 V, and the measurement temperature was room temperature. TABLE 1 shows the evaluation results of the drain breakdown voltages. As in TABLE 1, the SiFET has *L*/*W* of 60 nm/120 nm and the OSFET has *L*/*W* of 60 nm/60 nm, that is, both FETs have the same *L*.

According to the results in TABLE 1, the drain breakdown voltages of the SiFET and the OSFET are 2.25 V and 6.8 V, respectively. This means that the OSFET has a higher breakdown voltage than the SiFET and is thus less likely to be broken. Hence, a 1T1C FeRAM fabricated using the OSFET can withstand high-voltage driving, has a smaller size than a memory including the SiFET, and has a high density. In this study, we fabricated the 1T1C OS FeRAM using the OSFET with *L*/*W* of 60 nm/60 nm. For further scaling and higher density of the FeRAM in the future, whether the OSFET has a high breakdown voltage even with *L* smaller than 60 nm should be confirmed. Thus, the drain breakdown voltages of OSFETs with *L* of 20 nm, 30 nm, 40 nm, and 60 nm were measured under the same conditions as those in TABLE 1. The results in Fig. 1 reveal that the OSFET with *L* of 20 nm still has a higher breakdown voltage than the SiFET. From the prediction of the drain breakdown voltage of an OSFET with *L* smaller than 20 nm based on the measurement results, it is found that an adequate breakdown voltage is feasible at a driving voltage of 2.5 V. This raises an expectation of higher-speed operation with further area reduction.

B. CHARACTERISTICS EVALUATION WITH DIFFERENT FE-CAP AREAS

A 10-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film was selected as a ferroelectric material, and test element groups (TEGs) with different FE-Cap areas were evaluated. Specifically, the TEGs with three FE-Cap areas, a 94.97 μm^2 FE-Cap, 1024 parallel-connected FE-Caps each of which has an area of 0.06 μm^2, and 1024 parallel-connected FE-Caps each

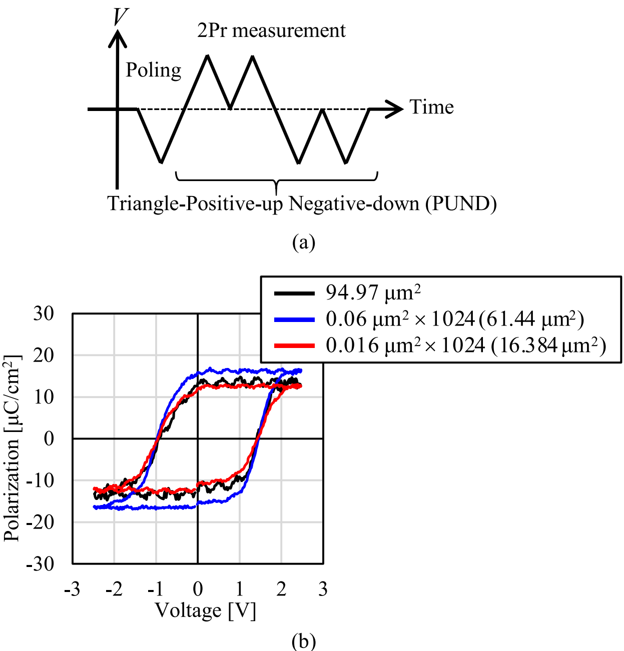


FIGURE 2. **(a) Input waveform (PUND) in *P*–*V* measurement, (b) *P*–*V* curve for each FE-Cap area.**

of which has an area of 0.016 μm^2, were evaluated. The small-area FE-Caps were connected in parallel to increase the capacitance for measurement with high signal to noise ratio. Figure 2 presents the polarization–voltage (*P*–*V*) curves of the TEGs with different FE-Cap areas. The field intensity was 2.5 MV/cm and the measurement frequency was 1 kHz. The results in Fig. 2 demonstrate that polarization is observed regardless of the FE-Cap area. The TEG with an FE-Cap area of 0.016 $\mu m^2 \times 1024$ has smaller 2Pr than the other TEGs; however, it is found that the ferroelectricity of the HZO film is not lost by scaling of the unit area of the FE-Cap. This indicates that further scaling is possible in the future.

Next, the rewriting endurance of the TEGs with different FE-Cap areas was evaluated. Positive up negative down measurement was performed under the conditions where the

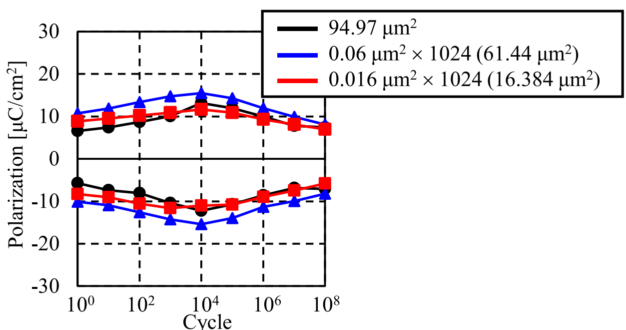


FIGURE 3. Endurance for each FE-Cap area.

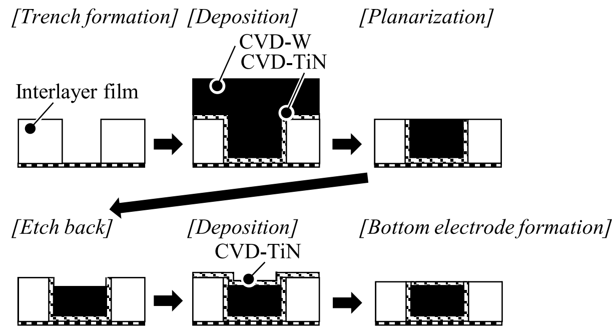


FIGURE 4. Process flowchart for single damascene bottom electrode.

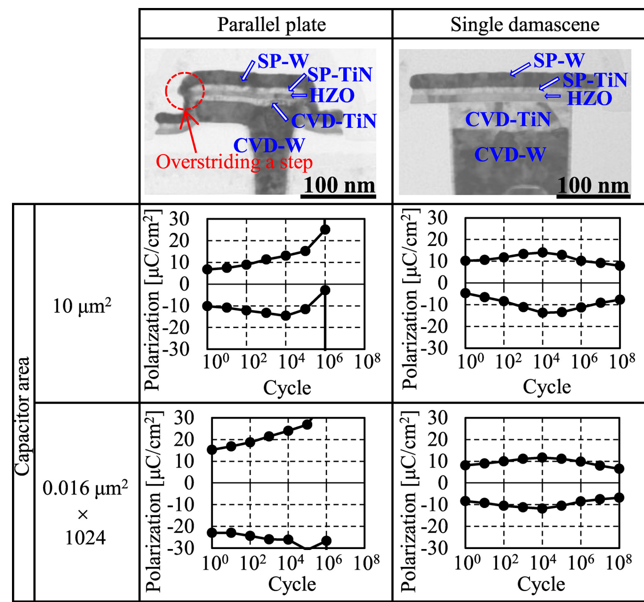
field intensity was 2.5 MV/cm, the endurance frequency was 100 kHz, the measurement frequency was 1 kHz, and the maximum number of cycles was 10^8. The FE-Cap areas were 94.97 μm^2, 0.06 $\mu m^2 \times 1024$, and 0.016 $\mu m^2 \times 1024$. Figure 3 shows the rewriting endurance results, indicating that adequate 2Pr is obtained until 10^8 cycles regardless of the FE-Cap area.

C. FE-CAP STRUCTURE AND CHARACTERISTICS

Figure 4 is a flowchart for a single damascene process. First, an opening is formed in an interlayer film and filled with a TiN film and a W film, and the TiN and W films are planarized by chemical mechanical polishing (CMP). After that, the W film is slightly etched back, and then a TiN film is embedded and planarized by CMP to form a bottom electrode. As shown in Fig. 4, the single damascene bottom electrode allows an HZO film to be formed flat thereover and thus a step is not formed on the bottom electrode, thereby eliminating leakage due to a short-circuit between the bottom electrode and the top electrode.

An FE-Cap with a metal-ferroelectric-metal structure is described. TABLE 2 shows cross-sectional images and rewriting endurance test results of a parallel plate FE-Cap and the single damascene FE-Cap. The rewriting endurance test was performed under the conditions where the field intensity was 2.5 MV/cm, the endurance frequency was 100 kHz, and the measurement frequency was 100 Hz. The FE-Caps each of which includes the electrode formed using a TiN film and has either of two area conditions of 10 μm^2 and 0.016 $\mu m^2 \times 1024$. The single damascene FE-Cap has

TABLE 2. Cross-sectional images and rewriting endurance test results of parallel plate FE-Cap and single damascene FE-Cap.



a rewriting endurance of 10^8 cycles even with a scaled area of 0.016 $\mu m^2 \times 1024$ as well as an area of 10 μm^2, whereas the parallel plate FE-Cap has a rewriting endurance of less than 10^6 cycles with both areas of 10 μm^2 and 0.016 $\mu m^2 \times 1024$. These results demonstrate a large difference in rewriting endurance between the single damascene FE-Cap and the parallel plate FE-Cap. This is probably because leakage at the edge of the capacitor due to the step is not caused in the single damascene FE-Cap. The single damascene FE-Cap can be formed through a back end of line (BEOL) along with the OSFET, which will contribute to capacitor area reduction and higher density of capacitors in the FeRAM.

III. OS FERAM DEVICE FABRICATION AND CHARACTERIZATION

A. DEVICE FABRICATION METHOD

The fabrication method and structure of the fabricated device are described. Figure 5 is a process flowchart for the OS FeRAM.

As shown in Fig. 5, first, a back gate is formed and a CAAC-IGZO is deposited. After that, source and drain electrodes and a top gate are formed. The bottom electrode of the FE-Cap is formed using TiN through a single damascene process. Then, a ferroelectric HZO layer is formed, followed by TiN deposition for the top electrode and rapid thermal annealing at 450°C. All the processes are performed at 450°C or lower, and the FE-Cap is formed in the BEOL process of the OSFET. Figure 6 is a cross-sectional image of the fabricated OS FeRAM. In Fig. 6, the OSFET has L/W of 60 nm/60 nm and the area of the bottom electrode (TiN) of the FE-Cap is 0.016 μm^2; thus, the scaled OSFET and FE-Cap are successfully formed.

Process Flowchart for OS FeRAM

OSFET
- Base film deposition
- Back gate electrode deposition (Threshold voltage control)
- Back gate insulator deposition
- CAAC-IGZO deposition
- S/D electrode deposition and island formation
- Trench formation (Etching of S/D electrode)
- Top gate insulator deposition
- Top gate electrode deposition and planarization

FE-Cap
- Single damascene formation
- Bottom electrode (TiN) deposition and planarization
- 10-nm-thick HZO deposition
- Top electrode (TiN) deposition
- Rapid thermal annealing (RTA) at 450°C
- Formation of passivation layer, inter layer, via, and wiring

FIGURE 5. Process flowchart for single damascene bottom electrode.

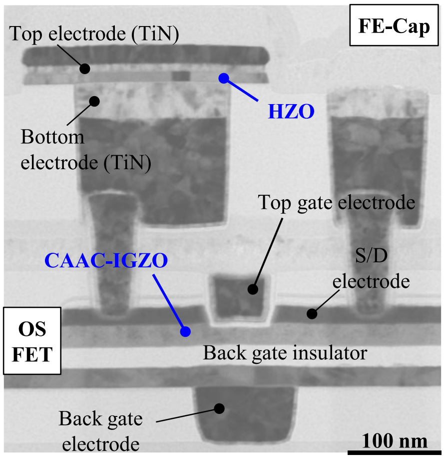


FIGURE 6. Cross section of OSFET and FE-Cap

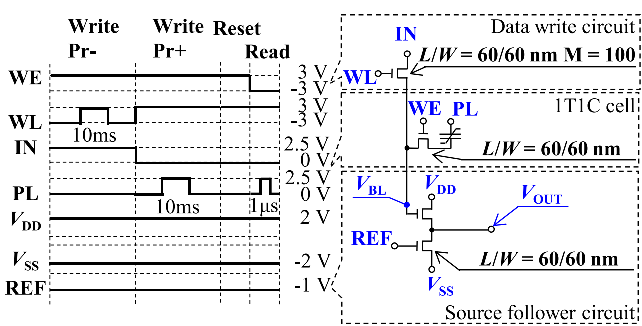


FIGURE 7. Timing chart for writing of Pr− and Pr+ in this order and circuit diagram of 1-bit OS FeRAM TEG.

B. 1-BIT OS FERAM TEG

We fabricated the 1-bit OS FeRAM TEG using the scaled OSFET with a high breakdown voltage and the single damascene FE-Cap, which were formed at a process temperature of 450°C or lower, and characterized. The OSFET in the OS FeRAM TEG has *L/W* of 60 nm/60 nm. Figure 7 shows a timing chart and a circuit diagram for the evaluation of the OS FeRAM TEG. The OS FeRAM has a simple configuration including a data write circuit, a 1T1C memory cell circuit, and a source follower circuit that performs reading. To examine the scaling limit of the memory element in this study, FE-Caps with different areas were evaluated.

Since the bit line voltage cannot be directly measured in the memory cell evaluation, the source follower characteristics were measured and the relational expression of V_{OUT} and the bit line voltage was obtained before the memory cell evaluation. This enabled the bit line voltage to be estimated from the relational expression of V_{OUT} and the source follower characteristics in the memory cell evaluation, and ΔV_{BL} that is a read potential difference between high V_{OUT} and low V_{OUT} was calculated (Fig. 8).

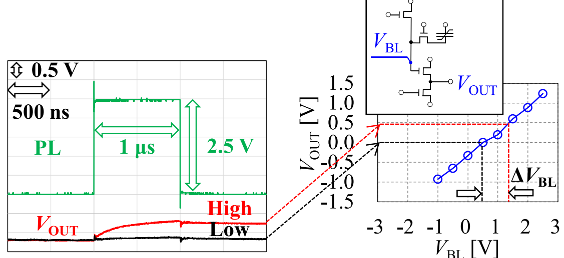


FIGURE 8. Input/output characteristics of OS source follower used for reading from 1-bit OS FeRAM.

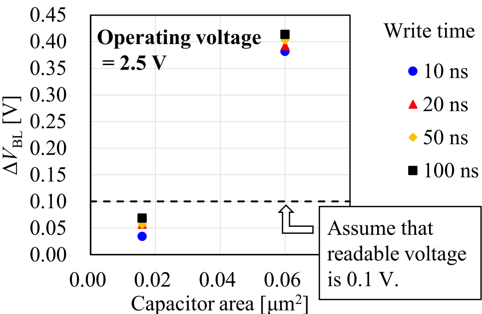


FIGURE 9. The relationship between the FE-Cap area and ΔV_{BL} depending on the write time of the 1-bit OS FeRAM.

C. WRITE TIME EVALUATION

The write time of the 1-bit OS FeRAM was evaluated. The FE-Cap area influences the write time and ΔV_{BL}; thus, the relationship between the FE-Cap area and ΔV_{BL} depending on the write time of the 1-bit OS FeRAM was evaluated. Figure 9 shows ΔV_{BL} with different FE-Cap areas and write times. The write time dependence is very small with FE-Cap areas of 0.016 μm^2 and 0.06 μm^2. A comparatively large ΔV_{BL} is obtained with an FE-Cap area of 0.06 μm^2, whereas a small ΔV_{BL} is obtained with an FE-Cap area of 0.016 μm^2. The reason why ΔV_{BL} is small with an FE-Cap area of 0.016 μm^2 is that the capacitance increases with increasing FE-Cap area and thus Pr also increases, when the measurement is performed with the same HZO thickness and the same potential. The capacitance decreases

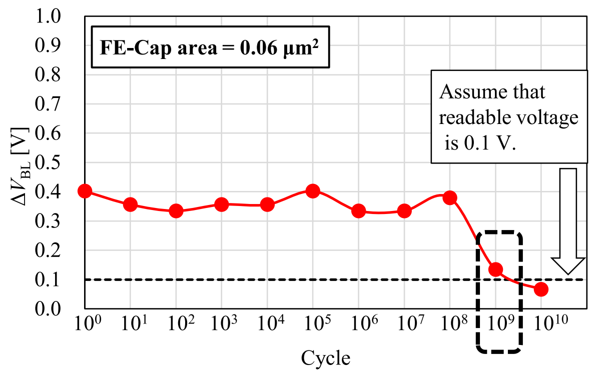


FIGURE 10. ΔV_{BL} change with the number of rewriting times of 1-bit OS FeRAM.

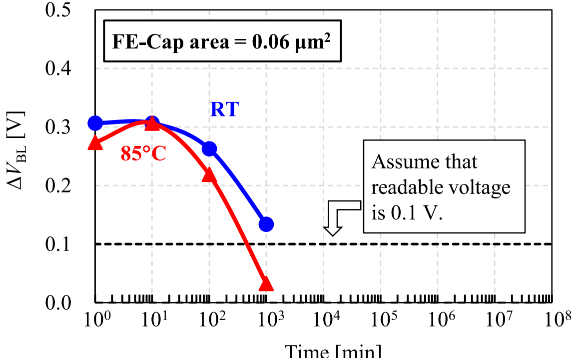


FIGURE 11. ΔV_{BL} change over retention time of 1-bit OS FeRAM.

with decreasing FE-Cap area and accordingly ΔV_{BL} possibly becomes small. In the results in Fig. 9, an FE-Cap area of 0.016 μm^2 might lead to insufficient capacitance and thus the excellent characteristics cannot be obtained; on the other hand, with an FE-Cap area of 0.06 μm^2, ΔV_{BL} of approximately 0.4 V is maintained at an operating voltage of 2.5 V and a write time of 10 ns. This indicates that a write operation is successfully performed.

D. ENDURANCE TEST EVALUATION

The 1-bit OS FeRAM was subjected to an endurance test at room temperature. Figure 10 plots ΔV_{BL} changes versus the rewriting endurance of the OS FeRAM. The value of the read potential difference ΔV_{BL} does not significantly change until the number of rewriting times reaches 10^8 cycles. Assuming that the readable ΔV_{BL} is 0.1 V or higher, the rewriting endurance of 10^9 cycles is possible with an FE-Cap area of 0.06 μm^2.

E. RETENTION TEST EVALUATION

The retention test of the 1-bit OS FeRAM was conducted at room temperature and 85°C. Figure 11 shows ΔV_{BL} change over the retention time of the OS FeRAM. Assuming that the readable ΔV_{BL} is 0.1 V or higher, data retention for 1000 min at room temperature and for 100 min at 85°C was demonstrated.

TABLE 3. Comparison between OS FeRAM in this paper and FeRAMs in other works.

Type	FeFET [14]	FeRAM [15]	FeRAM [2]	FeRAM [4]	FeRAM This Work
Transistor	SiFET	SiFET	SiFET	SiFET	OSFET
Technology node	-	130 nm node	130 nm node	130 nm node	60 nm node
Cap-area	0.004 μm²	0.12 μm²	0.4 μm²	0.2 μm²	0.06 μm²
Structure	1T	1T1C	1T1C	1T1C	1T1C
Write voltage	4.2 V	4.0 V	2.5 V	2.0 V	2.5 V
Write latency	20 ns	100 ns	14 ns	16 ns	10 ns
Retention	250°C > 7 days	125°C > 1000 min.	85°C > 100 min.	85°C > 100 min.	85°C > 100 min.
Endurance	10^5	> 10^{11}	> 10^{11}	> 10^{15}	> 10^9

IV. CONCLUSION

We fabricated the 1T1C OS FeRAM using the OSFET with a higher breakdown voltage than the SiFET and HZO that is a ferroelectric material. The OS FeRAM was fabricated through the BEOL process at a temperature of 450°C or lower, and attained an area reduction per cell by using the combination of the scaled OSFET with L/W of 60 nm/60 nm and the single damascene FE-Cap with no leakage at the edge that has an unprecedentedly small area of 0.06 μm^2. TABLE 3 compares the OS FeRAM in this paper and FeRAMs in other works. The evaluation results demonstrate that the OS FeRAM with an FE-Cap area of 0.06 μm^2 achieves a write time of 10 ns, a rewriting endurance of 10^9 cycles, and a data retention time of 100 min at 85°C. The write voltage of the OS FeRAM including the 60-nm-node OSFETs is comparable to that of the FeRAM including the 130-nm-node SiFETs, which indicates that the footprint can be reduced while the performance is being maintained. The OSFET scaled down to L of 20 nm or smaller can have a breakdown voltage at which a driving voltage of 2.5 V is feasible. Thus, the OSFET is a promising selector element for emerging memories such as FeRAMs.

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