# A Comprehensive RF Characterization and Modeling Methodology for the 5nm Technology Node FinFETs

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**ABSTRACT** This paper aims to provide insights into the thermal, analog, and RF attributes, as well as a novel modeling methodology, for the FinFET at the industry standard 5nm CMOS technology node. Thermal characterization shows that for a 165K change in temperature, the Sub-threshold Slope (SS) and threshold voltage vary by 69 % and ~70 mV, respectively. At room temperature, a single gate contacted n-FinFET RF device exhibits a cutoff and maximum oscillation frequency of ~100 GHz and ~170 GHz, respectively. Analog and RF Figures of Merit (FoMs) for 5 nm technology at a device level and their temperature sensitivity are also reported. The industry standard BSIM-CMG model is modified to capture the impact of self-heating (SH) and parasitics. The SH model is based on measured data, and the modeling approach renders it independent of other model parameters. To the authors' knowledge, an iteration free approach to develop a model-card for RF applications is explained for the very first time. Excellent agreement between the measured data and the model indicates that our methodology is accurate and can be used for faster PDK development.

**INDEX TERMS** Characterization, modeling, RF, analog, self-heating, 5nm technology, FinFET.

## I. INTRODUCTION

The rise of the wireless and Radio Frequency (RF) IC performance in the early 1990's has led to affordable mobile communication. Significant strides in device fabrication techniques in the past two decades have been a key enabler for the explosive growth in the semiconductor industry. Sub-28 nm FinFET technologies ushered in the era of mobile SoCs for 3G/4G smartphones, applications such as High Performance Computing (HPC), Artificial Intelligence (AI), cloud computing, 5G communications. These popular applications, in turn, have increased demand for best-in-class logic and RF technologies with high yield and better performance. These applications are the key driving force for the development of the leading 5 nm CMOS technology, which offers the best in terms of PPACT (Power, Performance, Area, Cost, Time to market) compared to its predecessors [1], [2], [3], [4], [5].

The key challenges encountered when designing RF and analog circuits with digital CMOS technology include (a) the limited number of available devices (active and passive), (b) optimization of logic devices for non-digital design, and (c) characterization and modeling of the devices using simple benchmarks (e.g., drive current and device delay). Some of these challenges can be mitigated at the circuit level. Shin et al. presented an LNA operating in the frequency range of 71 GHz to 76 GHz by considering the self-heating effects in the fin as part of the design flow [6]. However, in general, poor characterization and modeling of devices lead to circuits that cannot achieve the full potential of the underlying technologies. These issues lead to a complex,

error-prone, tedious, and iterative design procedure. Poor characterization of devices leads to inaccurate information about device parasitics and the impact of process variation, making it difficult to define the exact achievable output frequency of designed circuits such as oscillators.

A key issue with state-of-the-art technology nodes, given their increasing density, is self-heating in the devices. The heat dissipation capability of transistors decreases significantly as the device architecture changes from planar to 3-D, while current density (and thus Joule heating) increases. These coupled effects lead to acerbating thermal issues in the device channel [7], [8]. The underlying reason for severe self-heating effects in these high-performance devices is higher drive current and fin density– which lead to a higher thermal resistance for the device [9], [10], [11], [12].

There are multiple studies on the RF characteristics of FinFET devices [13], [14], [15], [16], [17]. However, to the authors' knowledge, existing 5 nm FinFET technology literature is limited to the digital aspects of the technology [18], [19], [20], [21]. An accurate DC and RF model is a critical requirement for the development of RF SoCs for upcoming technologies. In this direction, this work presents an extensive and in-depth characterization of the analog and RF performance of these devices, followed by a thoroughly described model extraction flow (using a modified BSIM-CMG model) for analog and RF applications. Existing literature [22], [23], [24], [25], [26], [27] proposes the extraction of the thermal network after the DC model is extracted, which leads to an iterative approach for the full model development. We propose a step-by-step procedure for model extraction which avoids iterative switching between DC and thermal modeling. The proposed methodology meets the characterization and modeling requirements of all advanced node devices.

There are multiple approaches reported in the literature based on the physical, equivalent circuit, and black-box-based models [28]. This work involves the physics-based modeling approach using the modified BSIM-CMG compact model, and the de-embedded two-port S-parameter data for intrinsic device modeling. Large signal measurement is performed for the complete characterization of an RF transistor, i.e., determining the impact of harmonics and non-linearity. We discuss the experimental setup and the Device Under Test (DUT) in Section II, followed by the characterization techniques in Section III. Section IV discusses the modeling flow, including the model validation on large-signal measurements, and we conclude the paper in Section V.

## II. EXPERIMENTAL DETAILS
### A. DC AND SMALL SIGNAL MEASUREMENTS
Two n-FinFET devices (having length $L_B$ and $L_A = 1.5L_B$), fabricated using an industrial 5 nm FinFET technology, were used for this study. On-wafer measurements were performed using a Cascade Summit 11K Probe Station (Fig. 1(a)). A thermal chuck was used to set the substrate temperature ($T_{sub}$) during the measurements. Bias conditions for the
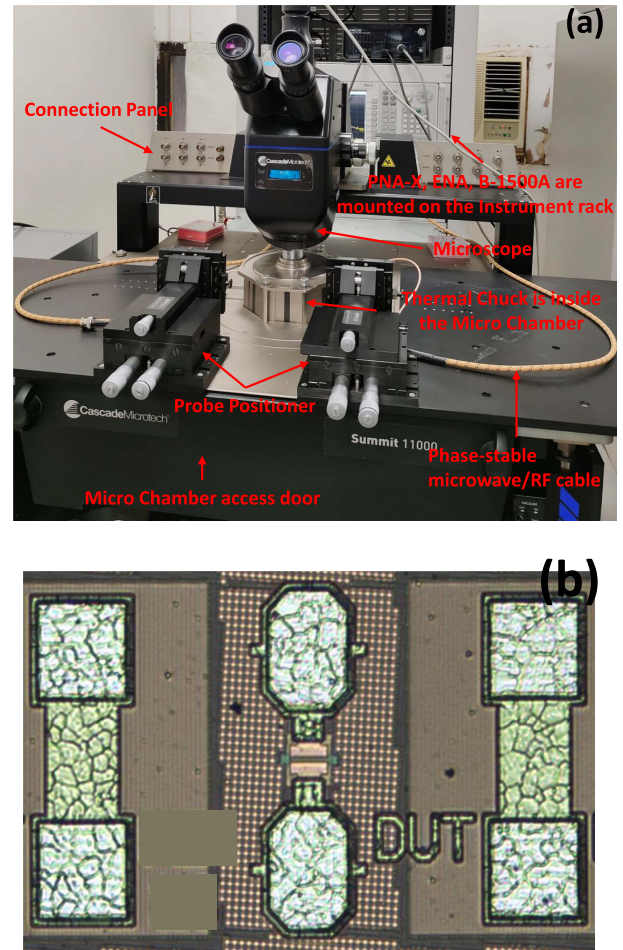




FIGURE 1. Experimental Setup: (a) Photograph of Experimental Setup used for two-port RF measurements (b) DUT embedded in Ground-Signal-Ground structure.

measurements were set using the Keysight B1500A semiconductor parameter analyzer. We used a low-frequency Keysight ENA E-5071C to perform measurements in the 100 kHz-8.5 GHz frequency range and the Keysight PNA-X N5244A for high-frequency measurements (500 MHz-43.5 GHz). All the instruments were controlled through a PC using a Keysight GPIB interface. Using these two sets of instruments for S-parameter measurements allowed us to increase the characterization accuracy for a wide frequency band. The signal power for both instruments was chosen after carefully investigating the low and high-frequency measurements, ensuring that all the measurements remain in small-signal regime to avoid non-linearity. Ground-Signal-Ground (GSG) probes were used for both DC and RF measurements (Fig. 1(b)). Short-Open-Load-Through (SOLT) calibration was performed to shift the reference planes from the instrument ports to the probe tips [23], [24], [29]. Parasitic elements between the probe tips and DUT were de-embedded using on-wafer open-short de-embedding structures [29]. A comparison between measured and de-embedded data
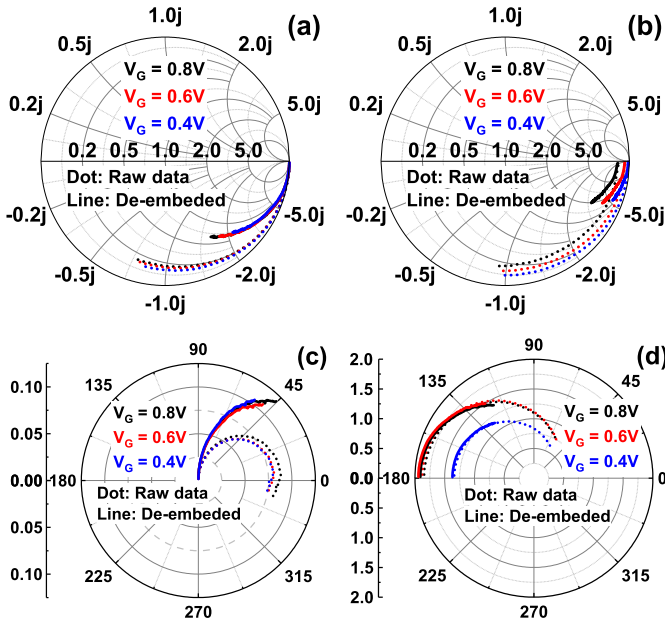
FIGURE 2. Impact of de-embedding on the measured S-parameters: (a) $S_{11}$, (b) $S_{22}$, (c) $S_{12}$, and (d) $S_{21}$ for multiple gate biases at $V_{DS} = V_{DS,SAT}$.



FIGURE 3. Characterization and Modeling Flow.

shown in Fig. 2 highlights the impact of the pad and wiring parasitic.

## B. LOAD-PULL MEASUREMENTS

An AMCAD passive load-pull measurement system with a Cascade Summit probe station is used for large-signal measurements. The load-pull setup consists of a Maury Microwave Load Tuner (XT982GL01) with a frequency range of 0.6 GHz to 18 GHz, Keysight's Network Analyzer (PNA-X N5244A) configured with the tuner to provide the RF signal and Keysight B1500A which is used to supply the DC bias. A high-power bidirectional coupler at the input and output of DUT separates the incident and the reflected RF signal during load-pull measurements. The PNA-X measures the incident and reflected waves from the source and receiver path and calculates large-signal performance metrics such as transducer gain ($G_T$), power gain ($G_p$), Power Added Efficiency (PAE), gain compression, etc. Measurements are performed with the delivered input signal power swept from –43dBm to –32dBm at a frequency of 2.5 GHz. The bias conditions were set at $V_{GS} = 0.5$ V and $V_{DS} = 0.75$ V. To perform the load-pull measurement of the DUT, SOLT and power calibration were performed to remove the impact of wire parasitics on RF signals.

## III. CHARACTERIZATION

The CMOS process is primarily characterized and modeled for digital design. However, a deep understanding of devices can also reduce the large number of iterations involved in RF circuit design. Inaccurate, iterative, and simple modeling of the output resistance (which directly correlates with the matching of transistor impedances) necessitates the
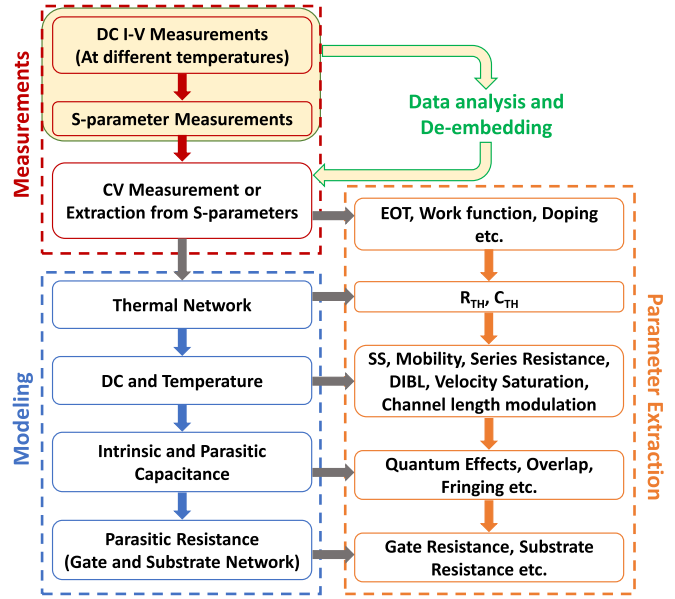
development of specialized characterization for analog and RF applications. In this paper, we characterize and model the DC and RF performance of production level n-type FinFETs fabricated using the 5 nm technology node. The device characterization will be discussed under three different categories as: Thermal, DC, and RF characterization. Characterization, modeling, and parameter extraction flow adopted in this work is illustrated in Fig. 3.

### A. THERMAL CHARACTERIZATION

Thermal characterization is much more pertinent for advanced nodes, given the strong temperature-dependent effects, and has been implemented in two parts in this work. First, we assess the impact of temperature on the device DC and analog Figures of Merit (FoMs), and later, we extract the impact of self-heating on the transistor's RF characteristics.

To evaluate the temperature sensitivity, we measure the DC characteristics at different substrate temperatures (Fig. 4(a) and Fig. 4(b)). The threshold voltage was extracted using the constant current method [30]. Fig. 4(c) shows ~70 mV reduction in $V_{TH}$ with a 165 K increase in temperature. Field-effect mobility for charge carriers shown in Fig. 4(d) is extracted at the peak transconductance ($g_{m,LIN}$ and $g_{m,SAT}$) value using [31], [32]:

$$\mu \cong \frac{g_m}{W/L \cdot C_{GG} \cdot V_{DS}} \tag{1}$$

Carrier mobility (and hence transconductance) varies nonlinearly with temperature [33]. However, for the measured temperature range, this change is almost linear (Fig. 4(d)) and includes the impact of series resistance. A better representation is effective mobility, extracted from the current and capacitance characteristics of the transistor operating in
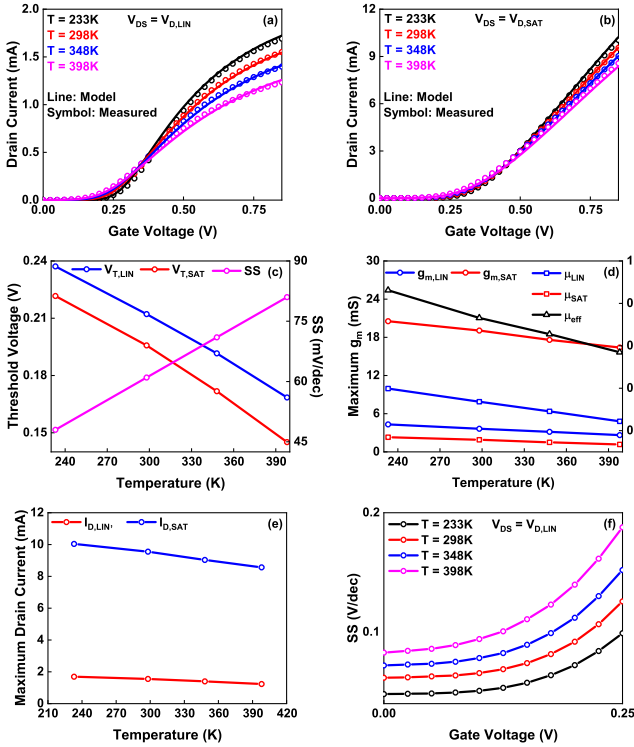
**FIGURE 4.** Thermal Characterization: (a) $I_{DS,LIN}$ (b) $I_{DS,SAT}$ vs. $V_{GS}$ with varying substrate temperature ($T_{sub}$), where, $V_{DS,LIN}$ and $V_{DS,SAT}$ are 0.05 V and 0.75 V, respectively. (c) Threshold Voltage and Sub-threshold Slope vs. $T_{sub}$. (d) Mobility and Transconductance variation with $T_{sub}$. (e) Variation of $I_{DS,LIN}$, $I_{DS,SAT}$ as a function of $T_{sub}$. (f) Sub-threshold Slope variation with Gate Voltage at different $T_{sub}$.

the linear regime using the following expression [34]:

$$\mu \cong -\frac{2 \cdot L}{W \cdot C_{GG} \cdot \Delta V_{DS}} \cdot \left[ \frac{1}{r_{o,1}} - \frac{1}{r_{o,2}} \right] \quad (2)$$

where $W = NF \cdot NFIN \cdot M \cdot (2 \cdot HFIN + TFIN)$ is the total device width, $L$ is the length of the transistor, $C_{GG}$ is the gate capacitance per unit area, $r_{o,1}$ and $r_{o,2}$ are the output resistances at two small drain voltages $V_{D1}$ and $V_{D2}$, and $\Delta V_{DS} = V_{D1} - V_{D2}$. $NF$, $NFIN$ and $M$ are number of fingers, fins and multiplicity, respectively. Degradation in $g_{m,LIN}$ and $g_{m,SAT}$ is 38.75% and 20% respectively for a 165K increase in temperature (Fig. 4(d)). An approximately constant slope of mobility in the studied temperature range points that the phonon scattering is a dominant scattering, and the measured devices exhibit a defect-free high-quality oxide-semiconductor interface. The enhanced phonon scattering with an increase in the temperature further results in $I_{DS,SAT}$ degradation (Fig. 4(e)).

Another important parameter that shows a linear dependence on temperature is the SS (Fig. 4(c)). We observed that reducing the temperature by 165K improves the SS by 69% in the measured temperature range (Fig. 4(f)). Impact of the $T_{sub}$ is also observed on the Cut-off frequency ($f_T$) and is extracted using $g_m / 2\pi C_{GG}$ (Fig. 5(a)). Since analog, digital, and RF circuits operate in the kHz to 1 GHz, 1 GHz to 5 GHz, and 2 GHz to 100 GHz range, respectively,
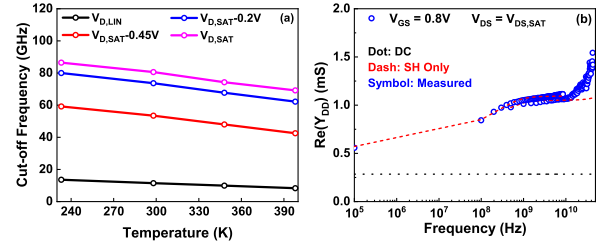


**FIGURE 5.** (a) Variation in Cut-off frequency with increase in $T_{sub}$ at multiple drain biases. (b) Output conductance variation with frequency at $V_{DS} = V_{DS,SAT}$, $V_{GS} = 0.8$ V.

we have characterized the device from DC to 43.5 GHz to observe the impact of SH on digital and RF applications. Variation in the value of $g_{DS}$ with increasing frequency (Fig. 5(b)) confirms the existence of self-heating in the device [12], [22], [23], [24], [25], [35], [36], [37], [38], [39]. Difference between the two sets of measurement data (low and high frequency) in overlapping frequency range is the result of different resistance seen by two measuring instruments. We have included the impact of these resistance in our simulation setup to accurately model the intrinsic device behavior.

## B. DC CHARACTERIZATION

Though advanced models such as BSIM-CMG [40], BSIM-BULK [41], BSIM-IMG [42] have several parameters to accurately mimic the behavior of devices, a significant number of data points are required to accurately model the analog behavior of any technology. For assessing the DC and analog performance of the device, we measured the transfer and output characteristics at multiple drain and gate bias conditions. For assessing the analog performance of the device, metrics like normalized drain current at a constant value of $g_m/I_{DS}$, intrinsic gain ($A_V = g_m / g_{DS}$), cut-off frequency ($f_T$) and maximum frequency of oscillation ($f_{MAX}$) etc., are taken into consideration. Fig. 6(a) and (b) provide a picture of $g_m/I_{DS}$ for both weak and strong inversion of the characterized DUT. The temperature dependence of SS and $\mu$ causes a significant decrease in $g_m/I_{DS}$ in Fig. 6(b) with increasing temperature at lower current densities than at higher current densities. Reduction in temperature can lead to improved performance for both baseband/low-frequency (where higher gain and accuracy are key requirements) and high-frequency (where higher cut-off frequencies are needed). The $g_m$-$A_V$ characteristic plays a crucial role in choosing the device geometry and bias conditions. It reveals that for a higher $g_m$ and constant high gain, one needs to bias the transistor in strong inversion and $V_{DS} \geq 0.3$ V (Fig. 6(c)). Variation of $g_m$ vs. $A_V$ with increasing temperature (Fig. 6(d)) shows that a high value of this metric can be obtained at lower temperatures. Fig. 6(c) and Fig. 6(d) can help in determining the optimum bias and temperature range for target applications.
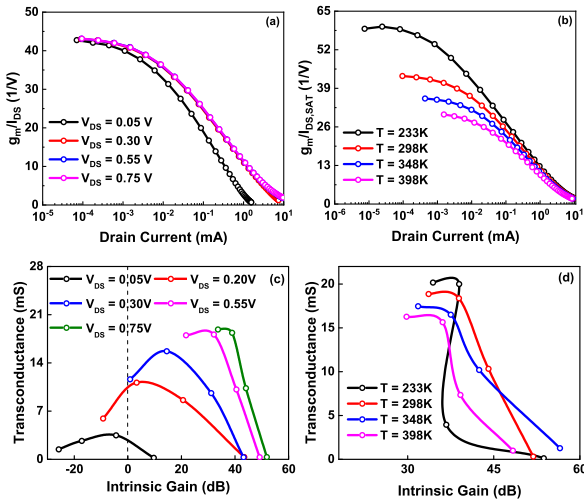
FIGURE 6. These analog metrics are insensitive to L, W, and number of fins: (a) $g_m/I_{DS}$ vs. drain current at room temperature. (b) $g_m/I_{DS}$ as a function of drain current for different temperature at $V_{DS} = V_{DS,SAT}$. (c) $g_m - A_V$ metric for multiple drain biases at room temperature having $V_{GS} = 0.15$ V, 0.35 V, 0.55 V and 0.75 V. (d) Impact of temperature on $g_m - A_V$ metric at $V_{DS} = V_{DS,SAT}$.
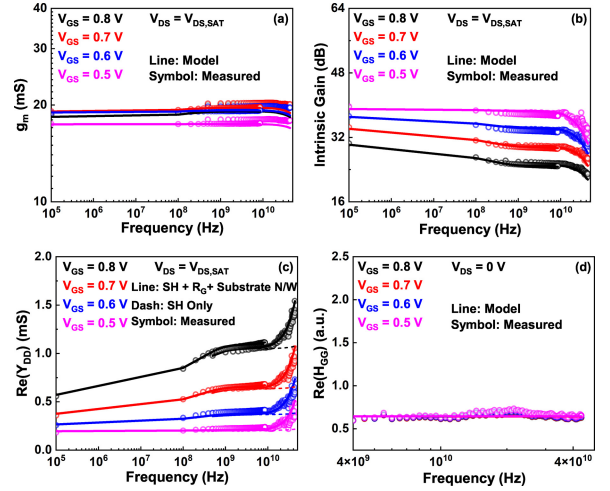


FIGURE 7. RF Performance: (a) $g_m$ vs. frequency extracted using $|Y_{DG}-Y_{GD}|$. (b) Variation of intrinsic gain with frequency. (c) Frequency dependence of $g_{DS}$. (d) Real part of $H_{GG}$ vs. frequency.

## C. RF CHARACTERIZATION

As all the analog/RF FoMs vary with frequency, performance metrics completely based on DC data are inadequate. For example, in Fig. 7(a) $g_m$ shows almost no variations with frequency up to 43.5 GHz, while $A_V$ decreases significantly with increase in frequency (Fig. 7(b)). This decrease can be attributed to the change in $g_{DS}$ (Fig. 7(c)) due to the impact of self-heating, gate and substrate parasitics [12], [22], [23], [24], [25]. To overcome the inaccuracy due to these effects in performance estimation, wide-band characterization is necessary. Device parameters such as mobility ($\mu$), threshold voltage ($V_{TH}$) etc., can also be extracted using the high frequency data [43]. In advanced node devices, SH can be observed between DC to a few GHz due to the short thermal time constant resulting from shrinking device size. SH is characterized based on current and output impedance vs. frequency characteristics. An in-depth discussion of SH modeling is provided in Section IV-A. The frequency at which the impact of SH becomes negligible is known as iso-thermal frequency ($f_{iso}$), and depends on various factors, including device geometry and operating temperature. Variations in Y-parameters above the $f_{iso}$ are caused by parasitic components present at the gate and substrate and by non-quasi static effects. Figs. 8(a) and 8(b) present the two-port equivalent circuit for Y-parameters looking in from the gate and drain terminals. It can be observed that the total gate terminal capacitance is a combination of parasitic and intrinsic capacitances. Extraction of all terminal capacitances looking into the gate and drain terminal from de-embedded Y-parameters has been performed using the expressions given in (3) [22], [23], [24], [38], [44].

$$C_{GG} \approx \frac{Imag(Y_{GG})}{2\pi f}$$

$$C_{DD} \approx \frac{Imag(Y_{DD})}{2\pi f}$$
$$C_{GSB} \approx \frac{Imag(Y_{GG}) + Imag(Y_{GD})}{2\pi f}$$
$$C_{GD} \approx \frac{-Imag(Y_{GD})}{2\pi f} \quad (3)$$

where $Y_{GG}$, $Y_{DD}$, and $Y_{GD}$ are the admittances seen from the transistor's gate terminal (port 1), drain terminal (port 2) and gate-to-drain terminal, respectively. These Y-parameters were obtained from the de-embedded two-port S-parameters of the transistor. A detailed model parameter extraction procedure for accurate modeling of these capacitances is discussed in Table 1.

The extracted value of $R_{GG}$ (Fig. 7(d)) is not the DC gate resistance, as it gets influenced by capacitances looking into the gate, acting in conjunction with source, channel, drain and substrate resistances, etc. Total resistance looking into the gate terminal is extracted from Y-parameters as:

$$R_{GG} \approx \frac{Real(Y_{GG})}{Imag(Y_{GG})^2} \approx Real(H_{GG}) \quad (4)$$

In the sub-threshold regime, $R_{GG}$ vs. $V_{GS}$ characteristics are dominated by the effective substrate resistance in series with the gate-to-body capacitance ($C_{GB}$) (Fig. 8(a)). In the strong inversion, it is predominantly influenced by the physical gate electrode resistance. After evaluating the terminal characteristics, the RF performance of the FinFET is assessed using RF FoMs viz. intrinsic current gain ($A_I = |H_{21}|$), unity gain frequency ($f_T$), power gain ($U$), and a maximum frequency of oscillations ($f_{MAX}$), etc. Current gain $|H_{21}|$ is used to extract $f_T$ while $f_{MAX}$ is evaluated using the unilateral power gain ($U$) (Fig. 9(a)-(d)). $U$ extracted from the Y-parameter data using the formula specified in [38] for $V_{DS} = V_{DD}$ (vdd) and $V_{DS} = V_{DS,LIN}$ is plotted in Figs. 9(b) and 9(d) respectively.

**TABLE 1.** Step-by-step parameter extraction methodology.

| Curves from Experiment | Parameters to Extract | Methodology |
|---|---|---|
| $C_{GG}$ vs. $V_{GS}$ | EOT, PHIG, NDEP | Obtain CV characteristics from S-parameters using (3) and extract mentioned process dependent parameters from $C_{GG}$ at $V_{DS} = 0$ V. |
| $C_{DD}$, $C_{DG}$, $g_{DS}$ vs. frequency, and $dI_{DS}/dT$ | $R_{TH}$, $C_{TH}$ | Extract Imag($Z_{TH}$) and capacitances using (3), and (5) and extract thermal network parameters by self-consistently fitting all curves at higher $V_{GS}$, $V_{DS}$ values. |
| $I_{DS}$ vs. $V_{GS}$ | CDSC, CIT | Focus on sub-threshold region of the log($I_{DS}$) curve at lower $V_{DS}$ (linear region) to fit SS. |
| $I_{DS}$ and $g_m$ vs. $V_{GS}$ | U0, UA, UD, EU, ETA-MOB | Fit both curves simultaneously in the linear regime and moderate to strong inversion to accurately extract these mobility model parameters. |
| $I_{DS}$ and $g_m$ vs. $V_{GS}$ | RSW, RDW, RDSW, RSWMIN, RDWMIN | Observe slope of both curves at a higher $V_{GS}$ (strong inversion) in the linear region of operation to extract series resistance parameters. If necessary, re-optimize UA, EU, and ETAMOB. |
| $I_{DS}$ vs. $V_{GS}$ | CDSCD, ETA0 | Fit SS at multiple $V_{DS}$ (Fitting of SS at this step need not be perfect). |
| $I_{DS}$ vs. $V_{GS}$, $I_{DS}$ vs. $V_{DS}$ | VSAT, VSAT1, KSATIV | Simultaneously fit the $I_{DS} - V_{GS}$, $I_{DS} - V_{DS}$, and their derivatives. The fitting of derivatives at this step does not have to be perfect. |
| $I_{DS}$ and $g_m$ vs. $V_{GS}$ | PTWG | Extract the $g_{m,SAT}$ degradation with increasing $V_{GS}$ by fitting both curves at all drain biases. |
| $I_{DS}$ and $g_{DS}$ vs. $V_{DS}$ | PDIBL2, PCLM | Extract PDIBL2 and PCLM by focusing on lower and higher $V_{GS}$ curves at all drain biases. |
| $I_{DS}$ and $g_{DS}$ vs. $V_{DS}$ | MEXP | Optimize the smooth transitioning of $I_{DS}$ and $g_{DS}$ with increasing $V_{DS}$ at all $V_{GS}$. |
| $I_G$ vs. $V_{GS}$, $I_G$ vs. $V_{DS}$ | AIGBACC, AIGBACC1, BIGBACC, CIGBACC, NIGBACC, AIGBINV, BIGBINV, CIGBINV, EIGBINV, NIGBINV, AIGC, AIGC1, BIGC, CIGC, PIGCD, AIGS, AIGS1, BIGS, CIGS, AIGD, AIGD1, BIGD, CIGD | Fit gate terminal current (gate to body, channel, source, and drain currents, respectively) for the entire bias range. |
| $C_{GG}$, $C_{GSB}$, and $C_{GD}$ vs. $V_{GS}$ | CGBO, CGSO, CGDO | Extract bias-independent overlap capacitance parameters by simultaneously fitting the $C_{GG}$, $C_{GS}$, and $C_{GD}$ curves at $V_{GS} = V_{DS} = 0$ V. If the source and body terminals are tied together, the impact of body-related capacitance can be extracted from the $C_{GS}$ vs. $V_{GS}$ curve. |
| $C_{GG}$, $C_{GSB}$, and $C_{GD}$ vs. $V_{GS}$ | CGSL, CGDL, CGBL, CK-APPAs, CKAPPAD, CK-APPAB, CFS, and CFD | Observe the trend with gate voltage in accumulation and depletion region at multiple $V_{DS}$, and extract bias-dependent overlap and fringing capacitance parameters. |
| $C_{GG}$ vs. $V_{GS}$ | QMTCENCV, QM0, and PQM | Extract the quantum effect-related parameters at higher $V_{GS}$ and $V_{DS} = 0$ V. Here, QM0 and PQM should be extracted by observing the slope/steepness of the curve. One must also notice the impact of source and drain resistance on $C_{GS}$, and $C_{GD}$. If the different value of $C_{GS}$ and $C_{GD}$ is observed at higher $V_{GS}$, parameters related to the source and drain resistance should be retuned by keeping the total series resistance similar to what is extracted from DC current characteristics. |
| $C_{GG}$, $C_{GSB}$, and $C_{GD}$ vs. $V_{GS}$ | PCLMCV, VSATCV | Observe the plots in strong inversion at multiple $V_{DS}$, and extract the impact of velocity saturation and channel length modulation on capacitances. |
| $R_{SUB}$, Re($Y_{DD}$) vs. frequency | $R_B$ | Extract substrate resistance $R_{SUB}$ using the (6). Fit $R_{SUB}$ vs. frequency at $V_{DS} = V_{GS} = 0$ V. While extracting the parameters related to the $R_{SUB}$, also focus on the real part of $Y_{DD}$ above $f_{iso}$ for more accurate results. |
| $R_{GG}$, Re($Y_{DD}$) vs. frequency | XRCRG1, XRCRG2 | Extract gate resistance using the (4). Fit $R_{GG}$ vs. frequency at $V_{DS} = 0$ V for multiple $V_{GS}$. While extracting the parameters related to the $R_{GG}$, one should target to accurately fit the real and imaginary parts of $Y_{GG}$ and $Y_{DD}$ above $f_{iso}$. |

The $f_{MAX}$ is defined as the frequency at which extrapolated value of $U$ equals unity.

The extracted value of $f_T$ in the strong inversion regime will be smaller than in moderate inversion, with the latter being the region where devices are biased for most RF applications. Hence, keeping typical applications in mind, $f_T$ is extracted from the moderate to strong inversion regimes, as shown in Figs. 9(a) and 9(c) [45], [46]. $|H_{21}|$ starts saturating after a certain frequency, primarily in the weak inversion regime at lower $V_{DS}$ values (Fig. 9(c)). While we can still use the $g_m / 2\pi C_{GG}$ approximation to extract $f_T$ after the cut-off frequency, linear extrapolation of non-saturated $|H_{21}|$ is used to extract the $f_T$ here. The $f_T$ with respect to normalized drain current is plotted in Fig. 9(e). The $g_m$ increases with increasing $V_{GS}$ (current density) and then starts decreasing at higher current densities. On the other hand, gate capacitance increases with increasing $V_{GS}$ (current density) and saturates at high current density, making
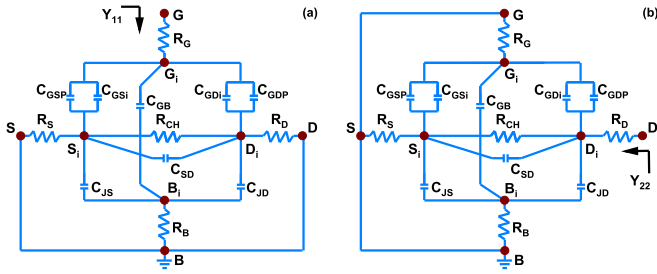
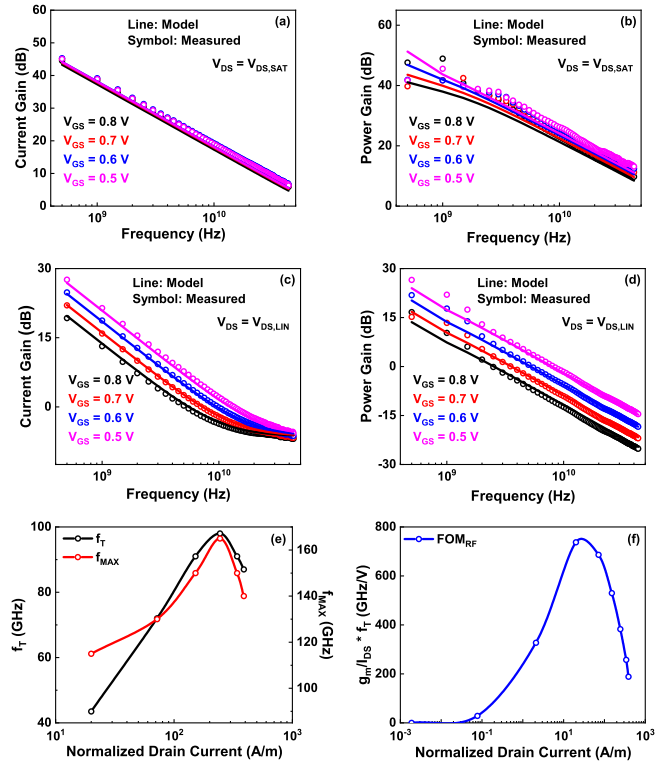**FIGURE 8.** Equivalent Networks: (a) for calculating $Y_{GG}$. (b) for calculating $Y_{DD}$.



**FIGURE 9.** RF FoMs: (a) Current Gain ($H_{21}$) vs. Frequency for multiple gate bias conditions at $V_{DS} = V_{DS,SAT}$. (b) Power gain ($U$) variation with frequency for multiple gate voltage at $V_{DS} = V_{DS,SAT}$. (c) Variation of Current Gain with frequency for increasing gate voltage values at low $V_{DS}$ value. (d) Power gain variation with frequency for multiple gate voltage at $V_{DS} = V_{DS,LIN}$. (e) $f_T$ and $f_{MAX}$ vs. normalized drain current at $V_{DS} = V_{DS,SAT}$. (f) $FOM_{RF}$ vs. normalized drain current at $V_{DS} = V_{DS,SAT}$.

$f_T$ reach a maximum value and decrease after that, as shown in Fig. 9(e). To optimize the operating point based on the trade-off between current efficiency and $f_T$, another RF FoM (($g_m/I_{DS}) * f_T$) vs. normalized current is illustrated in Fig. 9(f). This metric degrades at a lower current than $f_T$ because both $f_T$ and $g_m/I_{DS}$ degrade with increasing $I_{DS}$ at high $I_{DS}$.

## IV. PARAMETER EXTRACTION PROCEDURE AND MODEL VALIDATION

Based on the characterized data, we have developed and extracted a model valid from DC to 43.5 GHz. As thermal network for SH modeling can be extracted based on
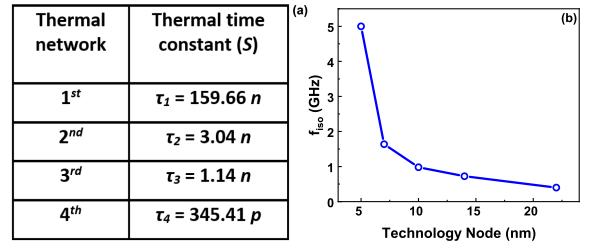


**FIGURE 10.** (a) Extracted fourth order network thermal time constants. (b) Comparison of iso-thermal frequency for different FinFET technology nodes.
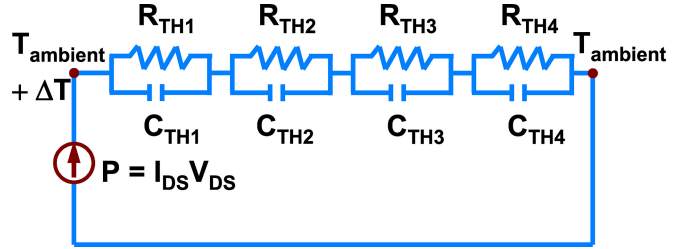
| Thermal network | Thermal time constant ($S$) |
|---|---|
| $1^{st}$ | $\tau_1 = 159.66\,n$ |
| $2^{nd}$ | $\tau_2 = 3.04\,n$ |
| $3^{rd}$ | $\tau_3 = 1.14\,n$ |
| $4^{th}$ | $\tau_4 = 345.41\,p$ |



**FIGURE 11.** The $4^{th}$ order thermal network for SH modeling over a wide frequency spectrum.

measurement data only. To avoid the iterations between DC, thermal, and RF model extraction, we have proposed that impact of SH should be extracted before extraction of the DC and RF model.

### A. THERMAL EFFECTS MODELING

In advanced technology nodes, reduction in transistor size and increased multi-fin density leads to a steep increase in the thermal resistance ($R_{TH}$), which determines the degree of self-heating ($\Delta T = R_{TH} * P$) in the device. At the same time, a reduction in volume causes an even greater decrease in the thermal capacitance ($C_{TH}$), which leads to a reduced thermal time constant $R_{TH} * C_{TH}$ (Fig. 10(a)). A reduced thermal time constant leads to significant SH effects even at very high frequencies, i.e., higher $f_{iso}$ (Fig. 10(b)). A single-order thermal network (cell with a parallel combination of single $R_{TH}$ and $C_{TH}$) cannot capture the thermal contribution over this large frequency range and necessitates using a higher-order thermal network, which connects multiple single-order thermal networks in series (Fig. 11(b)). In this work, $f_{iso}$ is determined to be 5 GHz from the plateau observed in output capacitance ($C_{DD}$) and transcapacitance ($C_{DG}$) (Figs. 12(a)-(b)). The extracted value of $f_{iso}$ shows that for accurate RF modeling, SH effects must be evaluated over a wider frequency range than in older technology nodes (Fig. 10(b)) [47]. Figs. 13(a)-(b) illustrate the dependence of output conductance degradation on self-heating and parasitics ($\Delta g_{DS,SH}$, $\Delta g_{DS,P}$, and $\Delta g_{DS}$) with varying gate bias (where $\Delta g_{DS,SH}$ is the difference between the output conductance at $f_{iso}$ ($g_{DS,iso}$) and at low frequency ($g_{DS}(100\,\text{kHz})$)). Since at lower gate voltages, the amount of current flowing inside the channel and power dissipated is very low, the degradation in $g_{DS}$ due to SH is very low and increases
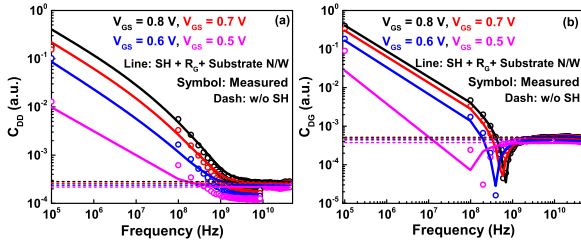
**FIGURE 12.** Thermal Network Extraction: Variation of capacitances vs. frequency (a) $C_{DD}$ and (b) $C_{DG}$ for different gate biases at $V_{DS} = V_{DS,SAT}$.
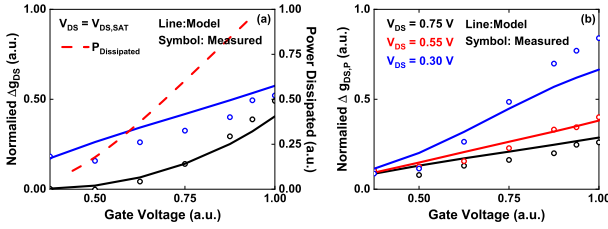


**FIGURE 13.** (a) Variation of amplitude transition in $g_{DS}$ with varying gate bias at constant $V_{DS}$ values due to: (i) Gate and Substrate parasitics, (ii) SH, (b) $g_{DS}$ degradation over the measured frequency at multiple drain voltages due to SH and parasitics. Where $\Delta g_{DS,P} = g_{DS}(f)(43.5\ GHz) - g_{DS,iso}$, $\Delta g_{DS,SH} = g_{DS,iso} - g_{DS}(100\ kHz)$ and $\Delta g_{DS}(f) = g_{DS}(43.5\ GHz) - g_{DS}(100\ kHz)$.

with increasing gate voltage. The $\Delta g_{DS,P} = g_{DS}(43.5\ \mathrm{GHz}) - g_{DS,iso}$ shown in Fig. 13(a) describes the impact of gate and substrate parasitics at constant $V_{DS}$ values with varying $V_{GS}$. The impact of parasitics on $\Delta g_{DS}$ increases with increasing $V_{GS}$ and reduces in the saturation regime. However, $\Delta g_{DS}$ (Fig. 13(b)) reduces with increasing drain voltages at a fixed gate voltage, which is due to the stronger dependence of $g_{DS}$ on parasitics compared to the variation in $g_{DS}$ due to SH. The minor difference between the measured and model results can be attributed to the noisy behavior of measured data with frequency. However, trends of simulation results from the extracted model are in good agreement with silicon data. Variation of $\Delta g_{DS}$ due to both SH and gate and substrate parasitics with increasing gate bias is presented in Fig. 13(b). Figs. 7(a) and (c) show that SH related variation in $g_{DS}$ is higher than $g_m$. As the intrinsic gain of the transistor shown in Figs. 6(c)-(d) is inversely related to $g_{DS}$, study of these variations in $\Delta g_{DS,SH}$, $\Delta g_{DS,P}$ and $\Delta g_{DS}$ with varying bias voltages becomes more important for analog and RF amplifier designs.

Hence, prior to the DC and RF modeling of devices, model parameters related to the thermal network (Fig. 11) are extracted using the measured DC and RF data. The output conductance ($g_{DS}$) curve (Fig. 7(c)) shows an increase with increasing frequency. Transitions in $g_{DS}(f)$ can be attributed to various physical phenomena like SH, gate, and substrate-related effects. Reduction of the channel length makes it difficult to separate the impact of SH and parasitics on the $g_{DS}(f)$ curve. Therefore, for the extraction of SH-related parameters, we analyze the total drain capacitance ($C_{DD}(f)$)
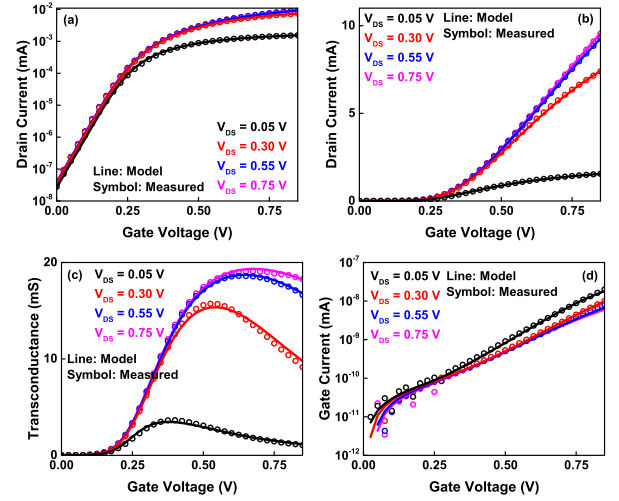


**FIGURE 14.** DC Transfer Characteristics: (a) Log($I_{DS}$) $-V_{GS}$. (b) $I_{DS} - V_{GS}$. (c) $g_m - V_{GS}$. (d) $I_G - V_{GS}$.

and drain-to-gate capacitance ($C_{DG}(f)$) characteristics apart from the $g_{DS}(f)$ curves, plotted in Fig. 12, as they depict several orders of change with frequency [24], [25], [36], [39]. Complex thermal impedance values can be evaluated from the measured data using the relation:

$$\frac{Z_{TH}}{Y_{DD} - Y_{DD}^{iso}} = \left[ \frac{dI_{DS}}{dT}\left( I_{DS} + V_{DS} \cdot Y_{DD}^{iso} \right) \right]^{-1} \quad (5)$$

where, $Z_{TH}$ is a complex thermal impedance of the $4^{th}$ order thermal network, $Y_{DD}^{iso}$ is the iso-thermal value of the output admittance and $dI_{DS}/dT$ represents the temperature sensitivity of the output current. For accurate thermal modeling, parameters of a $4^{th}$ order thermal network are extracted by self-consistently fitting the $g_{DS}(f)$, $C_{DD}(f)$, $C_{DG}(f)$ and $Im(Z_{TH})$ curves up to and beyond the iso-thermal frequency. To ensure the robustness of the extracted thermal model, we have presented the self-consistent fitting results from our SH network for different biases in Figs. 7(c) and 12(a)-(b).

## B. DC MODELING

The extracted values of the $4^{th}$ order thermal network parameters are used to incorporate the impact of SH in DC characteristics. Process parameters values, i.e., Effective Oxide Thickness (EOT), flat-band voltage, overlap capacitance, fringing capacitance, etc., are extracted from the total gate capacitance ($C_{GG}$) vs. gate voltage ($V_{GS}$) characteristics (Fig. 17(a)), evaluated using Y-parameters at a frequency of 500 MHz. Parameters related to trap density, DIBL, SS etc. are extracted from transfer characteristics ($I_{DS} - V_{GS}$) at several drain voltages ($V_{DS}$) on a semi-log scale as shown in Fig. 14(a). Parameters related to physical effects, i.e., mobility degradation, series resistance, high field degradation, etc., are extracted from transfer characteristics in the linear region (Fig. 14(b)) [48], [49]. The impact of velocity saturation, channel length modulation, etc., is modeled using the transfer characteristics in the
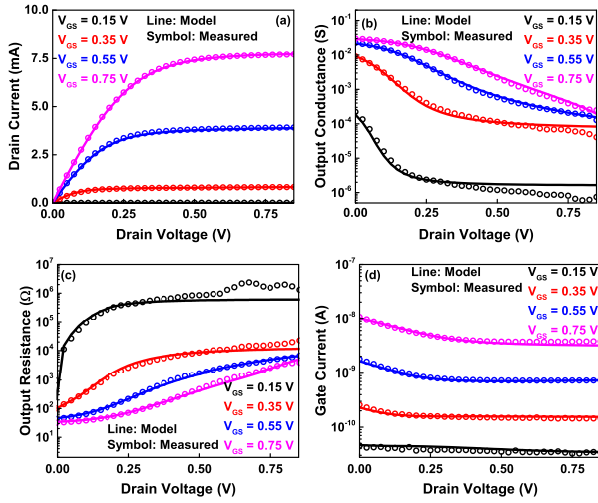
**FIGURE 15.** Output Characteristics: (a) $I_{DS}$ vs. $V_{DS}$. (b) Log ($g_{DS}$) vs. $V_{DS}$. (c) $R_{out}$ vs. $V_{DS}$. (d) $I_G$ vs. $V_{DS}$.
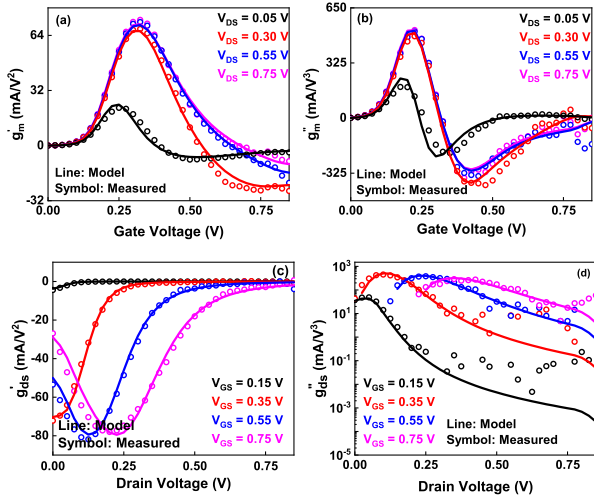


**FIGURE 16.** Higher Order Derivatives of DC current: (a) $g_m'$ - $V_{GS}$. (b) $g_m''$ - $V_{GS}$. (c) $g_{DS}'$ - $V_{DS}$. (d) $g_{DS}''$ - $V_{DS}$.

saturation region, as well as the output characteristics, as shown in Figs. 14(b) and 15(a) respectively. For a more accurate model, we refine the parameters related to DIBL by fitting the drain current in the log scale (Fig. 14(a)) at multiple $V_{DS}$, as well as the $g_{DS}$ (Fig. 15(b)) curves at lower gate voltages simultaneously. The extracted model results in a good fit between the model and measured data for transconductance, output resistance, and gate current (Figs. 14(c)-(d), 15(c)-(d)). Harmonic distortion (HD) characteristics get affected by higher-order derivatives, which necessitates the accurate modeling of higher-order current derivatives. An excellent fit with measured data for highest order derivatives is presented in Fig. 16. After extracting the entire charge-based DC model, we have extracted the impact of quantum confinement by observing various capacitances, i.e., $C_{GG}$, $C_{GSB} = C_{GS} + C_{GB}$, $C_{GD}$ etc. at zero drain voltage (Figs. 17(a)-(c)). Junction capacitance values are extracted
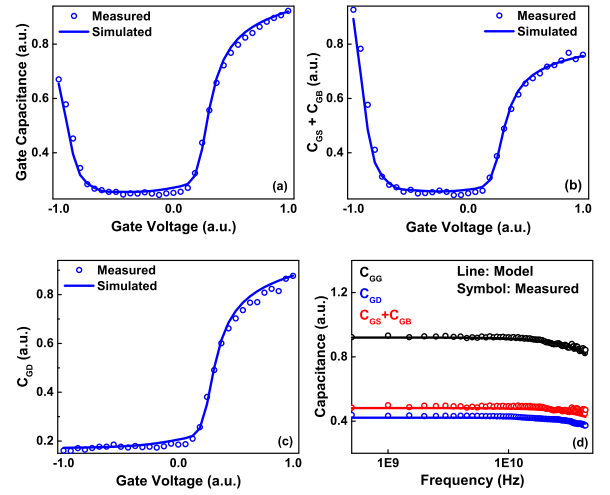


**FIGURE 17.** Terminal Capacitances: (a) $C_{GG}$ vs. $V_{GS}$. (b) $C_{GSB}$ vs. $V_{GS}$. (c) $C_{GD}$ vs. $V_{GS}$. (d) Variation in $C_{GG}$, $C_{GSB}$, and $C_{GD}$ with frequency in strong inversion at $V_{DS} = 0$ V.

using Y-parameters as: $C_{jd} = \text{Im}(Y_{DD} + Y_{GD}) / 2\pi f$. Since the OFF state is mainly dominated by junction capacitance, we choose an off-state bias condition to extract the junction capacitance.

### C. RF MODELING

For high-frequency modeling, capacitance vs. frequency curves are used to verify the extracted parasitic capacitance values (Fig. 17(d)). Junction capacitance also plays an important role in model extraction at higher frequencies. The influence of junction capacitance and gate resistance at higher frequencies can be observed in the $C_{DD}(f)$ and $C_{DG}(f)$ characteristics. Good match between the model and measured data for $C_{DD}(f)$ and $C_{DG}(f)$ is possible because of the SH, junction capacitance, and gate resistance models (Fig. 12(c)). This further accentuates the necessity to accurately extract the gate resistance and junction capacitances. At very high frequencies, most of the capacitances related to the gate network allow the signal to flow from the gate to the channel, making the physical gate electrode resistance the dominant component in strong inversion. In the ON state of the transistor, applied RF signal at gate terminal sees the inversion charge layer below the oxide and flows from gate towards source and drain terminal. Hence, the real components of the input and output impedances get influenced by the physical gate resistance ($R_{G,eltd}$), which represents the distributed resistance of the gate material over the channel [50]. Increase in $g_{DS}(f)$ above the iso-thermal frequency is modeled using gate resistance as shown in Fig. 7(c). The physical gate electrode resistance value is extracted from the total resistance looking into the gate terminal ($R_{GG}(f) = \text{Re}(H_{GG}(f))$) and output impedance curve in strong inversion (Figs. 7(c)-(d)). In the OFF state of the transistor (corresponding to the absence of the inversion charge layer), the applied RF signal at the gate terminal travels directly from the gate toward the substrate
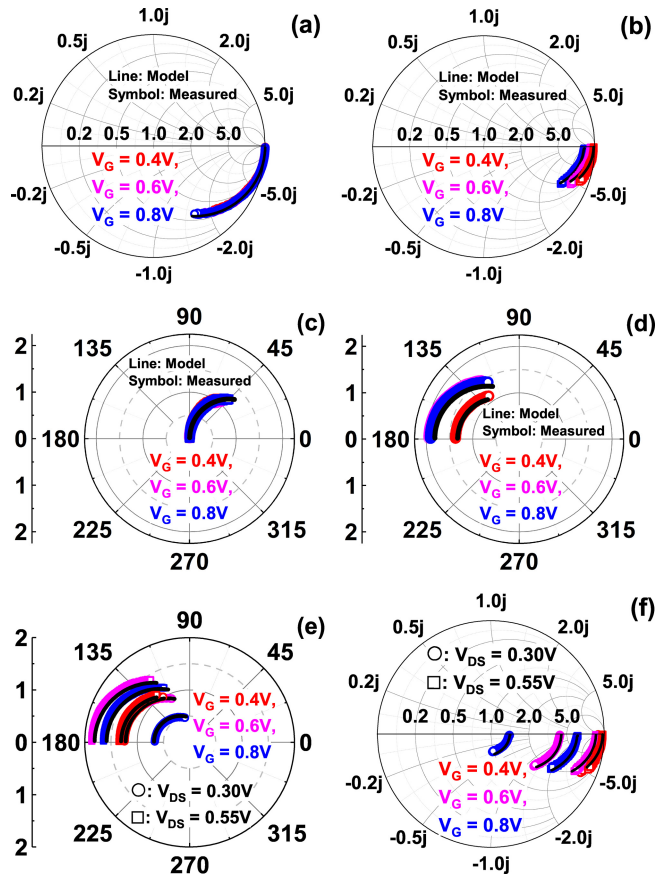
**FIGURE 18.** S-parameter validation of device A for frequency range of 500 MHz to 43.5 GHz: measured and modeled (a) $S_{11}$, (b) $S_{22}$, (c) $S_{12}$, and (d) $S_{21}$ for multiple gate biases at $V_{DS} = V_{DS,SAT}$. (e) $S_{21}$ and (f) $S_{22}$ for $V_{DS} = 0.3$ V and 0.55 V at multiple gate voltages.



**FIGURE 19.** S-parameter validation of device B for frequency range of 500 MHz to 43.5 GHz: (a) $S_{11}$, (b) $S_{22}$, (c) $S_{12}$, and (d) $S_{21}$ for $V_{DS} = 0.75$ V with varying gate voltages.



**FIGURE 20.** Large signal modeling validation of device A: measured and simulated output power ($P_{out}$), power gain and Power Added Efficiency (PAE) variation with delivered input power ($P_{in,del}$) at f = 2.5 GHz, $V_{GS} = 0.5$ V and $V_{DS} = 0.55$ V.

terminal. At higher frequencies, the junction impedance reduces significantly and couples the applied RF signal at the drain terminal to the bulk terminal via a series connection of drain resistance, drain-to-body junction capacitance, and substrate resistance as shown in Fig. 8(b) [23], [50]. Hence, the influence of the substrate network can be observed in the off-state by looking at $g_{DS}(f)$, $R_{GG}(V_{GS})$ plots [37], [44]. The effective value of the substrate resistance looking into the drain terminal can be calculated using the following relation [50]:

$$R_{sub,d} = \frac{Re(Y_{DD}) - g_{DS} - \omega^2 \cdot C_{GD} \cdot C_{DG} \cdot Re(H_{GG})}{[Im(Y_{DD})]^2} \quad (6)$$

For the final validation of the modeling strategy and extracted model, measured and modeled S-parameters for two different gate length devices (labeled Device A and Device B) are presented in Fig. 18 and 19, while the large signal measurement and simulation results of device-A are given in Fig. 20. A good correlation between simulated and measured data shown for both the weak and strong inversion regimes confirms the accuracy of the extracted model.
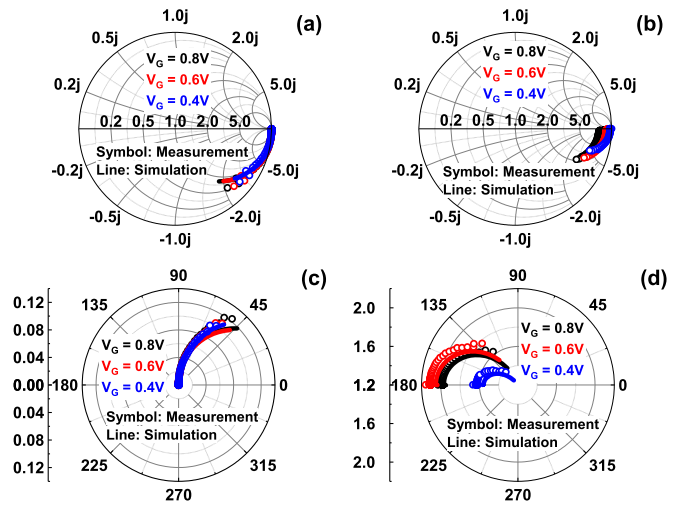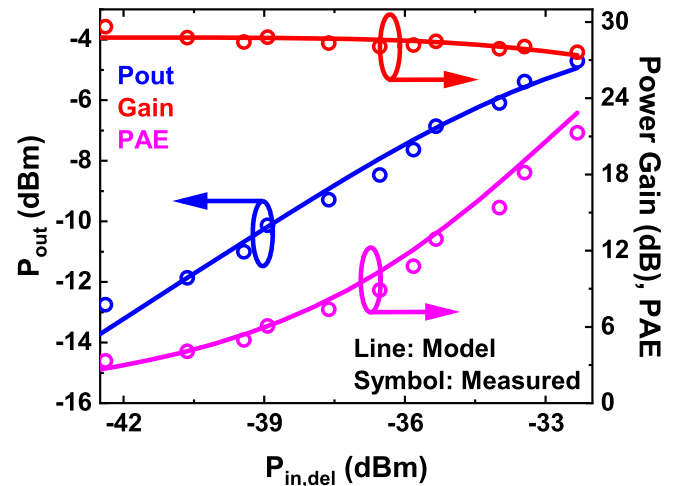
## V. CONCLUSION
Characterization, modeling, and model parameter extraction of the state-of-the-art 5 nm FinFETs are presented. A meticulously phased procedure for the extraction of a complete DC and RF model is presented for wide ranges of temperature, bias, and frequencies. SH extraction methodology based on a $4^{th}$ order thermal network is used for DC and RF modeling. The presented approach leads to a simplified flow for accurate extraction of the model and for Process Development Kit (PDK) development. The impact of self-heating is observed up to 5 GHz, which can affect the performance of the digital, analog, and RF circuits.

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