Received 31 May 2023; revised 8 July 2023; accepted 18 July 2023. Date of publication 20 July 2023; date of current version 3 August 2023.
The review of this article was arranged by Editor M. T. A. Rahimo.

*Digital Object Identifier 10.1109/JEDS.2023.3297329*

# The Chip-Level and Package-Level Degradation of Cascode GaN Device Under Repetitive Power Cycling Stress

**YIJUN SHI, SHAN WU, ZHIYUAN HE, ZONGQI CAI, LIYE CHENG, YUNLIANG RAO, QINGZHONG XIAO, YIQIANG CHEN (Member, IEEE), AND GUOGUANG LU**

China Key Laboratory of Reliability Physics and Application Technology for Electronic Components, Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou 510610, China

CORRESPONDING AUTHORS: Z. HE, L. CHENG, AND Q. XIAO (e-mail: hezhiyuan1988@126.com; chengliye4213@126.com; xiaoqingzhong@ceprei.com)

This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant 62004046, Grant 52107184, and Grant 62274043; in part by the National Key Research and Development Program of China under Grant 2021YFB3602300; in part by the Natural Science Foundation of Guangdong Province under Grant 2022A1515012127; and in part by the Guangzhou Basic and Applied Basic Research Project under Grant 202201010868.

**ABSTRACT** In this work, the electrical characteristics' failure due to the chip-level damage and its relationship with the package-level degradation have been investigated for the Cascode GaN device under long-term repetitive power cycling test (PCT). At first, it is found that, the device's transfer characteristics and threshold voltages have not changed until 8000-cycle PCT, while its on-state current decreases as the increases in cycles number. Meanwhile, the device's gate-to-source leakage have not changed even after 8000-cycle PCT, but there is a significant increase in drain-to-source leakage. The above phenomenon has been attributed to the structural damage in the gate region of GaN HEMT, which has been verified by TCAD simulation and EMMI analysis. Then, it is found that the device's thermal resistance is increased after the repetitive power cycling test, which is due to the package-level degradation. The increased thermal resistance will lead to the increase of heat accumulation, which has been verified by TCAD simulation, subsequently leading to the chip-level damage and electrical performance failure for Cascode GaN device. The relevant results may help to improve the long-term reliability of Cascode GaN device.

**INDEX TERMS** GaN HEMTs, power cycling test, package degradation, chip-level degradation.

## I. INTRODUCTION

Gallium nitride (GaN) has the advantages of wide band gap, high saturated electron drift velocity, high electron mobility, and high thermal conductivity, which make it to be an extremely ideal semiconductor material for the high-voltage, high-frequency, high-temperature, and high-power applications [1], [2], [3], [4], [5], [6]. GaN is expected to solve the "silicon limit" problem faced by the power electronics technology, and has become a research hotspot in the field of power electronics technology. GaN high electron mobility transistor (HEMT) is the most attractive structure in GaN power devices due to its mature technology, simple process, and excellent performance [1], [2], [3]. Currently, GaN HEMTs have gained more and more attentions in high-power applications. However, due to the strong polarization effect in AlGaN/GaN heterostructures, the conventional GaN HEMTs exhibit a negative threshold voltage characteristic [7], [8], [9]. In the field of power electronics technology, the enhancement mode (*E*-mode, or Normally Off) transistors with a positive threshold voltage can bring great convenience and are necessary in some applications for the safety considerations [1], [2], [3]. The enhancement technologies for AlGaN/GaN power devices mainly include P-type gate technology [10], [11], fluorine ion implantation technology [12], [13], [14], [15], [16], Cascode technology [17], thin barrier layer technology [18], and recessed-gate technology [3], [19], [20], [21]. Among them, the *E*-mode GaN HEMTs based on Cascode technology have been commercialized.

In spite of their superior operation properties, the long-term reliability of the Cascode GaN devices has drawn great concern. Many works have been carried out to investigate the long-term reliability of Cascode GaN device. Namely, the

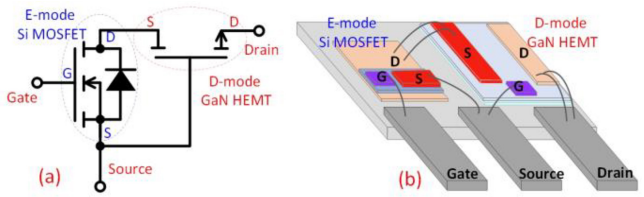


**FIGURE 1.** Equivalent circuit (a) and internal package structure (b) of Cascode GaN device.

power cycling test (PCT) [22], [23], [24], [25], [26], [27] is commonly used for investigating the long-term reliability of power devices, since it can simulate the practical working conditions for power devices. Generally, the failure mechanisms of Cascode GaN device can be classified as the chip-level and package-level degradation. The chip-level degradation of Cascode GaN device is mainly related to the gate region of GaN HEMT, the device's electrical characteristics will be affected by the gate region's internal and nearby defects generated during the long-term stress test. The package-level degradation is mainly related to solder layer and bond wire, the degradation in solder layer and bond wire may affect the thermal and electrical characteristics of the device. However, quite a limited study gives a comprehensive analysis on the relationship between the chip-level and package-level degradation for Cascode GaN device under long-term repetitive power cycling stress.

In this work, the electrical characteristics' failure due to the chip-level damage and its relationship with the package-level degradation have been investigated for the Cascode GaN device under long-term repetitive power cycling stress. It is found that the increased thermal resistance due to the package-level degradation will lead to the increase in heat accumulation, subsequently leading to the chip-level damage and device's electrical performance failure. The relevant conjecture has been verified through TCAD simulation, EMMI analysis and SAM analysis. The manuscript is organized as follows: The experiment details of the long-term repetitive power cycling test are presented in Section II; The electrical characteristics' failure behavior, the package-level degradation behavior, and the relationship between the two are investigated in Section III; The conclusions are drawn in Section IV.

## II. EXPERIMENT DETAILS

In this work, the commercially available Cascode GaN device (TPH3206PSB From Transporm) is employed to carry out relevant research. Fig. 1 gives the equivalent circuit and internal package structure of the Cascode GaN device, which contains a high-voltage *D*-mode GaN HEMT and a low-voltage *E*-mode Si power device. The source electrode of the low-voltage *E*-mode Si power device and the gate electrode of the high-voltage *D*-mode GaN HEMT are shorted together as the source electrode of the Cascode GaN device, the drain electrode of the low-voltage *E*-mode Si power device and the source electrode of the high-voltage *D*-mode GaN HEMT are shorted together, the ohmic drain electrode of the high-voltage *D*-mode GaN HEMT is used as the drain electrode of the Cascode GaN device, and the gate electrode of the low-voltage *E*-mode Si power device is used as the gate electrode of the device. At this time, the low-voltage *E*-mode Si power device determines the threshold voltage of the Cascode GaN device, and the breakdown voltage of the Cascode GaN device is determined by the high-voltage *D*-mode GaN HEMT. The *E*-mode GaN HEMT based on the Cascode technology has the advantages of simple driving circuit and high threshold voltage.

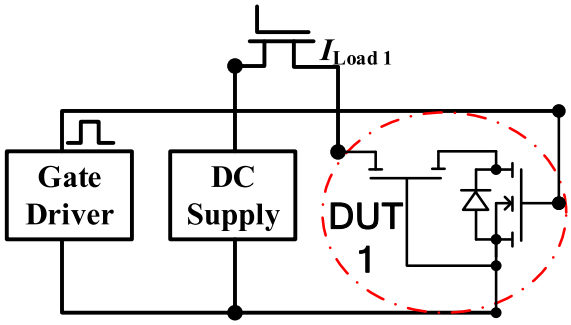


**FIGURE 2.** Simplified diagram of the power cycling test (PCT).

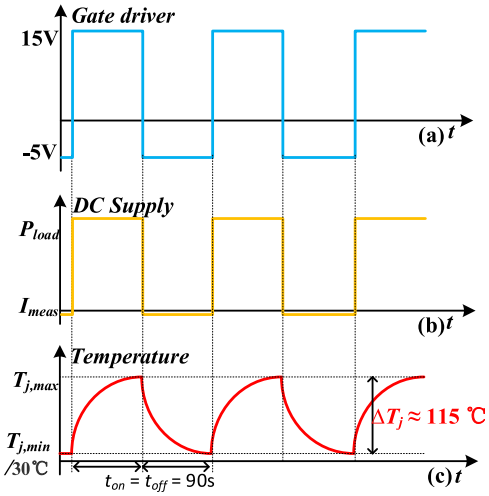


**FIGURE 3.** PCT setup: (a) gate voltage waveform with $t_{on}/t_{off}$ of 90s/90s, (b) load power and measurement current waveform, and (c) typical junction temperature waveform during PCT.

Fig. 2 shows the simplified diagram of the adoptable PCT setup. And Fig. 3 exhibits the working waveform for the devices under test (DUTs) during PCT. One power cycle of a typical PCT contains an active heating phase and a passive cooling phase. According to the duration of the power cycle, the PCT test is generally divided into fast and slow PCT, and the latter is adopted in this work to accelerate failure and shorten the required number of cycles [22], [23], [24], [25], [26], [27]. The time of the active heating phase (also is the on-state time of DUT, $t_{on}$) and the time of the passive cooling phase (also is the off-state time of DUT, $t_{off}$) are set to 90s and 90s, respectively. In the

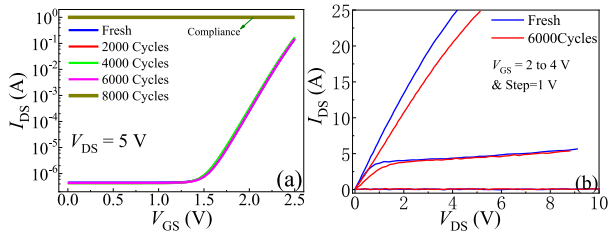


**FIGURE 4.** Transfer characteristics (a) and output characteristics (b) of the Cascode GaN device before and after PCT.

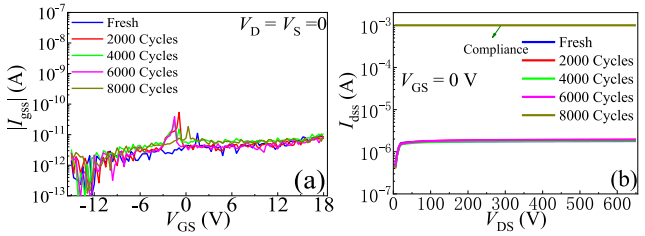


**FIGURE 5.** The gate-to-source leakage (a) and drain-to-source leakage (b) of the Cascode GaN device before and after PCT.

active heating phase, an additional high load power ($P_{load}$) is used to heat DUTs, as shown in Fig. 3(a) and Fig. 3(b). In the passive cooling phase, the negative voltage of −5V is used to quickly turn off DUT, and the forced air-cooling system is employed to quickly cool down the heated DUT. The long on-state/off-state time is employed to ensure that the junction temperature in the heating phase is close to the maximum operating temperature (150°C), and the maximum junction temperature fluctuation is about 115 °C in a cycle. At same time, a low reverse measurement current ($I_{meas}$) is also applied for junction temperature monitoring in the cooling phase. The specific temperature monitoring methods are as follows [28]: Firstly, a small current is applied (10 mA in this work) from the device's source electrode to drain electrode, and then the conduction voltage drop ($V_{SD}$) between the device's source electrode to drain electrode is measured at different temperatures to obtain the relationship between $V_{DS}$ and temperature. Then, during the power cycle, a small current from the source to the drain is applied to the device again, and $V_{DS}$ is measured. The temperature at this time is calculated based on the relationship between $V_{DS}$ and temperature. The typical junction temperature waveform of DUT during PCT is shown in Fig. 3(c).

## III. RESULTS AND DISCUSSION

### A. THE ELECTRICAL CHARACTERISTICS' FAILURE BEHAVIOR

Fig. 4 exhibits the transfer characteristics and output characteristics of the Cascode GaN device before and after the long-term repetitive PCT. As it can be found that, the device's transfer characteristics and threshold voltages have not changed significantly until 8000-cycle PCT. And after 8000-cycle PCT, there is a significant increase in device off-state current, which demonstrates the formation of a new leakage current channel between the source electrode and drain electrode of the Cascode GaN device. It can also be guessed from that no change in device's threshold voltage, there is no production of new electron traps in the gate region of the cascode GaN device (also is the gate region of the low-voltage *E*-mode Si power device) until 8000-cycle PCT. And the device's on-state current decreases as the increases in cycles number. As shown in Fig. 4(b), the device's on-state current at $V_{DS}$ = 4V and $V_{GS}$ = 4V is decreased by about 4A (about 17%) after 6000-cycle PCT, which may result from the production of new electron traps [2], [3] or the degradation in device's solder layer and bond wire. The new traps with electron trapped will increase negative charges, which will change the energy band structure and decrease the density of two-dimensional electron gas (2DEG), subsequently increasing the on-state resistance and decreasing its on-state current. The delamination of the solder layer and liftoff of the bond wire will also increase the on-state resistance, subsequently decreasing its on-state current. The GaN HEMT is a planar integrated device, the solder layer under GaN HEMT is only used to fix devices and increase its heat dissipation capacity. The causes for the decrease in the device's on-state current may be the production of new electron traps, delamination of the solder layer under the low-voltage *E*-mode Si power device or the degradation in device's bond wire. The specific reasons for the decrease in the device's on-state current will be analyzed later.

Fig. 5 exhibits the gate-to-source leakage current and drain-to-source leakage current of the Cascode GaN device before and after the long-term repetitive PCT. As it can be found, there is no change in the device's gate-to-source leakage even after 8000-cycle PCT, but there is a significant increase in the device's drain-to-source leakage. So, it can be inferred that the gate structure of the cascode GaN device (also is the gate structure of the low-voltage *E*-mode Si power device) is not damaged during the long-term repetitive PCT. And there is a new leakage current channel between the source electrode and drain electrode of the Cascode GaN device, which also results in the increase in the reverse conduction current, as shown in third quadrant *I*–*V* characteristics of the Cascode GaN device (Fig. 6). It can be seen from Fig. 1(a), there are two current paths between the source electrode and drain electrode of the Cascode GaN device. One is from the source electrode to the gate region and drain electrode of the low-voltage *E*-mode Si power device, and then to the drain electrode of the Cascode GaN device, the other is from the source electrode to the gate of the high-voltage *D*-mode GaN HEMT, and then to the drain electrode of the Cascode GaN device. As analyzed above, the gate structure of the low-voltage *E*-mode Si power device is not damaged during the long-term repetitive PCT. So, the new leakage current channel is passed through the gate of the high-voltage *D*-mode GaN HEMT.

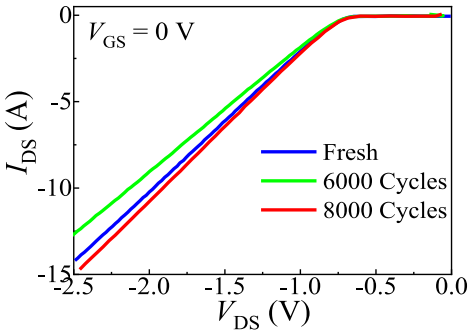


**FIGURE 6.** The third quadrant *I–V* characteristics of the Cascode GaN device before and after PCT.

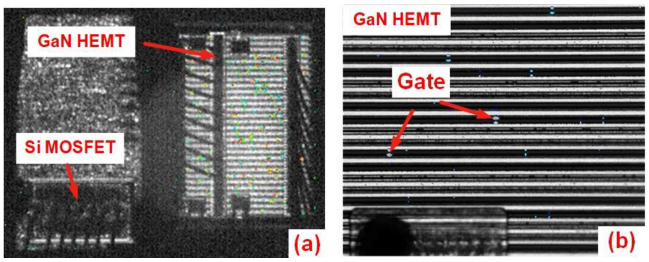


**FIGURE 7.** EMMI images of the Cascode GaN device after 8000-cycle PCT.

To verify the above conjecture, the TCAD simulation and emission microscope (EMMI) analysis have been carried out. As shown in Fig. 7, the EMMI images of the Cascode GaN device after 8000-cycle PCT have shown that there are many light spots on the gate edge of the high-voltage *D*-mode GaN HEMT, while no light spots on the gate region of the low-voltage *E*-mode Si power device, which demonstrates that there is a leakage current channel at the gate region of the high-voltage *D*-mode GaN HEMT. So, the increase in device's drain-to-source leakage results from the structural damage in the gate region of the high-voltage *D*-mode GaN HEMT. The TCAD simulated results show that there is massive heat accumulation under the gate edge of GaN HEMT during the on state, which will result in a hot spot and strong thermal stress under gate edge of device. If the device is subjected to this strong thermal stress for a long time, its gate insulator and AlGaN barrier at the gate edge may suffer degradation, such as the production of new electron traps. As the new electron trap gradually increases, the device's gate insulator is gradually damaged, and the new leakage current channel in the gate region of the high-voltage *D*-mode GaN HEMT will come into being. That is to say, the TCAD simulated results can also demonstrate the gate structure of the high-voltage *D*-mode GaN HEMT will be damaged during the long-term repetitive PCT. On the other hand, before the formation of a new leakage current channel in the gate region of the high-voltage *D*-mode GaN HEMT, the production of new electron traps at the gate region of the high-voltage *D*-mode GaN HEMT will decrease the 2DEG density, which will increase the on-state resistance and decrease device's on-state current, as shown in Fig. 4(b). So, the production of new electron traps is one of the reasons for the decrease in the device's on-state current.

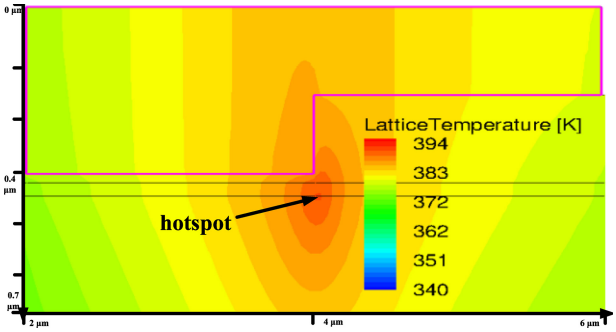


**FIGURE 8.** The heat distribution in GaN HEMT during the on state. The device's gate length, gate-to-source distance and gate-to-drain distance are 2, 1 and 10 $\mu$m, respectively. The applied gate voltage and drain voltage of D-mode AlGaN/GaN HEMT are 0V and 2V, respectively.

### *B. THE PACKAGE-LEVEL DEGRADATION BEHAVIOR*

The package-level degradation behavior of the Cascode GaN device mainly involves the delamination of the solder layer and liftoff of the bond wire. By observing the device after unpacking, the bond wire of the Cascode GaN device did not fall off. And the delamination of the solder layer of the Cascode GaN device will affect the device's thermal characteristics, such as leading to the increase in the device's thermal resistance, which will increase the device's working temperature. To verify if the package-level degradation has occurred, the operating temperature of the device can be tested. Since some device's static parameters are strong related to the temperature, which can be used as temperature sensitive electric parameter (TSEP) to monitor the device's working temperature. For the Cascode GaN device, its reverse voltage drop ($V_{SD}$) in low current is widely accepted for its good sensitivity. So, in this work, the device's junction temperature is monitored through measuring its $V_{SD}$ over the PCT. To determine the relationship between $V_{SD}$ and the device's junction temperature, related calibration is required. In this work, the periodic calibrations between $V_{SD}$ and the device's junction temperature are carried out at the $V_{gs}$ = –5 V and $I_{meas}$ = 10 mA, and the results are given in Fig. 9 (a). Thanks to the low current density of $I_{meas}$, the relationship between device's $V_{SD}$ and temperature in this work is not changed a lot. Fig. 9 shows that the on-line monitored junction temperature of DUT is increased with the increase in cycle number, which implies the increase in the thermal resistance.

To verify the above conjecture, the Cascode GaN device's thermal resistance has been detected before and after the long-term repetitive PCT. The testing process for device thermal resistance is as follows: 1) Selecting appropriate temperature sensitive parameters and calibrate their temperature relationship; 2) Obtaining transient temperature response curve; 3) Obtaining thermal impedance response curve; 4) Obtaining time constant spectrum; 5) Obtaining

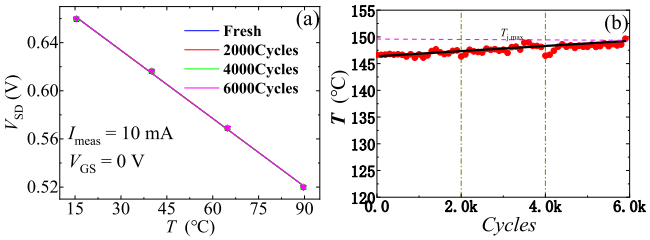


**FIGURE 9.** **(a) Variations of the calibrating results (where dots mean the testing date at various calibrating temperature along with lines referring to linear fitting results corresponding to the dots) regarding reverse voltage drop versus temperature. (b) The junction temperature.**

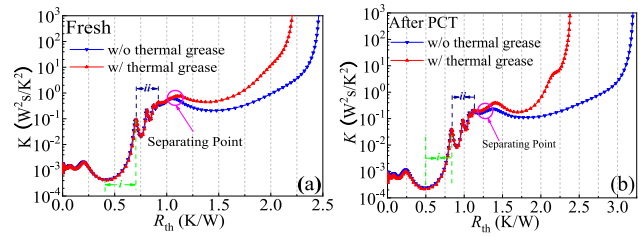


**FIGURE 10.** **The thermal resistance ($R_{th}$) of the Cascode GaN device before (a) and after (b) the long-term repetitive PCT. The thermal grease is evenly applied between the device and the cold plate.**

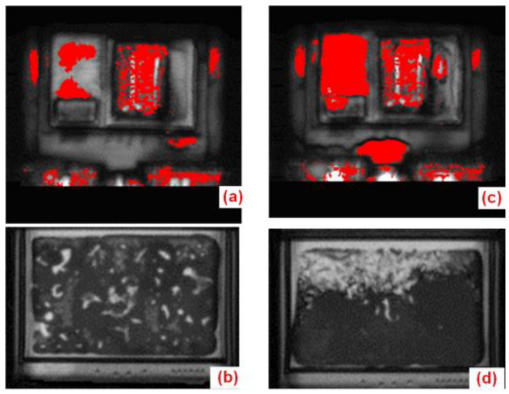


**FIGURE 11.** **(a) Images from the SAM analysis before (a)/(b) and after (c)/(d) the long-term repetitive PCT, (a)/(c) topside of DUT, (b)/(d) backside of the Cascode GaN device. The red area in (a) and (c) represents the structural deformation between materials, the black/dark gray area of (b) and (d) indicates good bonding of the solder, and the white/light gray area of (b) and (d) indicates voids in the solder.**

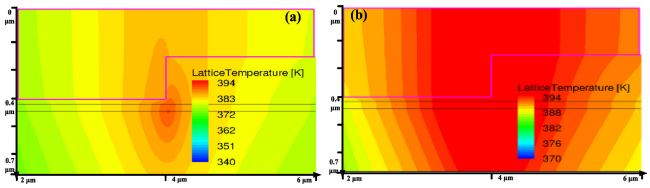


**FIGURE 12.** **The heat distribution in the high-voltage D-mode GaN HEMT during the on state: (a) Low thermal resistance (1.05 K/W), (b) High thermal resistance (1.25 K/W).**

thermal parameters in the Foster model through fitting; 6) Transforming to obtain thermal parameters in the Cauer model; 7) Drawing structural functions based on the thermal parameters of the Cauer model; 8) Obtaining two different structural functions under two different heat dissipation conditions; 9) Determining thermal resistance based on separation points of structural functions. As described in testing process, the different heat dissipation conditions will lead to different structural functions. Before the separating point, it is mainly the heat dissipation characteristics of the device. And after the separating point, it is mainly the heat dissipation characteristics of the environment. So, the separating point represents the thermal resistance of the device. As shown in Fig. 10, the Cascode GaN device's thermal resistance is increased from 1.05 K/W to 1.25 K/W after the long-term repetitive PCT.

To verify the delamination of the solder layer, the scanning acoustic microscope (SAM) analysis has been carried out before and after the long-term repetitive PCT. As shown in the SAM analysis (Fig. 11), there is large area delamination between chip and substrate for the device after the long-term repetitive PCT. The delamination of the solder layer under the low-voltage *E*-mode Si power device will not only lead to the increase in the device's thermal resistance, but also result in the decrease in the device's on-state current. Due to that the high-voltage *D*-mode GaN HEMT is a planar integrated device, the delamination of the solder layer under the high-voltage *D*-mode GaN HEMT will lead to the increase in the device's thermal resistance. So, after the long-term repetitive PCT, there are both the chip-level and package-level degradation for the Cascode GaN device. The package-level degradation (the delamination of the solder layer) will lead to the increase in the thermal resistance, and the chip-level degradation will result in the decrease in the device's on-state current and a significant increase in drain-to-source leakage.

To clarify the relationship between the chip-level and package-level degradation for Cascode GaN device under long-term repetitive power cycling stress, the TCAD simulation has been carried out. As shown in Fig. 12, the increase in the thermal resistance due to the package-level degradation will lead to the increase in the heat accumulation, which will result in increase in the maximum junction temperature, subsequently leading to the chip-level degradation (such as the structural damage in the gate region of the high-voltage *D*-mode GaN HEMT) and electrical performance degradation for the Cascode GaN device. That is to say, the package-level degradation will accelerate the electrical performance degradation for the Cascode GaN device under long-term repetitive power cycling stress.

## IV. CONCLUSION

In this work, the electrical characteristics' failure behavior due to the chip-level damage and its relationship with the package-level degradation have been investigated for the cascode GaN device under long-term repetitive PCT. It is found that, the gate structure of the cascode GaN device (also is the gate structure of the low-voltage *E*-mode Si power device)

is not damaged during the long-term repetitive PCT, but the gate structure of the high-voltage *D*-mode GaN HEMT is damaged after 8000-cycle PCT, which has been verified by TCAD simulation and EMMI analysis. Then, it is also found that the device's thermal resistance is increased after the repetitive power cycling test, which is due to the package-level degradation. The increased thermal resistance will lead to the increase in the heat accumulation, which has been verified by TCAD simulation, subsequently leading to the chip-level damage and electrical performance degradation for cascode GaN device. The relevant results may help improve the long-term reliability of cascode GaN device.

## REFERENCES

[1] N. M. Shrestha, Y. Li, T. Suemitsu, and S. Samukawa, "'Electrical characteristic of AlGaN/GaN high-electron-mobility transistors with recess gate structure," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1694–1698, Apr. 2019.

[2] Y. Shi et al., "Investigation on the long-term reliability of high-voltage p-GaN HEMT by repetitively transient overcurrent," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5322–5328, Dec. 2018.

[3] Y. Shi et al., "Normally off GaN-on-Si MIS-HEMTs fabricated with LPCVD-SiNx passivation and high-temperature gate recess," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 614–619, Feb. 2016.

[4] W. Chen, K.-Y. Wong, and K. J. Chen, "Single-chip boost converter using monolithically integrated AlGaN/GaN lateral field-effect rectifier and normally off HEMT," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 430–432, May 2009.

[5] Y. C. Liang, R. Sun, Y.-C. Yeo, and C. Zhao, "Development of GaN monolithic integrated circuits for power conversion," in *Proc. IEEE CICC*, 2019, pp. 1–4.

[6] X. Li et al., "200 V enhancement-mode p-GaN HEMTs fabricated on 200 mm GaN-on-SOI with trench isolation for monolithic integration," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 918–921, Jul. 2017.

[7] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN/$Al_xGa_{1-x}N$ heterojunction," *Appl. Phys. Lett.*, vol. 63, no. 9, pp. 1214–1215, 1993.

[8] M. A. Khan, J. N. Kuznia, D. T. Olson, and W. Schaff, "Microwave performance of a 0.25 $\mu$m gate AlGaN/GaN heterostructure field effect transistor," *Appl. Phys. Lett.*, vol. 65, no. 9, pp. 1121–1123, 1994.

[9] Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbaars, and U. K. Mishra, "Measured microwave power performance of AlGaN/GaN MODFET," *IEEE Electron Device Lett.*, vol. 17, no. 9, pp. 455–457, Sep. 1996.

[10] S. Huang et al., "High uniformity normally-off GaN MIS-HEMTs fabricated on ultra-thin-barrier AlGaN/GaN heterostructure," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1617–1620, Dec. 2016.

[11] T. F. Chang et al., "Phenomenon of drain current instability on p-GaN gate AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 339–345, Feb. 2015.

[12] G. Greco, F. Iucolano, S. D. Franco, C. Bongiorno, A. Patti, and F. Roccaforte, "Effects of annealing treatments on the properties of Al/Ti/p-GaN interfaces for normally off p-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2735–2741, Jul. 2016.

[13] C. Chen et al. "Fabrication of enhancement-mode AlGaN/GaN MISHEMTs by using fluorinated $Al_2O_3$ as gate dielectrics," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1373–1375, Oct. 2011.

[14] D. Song et al., "Normally off AlGaN/GaN low-density drain HEMT (LDD-HEMT) with enhanced breakdown voltage and reduced current collapse," *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 189–191, Mar. 2007.

[15] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: From depletion mode to enhancement mode," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2207–2215, Sep. 2006.

[16] R. Wang, Y. Cai, C.-W. Tang, K. M. Lau, and K. J. Chen, "Enhancement-mode $Si_3N_4$/AlGaN/GaN MISHFETs," *IEEE Electron Device Lett.*, vol. 27, no. 10, pp. 793–795, Oct. 2006.

[17] X. Wang et al., "Atomic layer deposition of $Sc_2O_3$ for passivating AlGaN/GaN high electron mobility transistor devices," *Appl. Phys. Lett.*, vol. 101, no. 23, 2012, Art. no. 232109.

[18] J. Ren et al., "A novel 700 V monolithically integrated Si-GaN cascoded field effect transistor," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 394–396, Mar. 2018.

[19] S. Huang et al., "High RF performance enhancement-Mode Al2O3/AlGaN/GaN MIS-HEMTs fabricated with high-temperature gate-recess technique," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 754–756, Aug. 2015.

[20] Q. Zhou et al., "High-performance enhancement-mode $Al_2O_3$/AlGaN/GaN-on-Si MISFETs with 626 MW/cm$^2$ figure of merit," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 776–781, Mar. 2015.

[21] Y. Wang et al., "High-performance normally-off $Al_2O_3$/GaN MOSFET using a wet etching-based gate recess technique," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1370–1372, Nov. 2013.

[22] B. Hu et al., "Failure and reliability analysis of a SiC power module based on stress comparison to a Si Device," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 727–737, Dec. 2017.

[23] "Qualification of power modules for use in power electronics converter units in motor vehicles," Eur. Center Power Electron., Nuremberg, Germany, ECPE Guideline AQG, Rep. 324, 2019.

[24] T. Herrmann, M. Feller, J. Lutz, R. Bayerer, and T. Licht, "Power cycling induced failure mechanisms in solder layers," in *Proc. Eur. Conf. Power Electron. Appl.*, Aalborg, Denmark, Sep. 2007, pp. 1–7.

[25] R. Amro, "Packaging and interconnection technologies of power and future trends," *World Acad. Sci. Eng. Technol.*, vol. 49, pp. 691–694, Jan. 2009.

[26] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.

[27] B. Ji, X. Song, E. Sciberras, W. Cao, Y. Hu, and V. Pickert, "Multiobjective design optimization of IGBT power modules considering power cycling and thermal cycling," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2493–2504, May 2015.

[28] C. Herold, J. Sun, P. Seidel, L. Tinschert, and J. Lutz, "Power cycling methods for SiC MOSFETs," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, 2017, pp. 367–370.