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Leakage Current Behavior in $HfO_2/SiO_2/Al_2O_3$ Stacked Dielectric on 4H-SiC Substrate

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ABSTRACT In this study, we investigate the deposition of high-k dielectric materials, namely Al_2O_3 and HfO_2, using atomic layer deposition for 4H-SiC metal-oxide-semiconductor applications. C-V measurements reveal that the $HfO_2/SiO_2/Al_2O_3$/4H-SiC structure exhibits lower interface state density (Dit) and a reduced number of fixed interface trap charges (Neff) than the $HfO_2/Al_2O_3/SiO_2$/4H-SiC structure. Furthermore, we observe significant degradation of the interface properties when annealing at 400 °C compared with 300 °C, as evidenced by atomic force microscopy images. Transmission electron microscopy analysis shows that the SiO_2/SiC surface is inhomogeneous and contains carbon clusters, while the Al_2O_3/SiC interface displays a more uniform structure. The I-V curves demonstrate a reduced leakage current for the high-k dielectric stacked structure to (10^{-11} A/cm^2), and the breakdown electric field of the $HfO_2/SiO_2/Al_2O_3$/4H-SiC structure reaches 9.6 MV/cm.

INDEX TERMS High-k dielectric, 4H-SiC, atomic force microscopy, transmission electron microscopy, dielectric breakdown field.

I. INTRODUCTION

Silicon carbide (SiC) possesses remarkable physical and electrical properties, such as a wide band gap, high critical breakdown electric field, and high thermal conductivity [1], [2], [3]. These properties make it a highly promising material for applications requiring high power, high frequency, and resistance to elevated temperatures [4], [5]. Traditionally, SiO_2 has been employed as the gate dielectric material for in metal-oxide-semiconductor field-effect transistors (MOSFETs), as it exhibits excellent insulation properties and a relatively stable interface state [6], [7], [8]. However, in SiC MOSFETs, the presence of a large number of interface traps at the SiO_2/SiC interface leads to significant challenges, including a low channel mobility, excessive gate leakage, and poor gate reliability in conventional thermally oxidized SiO_2 SiC MOSFET devices [9], [10], [11], [12]. Consequently, as the demand for enhanced device reliability increases, the adoption of high-k dielectrics has emerged as a critically important solution [13], [14], [15], [16].

By increasing the physical thickness, a high-*k* dielectric can achieve the same capacitance as SiO_2 while reducing the leakage current and increasing the breakdown electric field of The MOSFET. The gate dielectric layer using a high-*k* material requires a high dielectric constant, significant conduction band deviation, valence band deviation, and excellent thermal stability [15]. Among the various high-*k* dielectric materials, HfO_2 stands out as the most suitable candidate due to its high dielectric constant (k = 25) and good thermal stability [17], [18], [19]. However, the small conduction band energy (E_c) of HfO_2 in combination with SiC leads to electrons in the substrate experiencing a high electric field, which can change the characteristics of the gate dielectric and compromise device reliability through phenomena such as hot carrier injection or trap-assisted tunneling [20], [21]. To mitigate these issues, the addition of a SiO_2 layer between the high-k dielectric and SiC has been proven to reduce the leakage current [22], [23], [24]. Al_2O_3 has garnered significant attention as a gate dielectric material due to its wide band gap (7-8.8 eV), high breakdown field (10-13 MV/cm), and favorable interface characteristics [25], [26], [27], [28], [29]. Lo Nigro et al. [30] investigated the structural characteristics and dielectric performance of

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nanolayered Al_2O_3/HfO_2 thin films using plasma-enhanced atomic layer deposition (PEALD) technique. Recent research on gate dielectric stacks has predominantly focused on double-layer structures [31], [32], [33]. There have been studies on the influence of additional stress on the surface of metal-oxide- semiconductor (MOS) capacitors electron trapping [34]. However, studies on multi-layer structures are relatively scarce, employing a multi-layer structure can not only provide a high dielectric constant but also result in interface state improvements.

This paper focuses on investigating the HfO_2/SiC structure using a transition layer consisting of high-conduction-band Al_2O_3 and SiO_2. Two stacked dielectric configurations were examined: $HfO_2/Al_2O_3/SiO_2$/4H-SiC and $HfO_2/SiO_2/Al_2O_3$/4H-SiC. The performance improvement and advantages of these structures with respect to the traditional SiO_2/4H–SiC structure were analyzed through electrical measurements such as I-V and C-V characterizations, in comparison with the traditional SiO_2/4H-SiC structure. Furthermore, a microscopic perspective was employed to analyze the MOS capacitors with the stacked structure. Physical characterization measurements using techniques such as atomic force microscopy (AFM) and high-resolution transmission electron microscopy (TEM) were conducted.

II. EXPERIMENTAL PROCEDURE

In this experiment, N-type Si-surface 4H-SiC epitaxial wafers with a thickness of approximately 10 μm and a dopant concentration of 9.85×10^{15} cm^{-3} were utilized to prepare stacked dielectric MOS capacitors. The wafer surface was initially subjected to a standard RCA process to eliminate any contaminants and impurities. A 200-nm-thick Ni film was then sputtered on the back of the sample, and the sample was subjected to rapid thermal annealing at 1000 °C for 2 min under N_2 gas flow to establish an ohmic contact. To protect the electrodes, a 20-nm-thick Ti layer and a 50-nm-thick Au layer were sputtered on top of the Ni metal film. Prior to growing the dielectric film, the front side of the wafer was rinsed with a buffered oxide etchant (BOE) to remove the oxide layer. Subsequently, atomic layer deposition (ALD) was employed to deposit a 2-nm-thick Al_2O_3 dielectric film at 350 °C. Next, another ALD process was carried out at 300 °C to grow a 2-nm-thick SiO_2 dielectric film, which was then followed by the deposition of a 50-nm-thick HfO_2 film at 300 °C. The gate dielectric capacitor underwent a post-dielectric annealing (PDA) treatment in N_2 atmosphere at annealing temperatures of 300 °C and 400 °C for an annealing time of 30 min. Finally, a 200-nm-thick Al metal film was sputtered on the front of the sample to serve as an electrode. This completed the fabrication of the HfO_2 (50 nm) /SiO_2 (2 nm) /Al_2O_3 (2 nm) /4H-SiC structure.

For the purpose of comparison, MOS capacitors with stacked SiO_2 (50 nm) / 4H-SiC and HfO_2 (50 nm) / Al_2O_3 (2 nm) / SiO_2 (2 nm) / 4H-SiC dielectric structures were fabricated. In the case of the traditional SiO_2 MOS capacitor structure, the SiO_2 dielectric film was grown

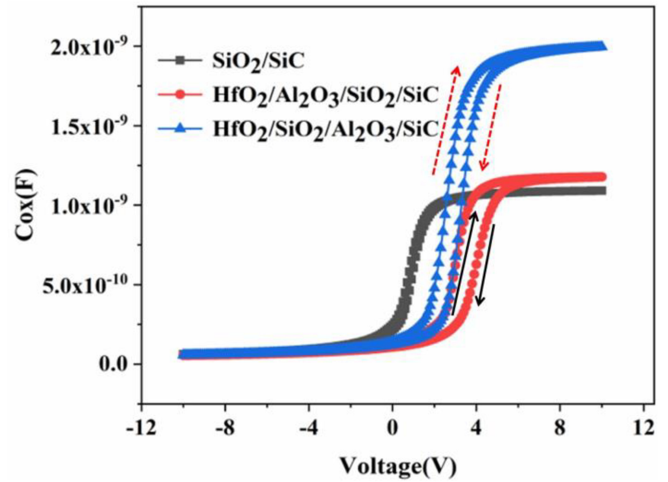

FIGURE 1. C-V curves of different stacked dielectric structures at 300°C annealing.

utilizing dry-oxygen thermal oxidation. The oxidation process involved subjecting the sample to thermal oxidation at a temperature of 1150 °C for 6 h, resulting in the growth of an oxide layer with a thickness of 50 nm.

III. RESULTS AND DISCUSSIONS

The MOS charge system consists of four types of charges. Among these, the trapped oxide layer (N_{ot}) contributes to the hysteresis voltage (V_{hy}), while the effective fixed charge density (N_{eff}) is primarily responsible for the shift in the flat band voltage (V_{fb}) [35]. Figure 1 illustrates the high-frequency capacitance-voltage (C-V) hysteresis curve of the different stacked samples (after being annealed at 300 °C) at a frequency of 1MHz. During the test, the voltage is swept from negative to positive and then from positive to negative.

By observing the results, it is evident that the SiO_2/4H-SiC MOS capacitor grown solely through thermal oxidation exhibits smaller V_{fb} and V_{hy} values, indicating that a high-quality SiO_2 dielectric film was obtained through thermal oxidation. However, when the upper 50-nm-thick SiO_2 layer is replaced with the HfO_2 dielectric film grown using ALD and when 2-nm-thick SiO_2 and Al_2O_3 films grown via ALD are inserted, both the hysteresis voltage and the flat band voltage experience a slight increase. Nonetheless, in comparison to the contact between the SiO_2 film and SiC ($HfO_2/Al_2O_3/SiO_2$/ 4H-SiC), the contact between the Al_2O_3 film and SiC ($HfO_2/SiO_2/Al_2O_3$/4H-SiC) displays smaller V_{fb} and V_{hy} values. This finding suggests that the Al_2O_3 dielectric film exhibits favorable interface characteristics.

Table 1 presents the calculated values of ΔV_{fb}, V_{hy}, and the interface state density (D_{it}) obtained through the analysis of the high-frequency C-V curves. The experimentally determined D_{it} value falls within the widely accepted energy level of E_c-0.2 eV [18], [36]. It can be observed that the hysteresis voltage of the MOS stacked MOS structure increases with the rise in the flat band voltage. This is attributed to the fact that while all four types of charges in the MOS system contribute to the shift in the flat band voltage, only

TABLE 1. Parameters of different stacked dielectric structures at 300°C annealing.

Sample	C_{ox} (nF)	ΔV_{fb} (V)	V_{hy} (V)	N_{ot} ($\times 10^{11}$ cm^{-2})	N_{eff} ($\times 10^{12}$ cm^{-2})	D_{it} at E_C-0.2eV ($\times 10^{12} cm^{-2}eV^{-1}$)
SiO_2/4H-SiC	1.09	0.18	0.1	0.86	0.27	2.28
$HfO_2/Al_2O_3/SiO_2$/4H-SiC	1.17	2.86	0.9	8.71	3.36	5.23
$HfO_2/SiO_2/Al_2O_3$/4H-SiC	1.99	2.08	0.6	8.38	2.88	4.43

the effective fixed charge density significantly affects the hysteresis voltage. During the growth process of the dielectric layer, the presence of defects can lead to the generation of an effective fixed charge density, as they become charged through ionizing radiation and act as trapping sites [37]. The accumulation of a substantial number of oxide trap charges has two main effects. Firstly, it increases the number of traps that can be filled and emptied by electrons, thereby augmenting the hysteresis voltage. Secondly, it effectively increases the equivalent charge density of the oxide layer, subsequently influencing the flat band voltage [38].

Specifically, the deposition process of the dielectric introduces uncharged oxide traps. When a voltage is applied to the gate dielectric, a significant number of electrons tunnel from the substrate and migrate to the gate dielectric layer to fill the released oxide traps. This process results in a deviation of the flat band voltage. Furthermore, it is worth noting that the ALD-grown transition layer consisting of SiO_2 and Al_2O_3 introduces a higher number of oxide trap charges, leading to an increase in both the flat band voltage and the hysteresis voltage.

The N_{eff} in the MOS system primarily contributes to the shift in the flat band voltage and the modification of the boundary trap density. N_{eff} represents the net effective number of charges per unit area at the interface (number/cm^2). The corresponding net effective charge Q_{eff} (C/cm^2) is negative. In Table 1, the variation in the fixed interface trap density corresponds to the changes observed in the oxide trap density. Specifically, as the voltage increases, both trap densities exhibit an upward trend.The flat band voltage characterizes the presence of negative charges in the dielectric layer, and this experimental result indicates a significant reduction in negative charges, predominantly in the form of oxygen vacancies. Oxygen vacancies can capture one or two electrons, forming negative oxygen vacancies and leading to a shift in the flat band voltage [39]. During the ALD growth of the transition dielectric layer and the annealing process of the $HfO_2/Al_2O_3/SiO_2$/4H-SiC and $HfO_2/SiO_2/Al_2O_3$/4H-SiC at 300 °C, the number of oxygen vacancies in the dielectric layer increases, resulting in an augmentation of the negative charges. Consequently, a shift in the flat band voltage occurs, accompanied by an increase in the density of the fixed interface traps. It is also noteworthy that the $HfO_2/Al_2O_3/SiO_2$/4H-SiC MOS capacitor exhibits the highest interface state density. The trend of the interface state density is in good agreement with the trend of the hysteresis voltage. The greater the hysteresis voltage, the higher the density of the oxide trap charges, and the larger the interface state density.

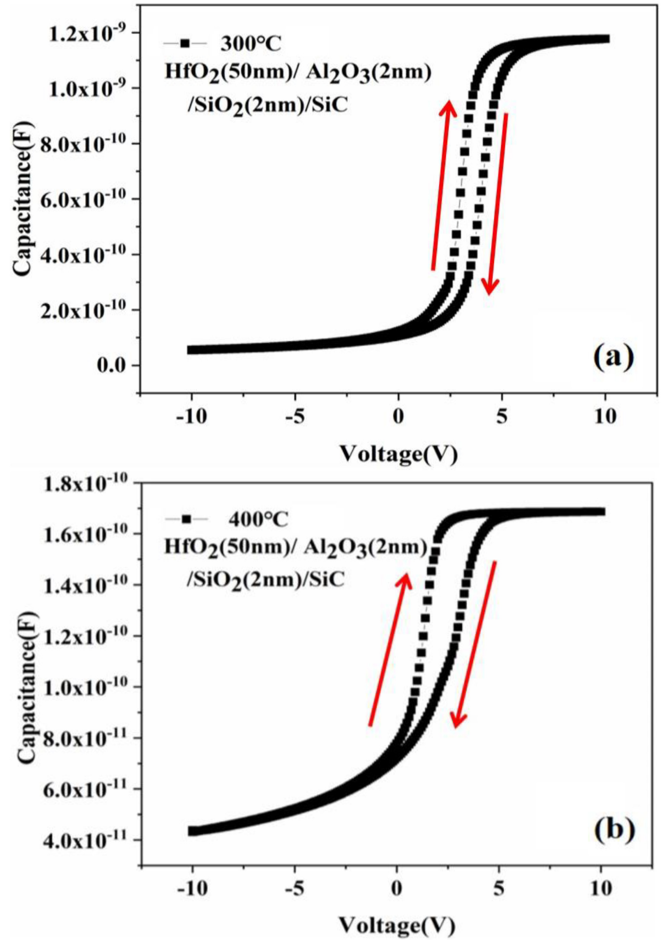

FIGURE 2. C-V curves of $HfO_2/Al_2O_3/SiO_2$/4H-SiC at (a) 300°C and (b) 400°C annealing.

However, it is important to acknowledge that the increases in the oxide trap charge density, boundary trap density, and interface state density are relatively small, as there may be some errors associated with the growth conditions of the process. Subjecting the dielectric to an annealing process can improve the interface characteristics to some extent [40], [41]. Therefore, the stacked $HfO_2/Al_2O_3/SiO_2$/4H–SiC and $HfO_2/SiO_2/Al_2O_3$/4H–SiC dielectric structures were subjected to annealing at 400 °C. Figure 2 depicts the C–V curve of the stacked $HfO_2/Al_2O_3/SiO_2$/4H–SiC MOS dielectric structure, comparing the annealing processes at 300 °C and 400 °C. It is evident from the curve that after annealing at 400 °C, both the hysteresis voltage and the flat-band voltage are higher than those obtained after annealing at 300 °C. Additionally, D_{it} increases to 5.74×10^{12} $cm^{-2}eV^{-1}$.

Similar conclusions can be drawn by observing the C-V curves of the $HfO_2/SiO_2/Al_2O_3$/4H-SiC MOS structure annealed at 300 °C and 400 °C, as shown in Figure 3. This phenomenon can be attributed to two possible causes.

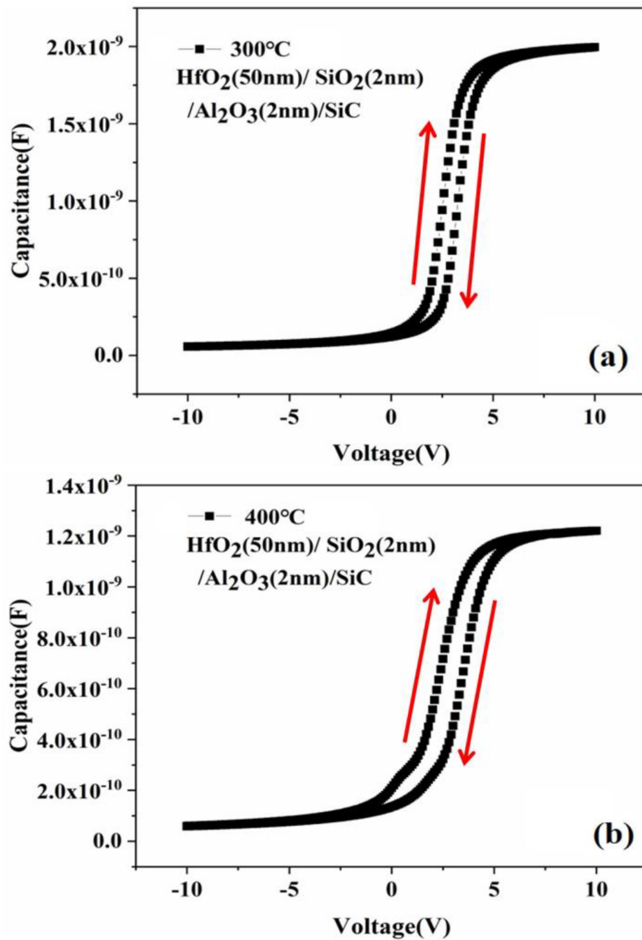

FIGURE 3. C-V curves of $HfO_2/SiO_2/Al_2O_3$/4H-SiC at (a) 300°C and (b) 400°C annealing.

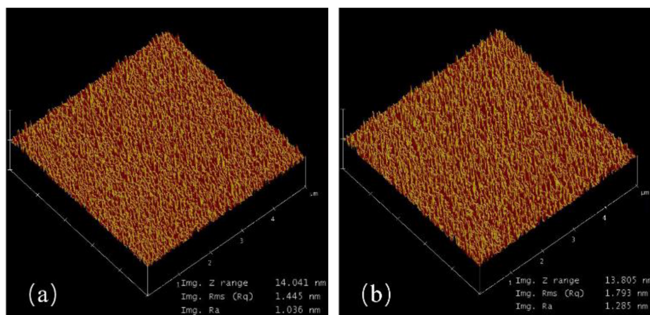

FIGURE 4. AFM image of $HfO_2/SiO_2/Al_2O_3$/SiC at (a) 300°C and (b) 400°C annealing.

Firstly, at the higher annealing temperature of 400 °C, the Al_2O_3 or SiO_2 dielectric film reacts with SiC at the interface, leading to the introduction and generation of more oxygen vacancies as well as an increase in the interface trap density. Secondly, it is also possible that the temperature of 400 °C exceeds the crystallization temperature of HfO_2, resulting in the formation of leakage paths and the introduction of more defects [20]. Therefore, the temperature of 300 °C is considered to be the most suitable annealing temperature for the stacked dielectric structure.

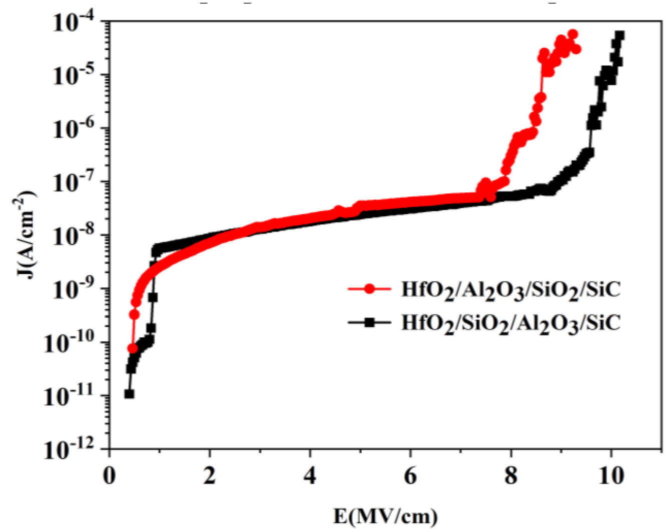

FIGURE 5. J-E curves of different stacked dielectric structures at 300°C annealing.

Figure 4 presents the AFM surface morphology of the stacked $HfO_2/SiO_2/Al_2O_3$/4H-SiC structure annealed at 300 °C and 400 °C. It can be observed that the surface of the HfO_2 thin dielectric film is not very smooth when annealed at 300 °C, and after annealing at 400 °C, there are noticeable convex regions on the surface. However, it is also evident that the surface distribution remains relatively homogeneous. Based on the AFM measurement results, the root mean square (RMS) roughness values for the HfO_2 thin dielectric film dielectric annealed at 300 °C and 400 °C are 1.445 and 1.793 nm, respectively.

The main factors that affect the gate leakage current density are the oxide trap density and the boundary trap density, followed by the valence band between the gate dielectric and the silicon carbide or the conduction band; this is because a large valence band or a large conduction band can reduce both the probability of electron tunneling and the barrier height of the tunneling, thereby increasing the gate leakage current density [42]. A higher dielectric constant actually helps the dielectric to maintain a larger electric field. This is a key motivation for using high-k dielectrics. The leakage current is not directly related to the dielectric constant, but it is influenced by the alignment of the energy bands between the dielectric and SiC.

Figure 5 shows the current density (J) as a function of the electric field (E) for the different stacked dielectric structures. The electric field (E) calculated in this experiment is obtained by calculating it after excluding the factor of the experimentally measured flat-band voltage (V_{fb}). It can be seen from the curves that the leakage currents of the $HfO_2/Al_2O_3/SiO_2$/4H-SiC and $HfO_2/SiO_2/Al_2O_3$/4H-SiC structures can reach 10^{-11} A/cm^2. The band gaps of SiO_2 and Al_2O_3 are 8.9 and 9 eV, respectively [9], [43]. The conduction band offsets of SiO_2/SiC and Al_2O_3/SiC are significant, which reduces the likelihood of electrons tunneling through the gate dielectric.

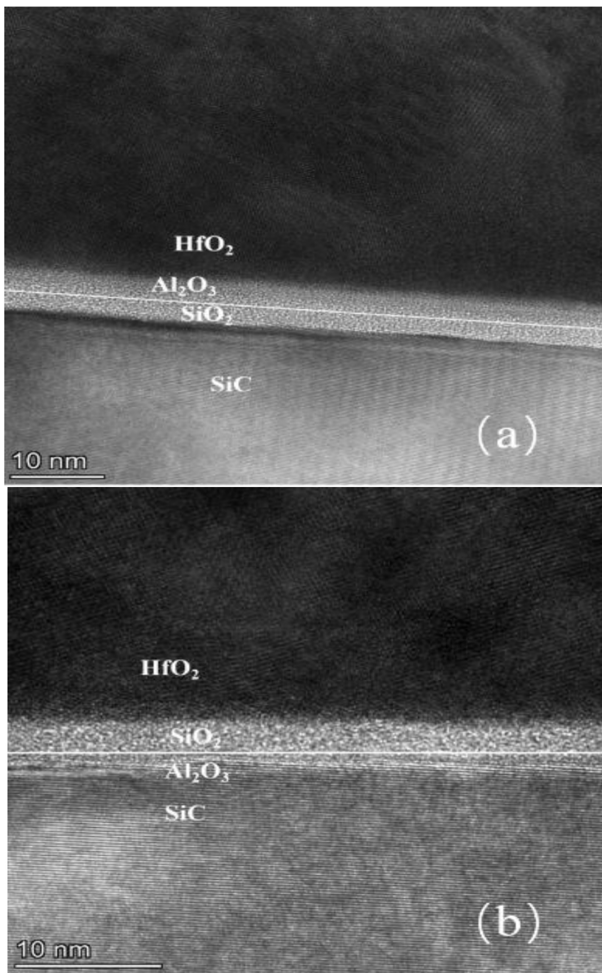

FIGURE 6. TEM of (a) $HfO_2/Al_2O_3/SiO_2$/4H-SiC and (b) $HfO_2/SiO_2/Al_2O_3$/4H-SiC at 300°C annealing.

As a result, the current density of the gate electrode is significantly reduced.

Figure 5 illustrates that the leakage currents of the $HfO_2/Al_2O_3/SiO_2$/4H-SiC and $HfO_2/SiO_2/Al_2O_3$/4H-SiC structures exhibit a sharp increase at an electric field of 1 MV/cm, followed by a plateau. this behavior indicates that the breakdown of the gate dielectric involves the breakdown of the SiO_2 transition layer. Deviation from Fowlern-Nordheim tunneling, once the SiO_2 transition layer breaks down, a conductive channel is formed, resulting in the largest proportion of the gate voltage being applied to the HfO_2 dielectric layer. Consequently, the leakage current after breakdown is primarily determined by the ability of the HfO_2 gate dielectric to impede electron tunneling [18]. The breakdown electric field of the $HfO_2/Al_2O_3/SiO_2$/4H–SiC structure (8.3 MV/cm) is lower than that of the $HfO_2/SiO_2/Al_2O_3$/4H–SiC structure (9.6 MV/cm). One possible reason is that Al_2O_3 exhibits good interface characteristics, and the Al_2O_3/SiC interface possesses a high barrier [27].

Figure 6 displays the TEM images of the $HfO_2/Al_2O_3/SiO_2$/4H–SiC and $HfO_2/SiO_2/Al_2O_3$/4H–SiC structures. In Figure 6(a), it is evident that the SiC/SiO_2 interface is not very uniform. Additionally, the Si atoms in the SiO_2 film react with the SiC material, resulting in the formation of a silicate substance, which can affect the device performance. Furthermore, an inhomogeneous layer of carbon clusters can be observed at the SiC/SiO_2 interface. The presence of carbon cluster impurities contributes to the nonuniformity of the interface and the increased number of interface state traps, consequently leading to a higher interface state density.

On the other hand, the TEM image of the $HfO_2/SiO_2/Al_2O_3$/4H–SiC structure shown in Figure 6(b) reveals that the Al_2O_3/SiC interface does not exhibit black carbon clusters, and the surface is uniform. This suggests that the introduction of the Al_2O_3 layer helps to mitigate the presence of carbon cluster impurities and promotes the formation of a more homogeneous interface.

IV. CONCLUSION

This paper investigated the enhancement of the MOS capacitance of 4H–SiC by depositing Al_2O_3 and HfO_2 high-k dielectrics via ALD. The results revealed that the stacked $HfO_2/SiO_2/Al_2O_3$/4H-SiC structure exhibits a lower interface state density and a reduced number of fixed interface trap charges than the $HfO_2/Al_2O_3/SiO_2$/4H-SiC structure. Furthermore, annealing at 400 °C caused a significant degradation of the interface characteristics, which is likely due to the reaction between the dielectrics and SiC, leading to an increased trap density and the formation of a leakage path. The TEM analysis showed that the SiO_2/SiC interface is inhomogeneous and contains carbon clusters, while the Al_2O_3/SiC interface is more uniform. The I–V curve demonstrated a reduced leakage current for the high-k dielectric stack structure, reaching 10^{-11} A/cm^2. Notably, the breakdown electric field of the $HfO_2/SiO_2/Al_2O_3$/4H-SiC structure reached 9.6 MV/cm, indicating an improved dielectric withstand capability, reduced leakage current, and enhanced device reliability.

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