Received 16 May 2023; revised 25 June 2023; accepted 1 July 2023. Date of publication 7 July 2023; date of current version 26 July 2023.
The review of this article was arranged by Editor A. Nathan.

Digital Object Identifier 10.1109/JEDS.2023.3293232

A High-Voltage Serial-In-Parallel-Out Shift Register With Amorphous Silicon TFTs

YINGBO WEI[1], DONGPING WANG[2] (Member, IEEE), SHENGZHE JIANG[1], HANBIN MA[2,3] (Member, IEEE), AND JUN YU[1] (Member, IEEE)

1 School of Information Science and Engineering, Shandong University, Qingdao 266237, China
2 CAS Key Laboratory of Bio-Medical Diagnostics, Suzhou Institute of Biomedical Engineering and Technology, Chinese Academy of Sciences, Suzhou 215163, China
3 Biochip Application Center, Guangdong ACXEL Micro & Nano Tech Company Ltd., Foshan 528000, China

CORRESPONDING AUTHOR: J. YU (e-mail: jun.yu@sdu.edu.cn)

This work was supported in part by the National Key Research and Development Program of China under Grant 2022YFB3606900; in part by the Major Scientific and Technological Innovation Project in Shandong Province under Grant 2022CXG010504; in part by the Innovation and Entrepreneurship Team of Jiangsu Province under Grant JSSCTD202145; in part by the Science and Technology Innovation Team Project of Foshan, China, under Grant 1920001000047; and in part by the Natural Science Foundation of Shandong Province under Grant ZR2022QF145.

ABSTRACT In this paper, we proposed a high-voltage serial-in-parallel-out (SIPO) shift register based on amorphous silicon thin-film transistors (a-Si TFTs). We provided a detailed introduction of the bootstrap inverter, the key component of the proposed shift register, and presented the simulation and analysis of one-stage and five-stage SIPO shift registers, respectively. Then we fabricated the five-stage SIPO shift registers employing a-Si TFTs. Both the simulation results and experimental results show that the proposed SIPO shift register is capable of transmitting a 50 V high voltage pulse signal with a clock frequency of 20 kHz and is expected to be an important building block for the applications of digital microfluidics.

INDEX TERMS Digital microfluidic (DMF), amorphous silicon thin-film transistor (a-Si TFT), serial-in-parallel-out (SIPO), shift register.

I. INTRODUCTION

In recent years, digital microfluidic (DMF) chips have developed rapidly because of the wide range of prospective applications in biology, chemistry, medicine, and other fields. Electrowetting-on-dielectric (EWOD) has been widely used as a droplet manipulation method in DMF chips [1], [2], [3], [4], [5]. Moreover, in order to solve the problem of the excessive number of DMF chip electrodes required for the improvement of throughput, active matrix electrowetting-on-dielectric (AM-EWOD) technology has been developed as a new DMF architecture [1], [6], [7].

An AM-EWOD DMF chip uses a thin-film transistor (TFT) array to drive the electrodes. This architecture allows a larger electrode array; it also greatly reduces the size of the electrodes and enables precise control over the size and shape of the droplets [6].

The precision of the TFT manufacturing process can reach the micrometer level. This is sufficient to meet the fabrication requirements for most DMF chips. Furthermore, glass substrates used in TFTs have lower fabrication costs and higher production efficiency compared with the silicon substrates used in CMOS.

Currently, there are various kinds of TFTs, such as amorphous silicon (a-Si) TFTs [8], low-temperature polycrystalline silicon (LTPS) TFTs [9], indium-gallium-zinc-oxide (IGZO) TFTs [10], and organic TFTs (OTFTs) [11]. Among these, a-Si TFTs are relatively cost effective and more suitable for mass production. Besides, the a-Si TFTs have better uniformity and stability, thus their performance is sufficient for most DMF chips.

Generally, the working voltage of standard EWOD applications extends up to several tens of volts [7], [12], [13], [14], [15]. Therefore, it is necessary to provide such high voltages for the design of practical AM-EWOD drive circuits.

The purpose of this paper is to report a high-voltage serial-in-parallel-out (SIPO) shift register based on a-Si TFTs. A SIPO shift register can output input serial data in parallel format. Using the shift register to apply driving voltage to the electrodes of the AM-EWOD DMF chips can further reduce the number of driving signals and improve the integration

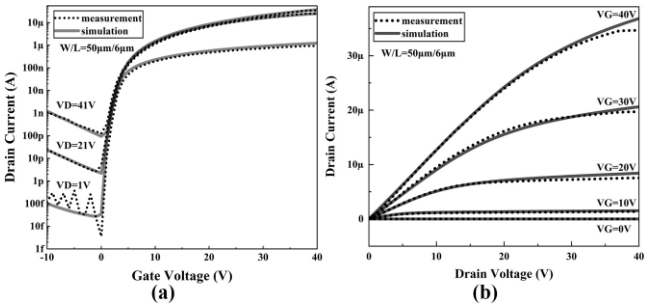

FIGURE 1. (a) Transfer characteristics (ID–VG) of discrete a-Si TFTs with W/L = 50 μm/6 μm and VD varied from 1 to 41 V in 20 V steps. (b) Output characteristics (ID–VD) of the TFT with W/L = 50 μm/6 μm and VG varied from 0 to 40 V in 10 V steps.

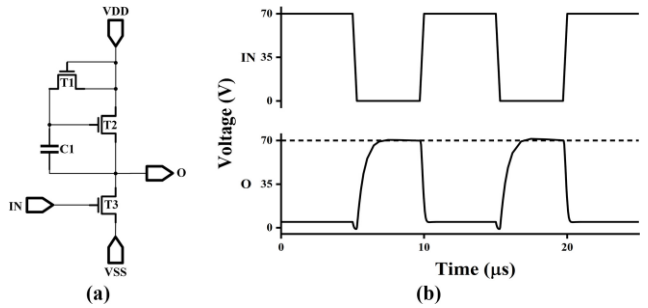

FIGURE 2. Schematics of (a) a bootstrap inverter circuit and (b) its simulation results with a clock frequency of 100 kHz, VDD of 70 V, and VSS of –3 V.

of the chips. In addition, a five-stage SIPO shift register has been proposed and simulated based on the SIPO shift register unit. And then, we fabricate the SIPO shift register employing a-Si TFTs. Both the simulation and experimental results show that the shift register exhibits a 50 V high voltage output pulse and a maximum clock frequency of 20 kHz.

II. CHARACTERISTICS OF A-SI TFTS

Fig. 1 (a) and (b) show the transfer characteristics and output characteristics, respectively, of a typical a-Si TFT (W/L = 50 μm/6 μm) used in the present study. All simulations presented in this paper use the a-Si TFT model as shown in Fig. 1.

III. DESIGN AND SIMULATION

First, we introduce the bootstrap inverter, which is an extremely critical component in our proposed SIPO shift register. The bootstrap inverter, as the name implies, uses the bootstrapping effect of capacitors to raise the output high level [16]. An example of this effect can be seen with the bootstrap inverter shown in Fig. 2(a). Assume that the initial input signal IN is high level VIH, and the initial output signal O is low level VOL. As the gate voltage and drain voltage of T1 are both VDD, T1 is in the saturation state. The source voltage of T1 and the gate voltage of T2 are both VDD-Vth1. Vthn is the threshold voltage of Tn. Therefore, the voltage applied to C1 is VDD-Vth1-VOL. Due to T2 in saturation state and T3 in deep linear state having the same drain current, the VOL can be obtained as follows:

$$0.5\mu C_{OX}\alpha(VDD - Vth1 - VOL - Vth2)^2 = \mu C_{OX}\beta[(VIH - VSS - Vth3)(VOL - VSS)] \quad (1)$$

$$VOL \approx \frac{\alpha(VDD - Vth1 - Vth2)^2}{2\beta(VIH - VSS - Vth3)} + VSS \quad (2)$$

Here, α is the width-to-length ratio of T2; β is the width-to-length ratio of T3; μ is the carrier mobility; and C_{OX} is the gate insulating layer capacitance per unit area.

Therefore, it can be seen from expression (2) that VOL can be adjusted to the required low level by adjusting VSS.

When the input signal IN is low level VIL, T3, which is initially open, is gradually closed, and the voltage of output signal O is gradually increased. As the voltage applied to C1 cannot mutate, the gate voltage of T2 increases gradually based on VDD-Vth1, which is the bootstrapping effect of the capacitor C1. When the gate voltage of T2 increases to VDD + Vth2, T2 changes from the saturation state to the linear state, and the current of T2 in the linear state is equal to the current of T3 in cut-off state, which is equal to zero. Thus, we get:

$$\mu C_{OX}\alpha[(VDD + Vth2 - Vth2 - VOH)(VDD - VOH)] = 0 \quad (3)$$

$$VOH = VDD \quad (4)$$

Therefore, the output signal O becomes high level VOH, which is equal to VDD. This is the key to the ability of our proposed register to transmit high voltages.

Fig. 2(b) shows the simulation waveform of the bootstrap inverter built with our above-mentioned a-Si TFTs. The bootstrap inverter is operated with a clock frequency of 100 kHz, VDD of 70 V, and VSS of –3 V. It can be seen from the simulation waveform that the bootstrap inverter is enough to transmit a 70 V high voltage signal. Its performance is more than enough for our needs.

The proposed SIPO shift register unit circuit is shown in Fig. 3(a). The unit circuit is composed of nine transistors and four capacitors (9T4C). T1, T2, T3, and C1 are the first-stage bootstrap inverter, denoted as I1. Similarly, T4, T5, T6, and C4 constitute the second-stage bootstrap inverter, denoted as I2.

The working process of the proposed SIPO shift register unit circuit can be explained as follows: When the RESET is high level, C4 gets charged to high level, and the gate voltage of T6 is at high level as well; consequently, the output signal O is low level VSS. Thus, as long as RESET is high level, the output signal O will be maintained at low level regardless of CLKA, CLKB, and IN. When the RESET and CLKB are low level and CLKA is high level, the input signal IN registers at a Q-node through I1 in the form of reverse IN, and the output signal O remains unchanged. When the RESET and CLKA are low level and CLKB is high level, the voltage of a Q-node maintains its original level, and the reverse IN stored at the Q-node is the output at O through I2.

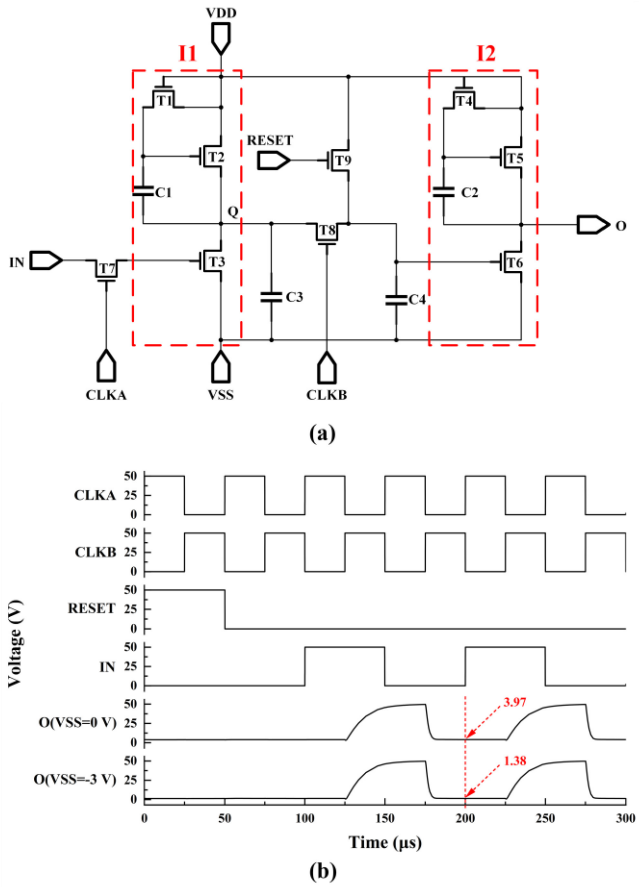

FIGURE 3. Schematics of (a) proposed SIPO shift register unit circuit and (b) its simulation results with a clock frequency of 20 kHz, VDD of 50 V, VSS of 0 V and –3 V, load capacitance of 10 pf and load resistance of 1 GΩ, respectively.

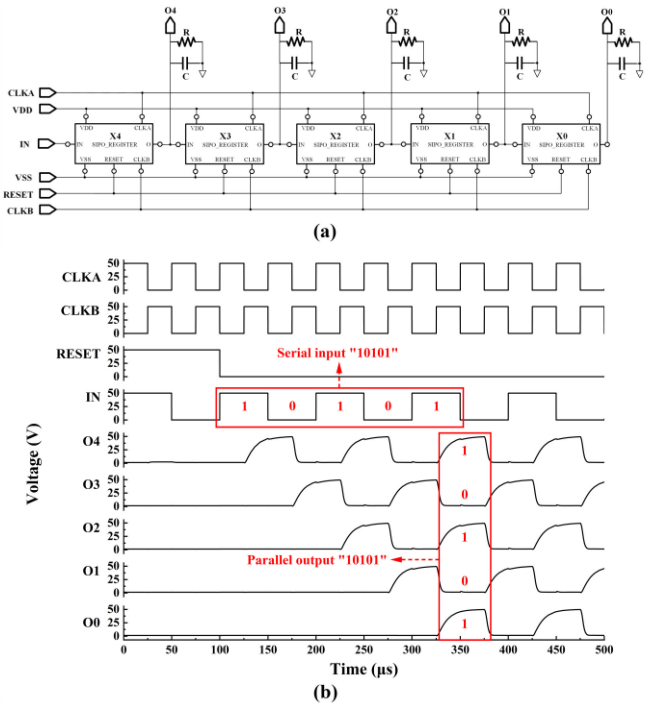

FIGURE 4. Schematics of (a) five-stage SIPO shift register circuit and (b) its simulation results with a clock frequency of 20 kHz, VDD of 50 V, and VSS of –3 V.

The parameters of each component in the proposed SIPO shift register unit circuit are listed in Table 1.

Fig. 3(b) shows the simulation waveform of the proposed SIPO shift register unit circuit. The load capacitance and load resistance during simulation are 10 pf and 1 GΩ respectively. In theory, the low level of output signal O should be approximately equal to VSS. However, the simulation results are not consistent with this. This is due to the working voltage being 50 V, owing to which the interference term $\frac{\alpha(VDD-Vth1-Vth2)^2}{2\beta(VIH-VSS-Vth3)}$ in the expression for calculating VOL cannot be ignored. Therefore, we reduced the low level of output signal O by setting VSS to a negative voltage, such as –3 V, to obtain the desired low level. As indicated by the red arrows in Fig. 3(b), the low level of output signal O drops from 3.97 V to 1.38 V when VSS changes from 0 V to –3 V.

We then built a five-stage SIPO shift register with the proposed SIPO shift register unit, as shown in Fig. 4(a), and conducted its simulation, in which load capacitance C is 10 pF and load resistance R is 10 GΩ. The simulation waveform is shown in Fig. 4(b). When the input signal "10101" is serially input to the five-stage SIPO shift register, the five-stage SIPO shift register outputs the signal "10101" in parallel. This verifies that the five-stage SIPO shift register can realize its functions with a clock frequency of 20 kHz, VDD of 50 V, and VSS of –3 V. However, we found that the intermediate stage shift register units of the five-stage SIPO shift register had a slight drop in the middle of their output signals when the output voltage is high level. This is because when the previous stage shift register transfers its high-level signal to the next stage shift register, it needs to charge the next stage shift register, resulting in a slight drop in the high level of the previous stage shift register. However, this has negligible influence.

IV. EXPERIMENTAL RESULTS

We fabricated the proposed five-stage SIPO shift register employing a-Si TFTs. The channel lengths of all TFTs are 6 μm. The channel widths of TFTs in the proposed shift register are similar as TFTs listed in Table 1.

Fig. 5(a) shows the optical image of the fabricated SIPO shift register. As shown in Fig. 5(b), the test result is slightly different from the simulation. Under the same supply voltage of 50 V and clock frequency of 20 kHz, the waveform of the output signal is as low as about 40 V and cannot reach 50 V. The reason is that there is a large parasitic capacitance at the output of the fabricated SIPO shift register due to the influence of the process and the test electrode will also introduce some capacitance, which results in a larger load capacitance at the output of the circuit, so the output high-voltage-level cannot meet the requirements. But its function of serial input

TABLE 1. Circuit parameters of the SIPO shift register.

Device	Parameter
T1	18 μm/6 μm
T2	18 μm/6 μm
T3	400 μm/6 μm
T4	33 μm/6 μm
T5	33 μm/6 μm
T6	700 μm/6 μm
T7	40 μm/6 μm
T8	200 μm/6 μm
T9	800 μm/6 μm
C1	1 pF
C2	1 pF
C3	1 pF
C4	0.1 pF

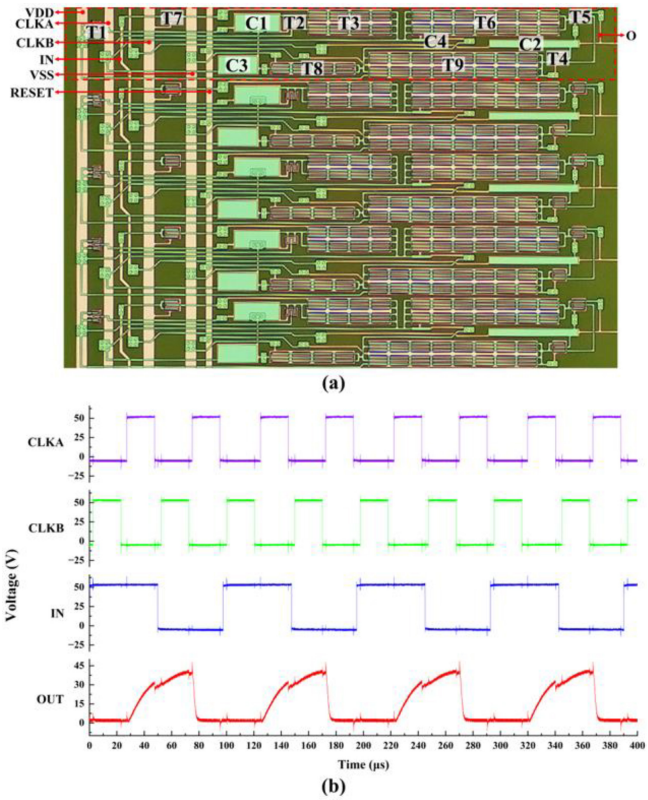

FIGURE 5. (a) Optical image of the fabricated SIPO shift register. (b) Output waveform of the last (five) stage.

and parallel output shift register can be realized. And we can make the output voltage meet our requirements by slightly increasing the power supply voltage.

Table 2 summarizes key factors of the proposed shift register unit circuit in comparison to other previous shift register unit circuits, showing that the proposed circuit can transmit the highest high-voltage-level pulse signal with the mature and cost effective a-Si TFTs. Its clock frequency is higher than the a-IGZO TFT circuit and lower than the LTPS TFT circuit. But the LTPS TFT circuit only has simulation results and has not been fabricated for verification.

TABLE 2. The key factors of the proposed and previous works.

Parameter	[17]	[18]	This work
Active layer	a-IGZO	LTPS	a-Si
Number of TFTs	11	11	9
Number of Capacitors	0	0	4
Number of Signals	7	5	6
High-voltage-level	20 V	30 V	50 V
Clock Frequency	13.9 kHz	100 kHz	20 kHz

V. CONCLUSION

This paper describes a high-voltage SIPO shift register based on a-Si TFTs for DMF chips. Simulation results illustrated that the proposed shift register can successfully transfer a 50 V signal with a clock frequency of 20 kHz. However, under the same condition of 50 V bias voltage and 20 kHz clock frequency, the experimental results show that the output high level of our fabricated SIPO shift register is slightly lower than the output high level of our simulated SIPO shift register. But this can be solved by increasing the supply voltage. The 50 V high voltage is abundant to drive most DMF chips to manipulate droplets, and the frequency of 20 kHz can sufficiently meet the high-speed requirements of DMF chips. Most importantly, a mature and low-cost a-Si TFT manufacturing process can greatly reduce the cost of the drive circuit of DMF chips. Therefore, the SIPO shift register presented in this paper will greatly promote the development of DMF chips.

REFERENCES

[1] F. Qin et al., "Solution for mass production of high-throughput digital microfluidic chip based on a-Si TFT with in-pixel boost circuit," *Micromachines*, vol. 12, no. 10, p. 1199, Sep. 2021, doi: 10.3390/mi12101199.

[2] K. Ugsornrat, T. Pogfai, T. Maturos, A. Wisitsoraat, and A. Tuantranont, "Experimental study of digital microfluidic biochip," in *Proc. 4th Biomed. Eng. Int. Conf.*, Chiang Mai, Thailand, 2012, pp. 207–211, doi: 10.1109/BMEiCon.2012.6172053.

[3] J. B. Chae, I. U. Shin, K. Rhee, and S. K. Chung, "Three-dimensional digital microfluidics using an alternative current electrowetting-on-dielectric (AC-EWOD)," in *Proc. 17th Int. Conf. Solid-State Sensors Actuators Microsyst. (Transducers & Eurosensors XXVII)*, Barcelona, Spain, 2013, pp. 1286–1289, doi: 10.1109/Transducers.2013.6627011.

[4] W. C. Nelson and C. Kim, "Monolithic fabrication of EWOD chips for picoliter droplets," *J. Microelectromech. Syst.*, vol. 20, no. 6, pp. 1419–1427, Dec. 2011, doi: 10.1109/JMEMS.2011.2167673.

[5] Z. Luo et al., "Programmable high integration and resolution digital microfluidic device driven by thin film transistor arrays," *IEEE Access*, vol. 10, pp. 30573–30582, 2022, doi: 10.1109/ACCESS.2022.3159243.

[6] M. Alistar and P. Pop, "Towards droplet size-aware biochemical application compilation for AM-EWOD biochips," in *Proc. Symp. Design Test Integr. Packag. MEMS/MOEMS (DTIP)*, Montpellier, France, 2015, pp. 1–6, doi: 10.1109/DTIP.2015.7161024.

[7] H. Ma et al., "Large-area manufacturable active matrix digital microfluidics platform for high-throughput biosample handling," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp. 35.5.1–35.5.4, doi: 10.1109/IEDM13553.2020.9372110.

[8] M. J. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2753–2763, Dec. 1989, doi: 10.1109/16.40933.

[9] J. H. Park, J. S. Han, and S. K. Joo, "Electrical properties of metal-induced laterally crystallized p-type LTPS-TFT with high-κ ZrTiO4 gate dielectric featuring low equivalent-oxide-thickness," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2391–2397, Jun. 2016, doi: 10.1109/TED.2016.2544862.

[10] S. Lee and A. Nathan, "Subthreshold Schottky-barrier thin-film transistors with ultralow power and high intrinsic gain," *Science*, vol. 354, no. 6310, pp. 302–304, Oct. 2016, doi: 10.1126/science.aah5035.

[11] C. Jiang, H. W. Choi, X. Cheng, H. Ma, D. Hasko, and A. Nathan, "Printed subthreshold organic transistors operating at high gain and ultralow power," *Science*, vol. 363, no. 6428, pp. 719–723, Feb. 2019, doi: 10.1126/science.aav7057.

[12] A. Banerjee, J. H. Noh, Y. Liu, P. D. Rack, and I. Papautsky, "Programmable electrowetting with channels and droplets," *Micromachines*, vol. 6, no. 2, pp. 172–185, Jan. 2015, doi: 10.3390/mi6020172.

[13] A. Meimandi, N. Seyedsadrkhani, and A. Jahanshahi, "Development of an electrowetting digital microfluidics platform using low-cost materials," in *Proc. 27th Iran. Conf. Elect. Eng. (ICEE)*, Yazd, Iran, 2019, pp. 154–157, doi: 10.1109/IranianCEE.2019.8786395.

[14] Y. Xing et al., "A robust and scalable active-matrix driven digital microfluidic platform based on printed-circuit board technology," *Lab Chip*, vol. 21, no. 10, pp. 1886–1896, Mar. 2021, doi: 10.1039/D1LC00101A.

[15] K. Jin, C. Hu, S. Hu, C. Hu, J. Li, and H. Ma, "'One-to-three' droplet generation in digital microfluidics for parallel chemiluminescence immunoassays," *Lab Chip*, vol. 21, no. 15, pp. 2892–2900, Jun. 2021, doi: 10.1039/D1LC00421B.

[16] D. Lei and W. Liu, *Microelectronics of Thin-Film Transistor*. Beijing, China: PHEI, 2020, pp. 117–212.

[17] B. Kim et al., "A depletion-mode a-IGZO TFT shift register with a single low-voltage-level power signal," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1092–1094, Aug. 2011, doi: 10.1109/LED.2011.2157989.

[18] S. Jiang, D. Wang, Y. Wei, H. Ma, and J. Yu, "High-voltage LTPS TFT shift register for active matric digital microfluidics," in *Proc. IEEE Int. Flexible Electron. Technol. Conf. (IFETC)*, Qingdao, China, 2022, pp. 1–2, doi: 10.1109/IFETC53656.2022.9948515.