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I-V-T Characteristics and Temperature Sensor Performance of a Fully 2-D WSe_2/MoS_2 Heterojunction Diode at Cryogenic Temperatures

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(Christian D. Matthus and Phanish Chava contributed equally to this work.)

ABSTRACT In this work, we demonstrate the usability of a fully-2D-material based device consisting of MoS_2/WSe_2 heterojunction encapsulated by hBN and contacted by graphene as temperature sensor for linear temperature measurement at cryogenic temperatures. More precisely, temperatures in the range of 10 K up to 300 K were applied to the device while recording the *I-V* characteristics. In contrast to the classical expectation, the main current flows through the device when it is reversely biased. We ascribe this to a combination of drift-diffusion and band-to-band tunneling, while for very low temperatures ($T < 100$ K), variable-range hopping or trap-assisted tunneling seems dominant. In case of forward bias, the Schottky contact on the WSe_2-anode hinders the charge transport in the voltage range of interest. Additionally, we obtained the activation energy of the saturation current in reverse direction in an Arrhenius diagram. Depending on the bias level, it varies between 100 meV and 300 meV, which may be related to the energy barrier caused by interface traps, generation centers between both semiconducting 2D materials, and the band-to-band tunneling. Furthermore, we investigated the temperature-sensor performance by applying a constant current to the device and measuring the voltage drop at different temperatures. In the range of 40 K up to 300 K, the sensitivity of the sensor is ∼2 mV/K, which is comparable to Si devices, while the linearity is still lower ($R^2 \sim 0.94$). On the other hand, the demonstrated device consists only of 2D materials and is, thus, substrate independent, very thin, and can potentially be fabricated on a fully flexible substrate in a low-cost process.

INDEX TERMS Temperature sensing, 2D-material diode, cryogenic measurements, MoS_2, WSe_2, heterojunction, 2D sensor.

I. INTRODUCTION

Since the invention of graphene achieving the Nobel Prize in physics in 2010 [1], 2D materials are among the most prominent research areas in chemistry, physics, material science, and engineering today. An extremely high potential for 2D materials is predicted in many areas, especially for photonics and printed and/or fully flexible integrated electronics [2], [3], [4]. Also, for advanced sensor systems, which

are in the focus of our work, 2D materials offer great potential. As an example from literature, MoS_2-based chemical sensors were presented [5]. On the other hand, diode-based temperature sensors, although well known for traditional semiconductors as Si [6], silicon-on-insulator (SOI) [7], [8], Ge [9], or emerging materials like SiC [10], [11], [12], were not yet in the main focus of research on 2D materials. Nevertheless, some recent works investigated temperature sensors, which were not based on traditional semiconductor technology but on advanced and nanoscale materials like graphene oxide [13], Ag/Al metal temperature sensors [14], organic-transistor temperature-sensor arrays [15], Pt/In_2O_3 thin-film thermocouples [16], or flexible temperature sensors devices like $SnSe_2$ nanoflakes with 1D NiO gate insulator [17] and, very recently, also the 2D material MoS_2 [18]. Furthermore, other works focused on the thermal carrier transport in 2D films also at cryogenic temperatures [19], demonstrated $MoSe_2$-based thermistors [20], or resistive temperature sensors, e.g., based on the most-prominent 2D material graphene [21], [22]. For a better understanding of the physics of defective semiconductor devices, cryogenic measurements are typically used at temperatures much below room temperatures, e.g., to de-charge or de-occupy defect states. In order to measure the actual temperature of the investigated structure, a monolithic temperature-sensor structure may be helpful. Furthermore, on-chip temperature sensing is also frequently used in circuit design, e.g., for compensating temperature effect in bias net-works defining the operation point of a circuit [23]. Additionally, several other applications can be found for cryogenic on-chip diode based sensors [24]. In most cases, substrate independency allowing, e.g., for mechanical flexibility, is a strong advantages which is also true for an easy manufacturing process. In this paper, we report for the first time on a semiconductor diode for linear temperature sensing at cryogenic temperatures consisting only of 2D materials and based on a MoS_2/WSe_2 heterojunction. The device is shown in Fig. 1 (a) as optical microphotograph and (b) schematic cross section. Note that both gate electrodes shown in Fig. 1 were connected to ground for all measurements, since we only investigated the pn-junction in this work. Several works within the last years already started investigating the transport mechanisms in 2D heterojunctions including MoS_2/WSe_2 interfaces [25], [26], [27], [28], [29], [30], [31]. In some works, studies even include measurements at cryogenic temperatures, while a detailed study on its application, as a temperature sensor, to best of our knowledge, has never been conducted.

The paper is organized as follows: In Section II, we de-scribe the device structure (see also Fig. 1) as well as the manufacturing procedure and the measurement setup. In Section III, the *I-V-T* characteristics are shown and discussed including the carrier transport mechanism, while in Section IV we report on the temperature-sensor performance. Finally, Section V contains the conclusions and the outlook.

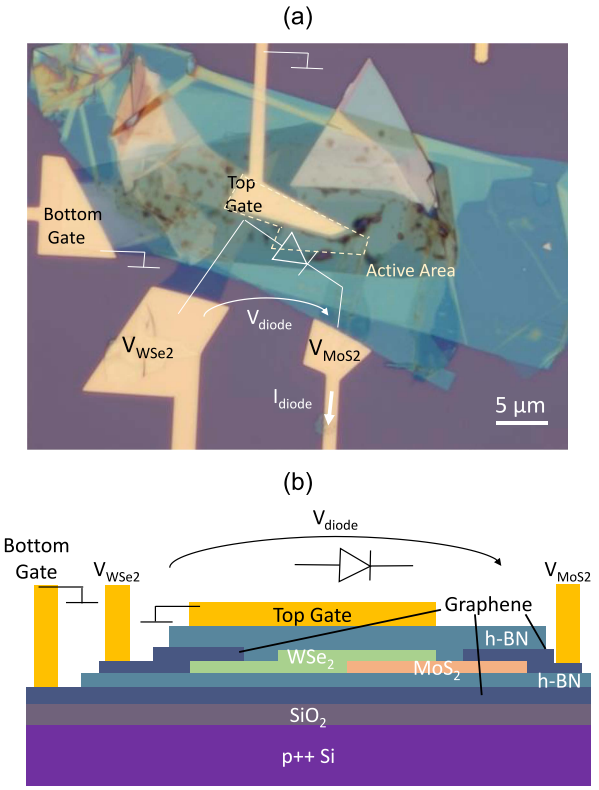

FIGURE 1. (a) Optical microscope image and (b) Cross section schematicshowing the device consisting of 2D materials MoS_2, WSe_2, hexagonal boron nitride (h-BN) and few-layer graphene (FLGr) with all the measurement terminals.

II. EXPERIMENTAL

A. DEVICE STRUCTURE AND FABRICATION METHOD

The 2D materials are mechanically exfoliated onto poly(dimethylsiloxane) PDMS with the help of a scotch tape and are stacked together using the dry stamping technique [32] on a highly p-doped silicon substrate with a thermally oxidized surface (oxide thickness of 285 nm). The complete assembly of the heterostructures is done in a nitrogen filled glove-box environment. The layer-by-layer transfer of each material is shown in Fig. 2 with the help of a schematic diagram and an optical microscope image showing the edges of the transferred flake by dotted lines. We firstly transferred semi-metallic few-layered graphene (FLGr) followed by the dielectric hexagonal boron nitride (h-BN) which forms the bottom gate stack for the device. Semiconducting WSe_2 as p-type semiconductor and MoS_2 as n-type semiconductor were then transferred onto the bottom h-BN forming the active region for the diode. FLGr was used again as an intermediate contact layer to the semiconductors in order to reduce the effect of the Fermi level pinning. The last step of 2D-material deposition was to encapsulate the active region with top h-BN. Finally, the source, drain and gate electrodes are patterned using a single electron beam lithography step. 10 nm/50 nm (Ni/Au) metal stack was evaporated as the interconnect material. The

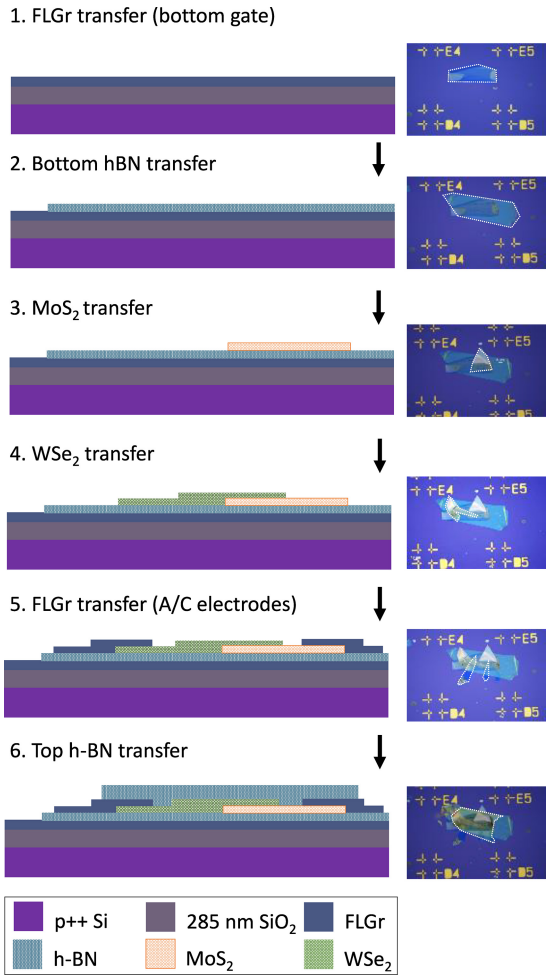

FIGURE 2. Step-by-step fabrication of the heterostructures illustrated by schematics and corresponding optical microscope images. Few-layer graphene (FLGr) was used for anode (A) and cathode (C) contacts.

thicknesses of the transferred flakes were investigated with the help of atomic force microscopy (AFM). The top and bottom h-BN layers were approximately 10-12 nm while the FLGr contacts to the pn-junction (anode and cathode contact) were 6-9 nm. The thickness of WSe_2 and MoS_2 flakes are approximately 5 nm and 3 nm, respectively with a thickness variation of about 1 nm. The AFM profile can be found in Fig. A1 in the Appendix. However, a more precise determination of the thicknesses is difficult without destroying the samples.

B. MEASUREMENT SETUP

The schematic measurement setup is shown in Fig. 3. The device was placed in a vacuum chamber that is connected to a liquid helium dewar in combination with a Lakeshore 340 temperature controller to regulate and monitor the temperature of the chamber. The probes on the devices in the chamber are connected to a 4155C Agilent semiconductor parameter analyzer from which the voltage and current sources were applied to the device-under-test (DUT). We first recorded the *I-V* characteristics of the sample at room

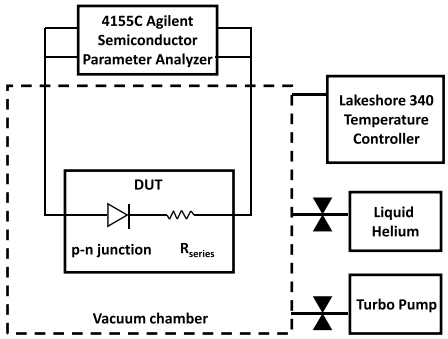

FIGURE 3. Schematic of the measurement setup.

temperature and then cooled down the chamber to the base temperature of 10 K. Measurements were performed at regular intervals of temperature starting from 10 K up to room temperature of 300 K. We mainly recorded two types of measurements throughout the temperature range mentioned: (a) sourcing voltage across the diode by sweeping in the range of −1 V to 1 V, and measuring the diode current (b) sourcing current through the diode in the range of −10 nA to 10 nA, and measuring the corresponding voltage drop across the diode. Although we mentioned about the gate electrodes on top and bottom of the diode previously, these terminals were always grounded during the measurements and therefore have nearly no effect on the characteristics of the diode. In future, we plan to investigate the effect of these gates on the diode. All parasitics (including, e.g., contact resistances) are combined in one series resistance R_{series} (cf. Fig. 3). Latter is not an ideal ohmic resistor and consists of nonlinearities, but for weak bias levels, i.e., low currents the pn-junction modeled by the nearly ideal diode as explained below determines the device current and, thus, R_{series} can be neglected in this case.

III. CURRENT-VOLTAGE-TEMPERATURE CHARACTERISTICS

The measured *I-V* characteristics are shown in Fig. 4 in linear and logarithmic y-scale within the temperature range between 10 K and 300 K for applied voltages over the heterojunction of −1 V up to 1 V in WSe_2/MoS_2 direction. As can be seen, the diode shows rectifying behavior for all temperatures. However, in contrast to a classical pn-junction diode, the main current flows in the reverse direction unlike. This type of reverse rectifying behavior has already been reported for MoS_2/WSe_2 diodes [25], [26], [27], [28]. This may be confusing at a glance, but can be explained having a deeper look on the band structure and, especially, the contact behavior as depicted in Fig. 5. The shown values for electron affinities and bandgaps of the 2D materials are experimentally determined values from literature [29], [33]. The observed current can be explained as follows. The FLGr and Ni/Au contacts form a nearly Ohmic contact to MoS_2 while they show a significant Schottky barrier and rectifying

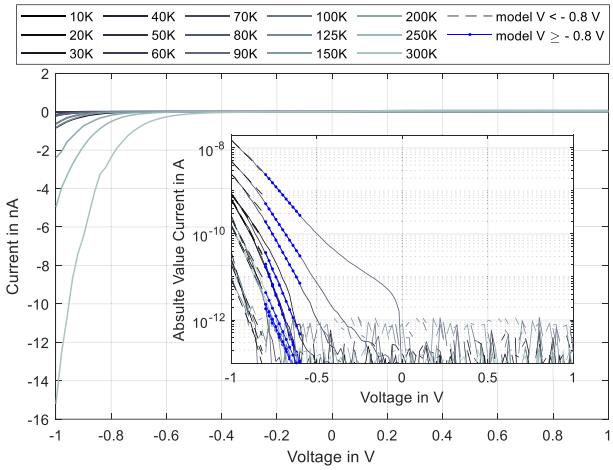

FIGURE 4. ***I-V*** **characteristics in linear scale for** $-1 \leq V \leq 1$ **and inset same in log scale just for** $V > 0$**V.**

behavior towards WSe_2. This Schottky diode (FLGr/WSe_2 junction) has the opposite polarity compared to that of the pn-junction diode (WSe_2/MoS_2 junction). If latter is reversely biased, the influence of the Schottky barrier decreases since it is forward biased and its depletion region becomes very narrow, but its effect cannot be fully ignored at low reverse bias voltages of the pn-junction. Furthermore, in this case minority carriers tunnel from the conduction band of MoS_2 to the valence band of WSe_2 leading to band-to-band tunneling. In case of forward bias of the pn-junction, the recombination and diffusion current (or even drift current for very high bias levels) is blocked by the Schottky barrier of the WSe_2/FLGr-contact. In this case, the width of the depletion region caused by the Schottky barrier increases which may lead to a lowering of the barrier between WSe_2 and MoS_2 when it interacts with the pn-junction depletion region. However, applying higher voltages to the device in order to achieve higher currents may lead to destruction of the sample by local stress due to high electric fields or current densities. In our measurements with low positive voltages applied to the device, nearly no current (1 pA or less) is flowing in forward direction for a bias level of up to 1 V.

In the reverse-biased pn-junction, current can flow due to i) drift-diffusion in light to moderately doped semiconductors; ii) generation of carriers due to defects (Shockley-Read-Hall generation/recombination) or photons; iii) band-to-band tunneling; iv) trap-assisted tunneling; and v) thermionic emission [34]. For the active area of the device of 25 ± 5 μm^2 (uncertainty caused by inhomogeneity of the flakes), the highest current density is approximately 64 mA/cm^2. However, the modeling of the reverse *I-V* characteristics of 2D-material based heterojunctions is not straightforward. Quantum mechanical transport simulations may be required for an in-depth analysis and many parameters have to be set as boundary conditions, which are not all known for the present device. Additionally, quantum mechanical simulations are limited to atomistic scale, while the geometric dimensions of our device are much larger (as shown above). Hence, for a very rough model, we used the classical diode equation to model our reverse current. Note that this is normally valid for the case of forward current in a classical pn-junction diode. In this case, the following equation can be used as also described in the model of Liu et al. [29] for reverse biased WSe_2/MoS_2 heterojunction diodes:

$$I(V,T) = I_0[\exp(qV/k_BT) - 1] \tag{1}$$

with the saturation current I_0, the Boltzmann constant k_B and the elementary charge q. For empirical data, where different carrier transport mechanisms may contribute to the overall current, a simplified formula is also frequently used for voltages much larger than $\sim 3k_BT$. We applied this to the reverse bias regime as follows:

$$I(V,T) = -I_0 \exp(-qV/nk_BT) \tag{2}$$

with the ideality factor n. Using this equation, one can fit a regression line on the obtained currents in semilog scale (see inset of Fig. 4) and deduct from these model lines the value of the saturation current and the ideality factor. This was done twice: for lower reverse bias levels (-0.6 V $>$ V $\geq$ -0.8 V) and higher bias levels (-0.8 V $>$ V $\geq$ -1 V). The obtained values for the ideality factor are shown in Fig. 6. For traditional semiconductor diodes in forward direction, typical values of the ideality factor are approximately between one and two and can be related to diffusion current or recombination current, respectively. However, the values obtained here are significantly higher, i.e., approximately between 3.3 and 8.6 for the lower bias level and temperatures above 50 K, while values between approximately 4.2 and 8.6 were obtained for the higher bias level and the same temperature range. It increases strongly for much lower temperatures (<50 K), which may be a hint for additional carrier transport mechanisms. This can be related to the freeze-out of dopants and charge transport by (Mott variable-range) hopping or trap-assisted tunneling [12], [35], [36], [37], [38], but due to the very low current levels closer to the noise level, the model fit is quite inaccurate and the interpretation needs to be treated with care since we do not use the model according to its physical basis but rather as an equation to fit the data. For temperatures above 50 K, one can have a look onto the temperature behavior of the saturation current I_0 as well. Typically, it follows an Arrhenius behavior in traditional semiconductors caused by the exponential increase of the intrinsic carrier density. Although the physics of this fully-2D heterojunction diode is different, we still expect to have many temperature activated processes involved and therefore one may assume an Arrhenius term as well, which can be described as follows:

$$I_0(T) = \tilde{I}_0 \exp(-E_A/k_BT) \tag{3}$$

with the pre-factor $\tilde{I}_0$ for $T \rightarrow \infty$ assumed to be nearly temperature independent in a first-order approximation and

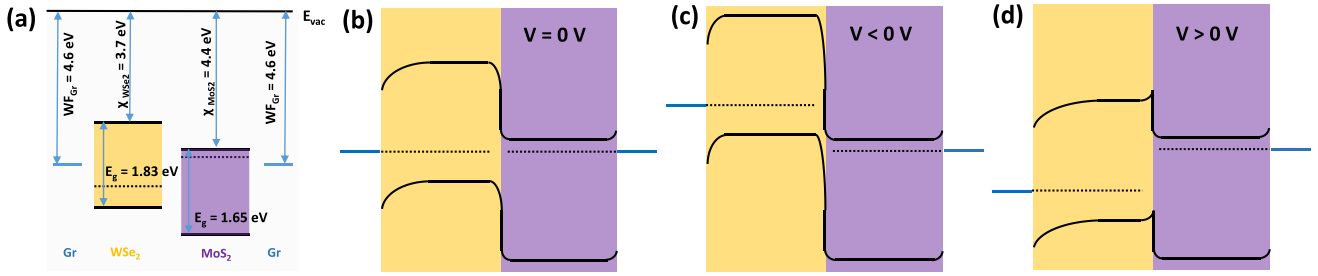

FIGURE 5. **Band diagrams of (a) Graphene, WSe_2 and MoS_2 before the formation of the junction; (b) at thermal equilibrium condition; (c) Reverse bias condition; and (d) forward bias condition. (The values of the electron affinities and the bandgaps for WSe_2 and MoS_2 are taken from [29], and the value of the graphene work function is taken from [33]. It should be noted that the bending of the band edges at the interface is very abrupt due to a very narrow depletion region constrained by the combined thickness of WSe_2 and MoS_2 (<10nm).**

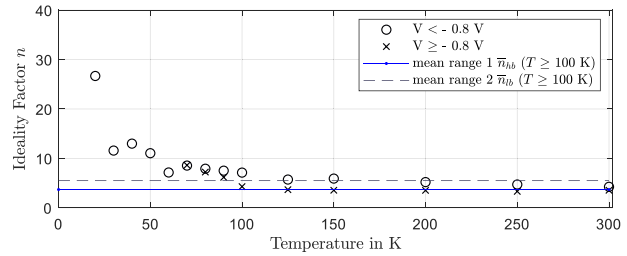

FIGURE 6. **Obtained values for the ideality factor *n* for forward bias levels below and above −0.8 V as a function of temperature.**

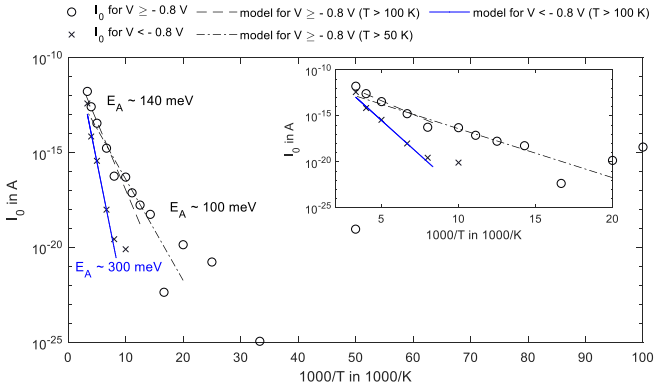

FIGURE 7. **Arrhenius diagram for saturation current I_0 obtained from the regression lines of the I-V characteristics (cf. Fig. 4). Inset: Detail shown for limited temperature range $T > 50$ K.**

the activation energy E_A. We extracted the activation energies again for both higher and lower bias level. The obtained values for I_0 are shown in an Arrhenius diagram in Fig. 7. As can be seen, for $T > 50$ K, i.e., where the model approximation is valid, the obtained values can be represented by an Arrhenius term quite accurately at least for the higher bias level. For the lower bias level, the model only results in a good fit for temperatures of 100 K and above. Thus, we could obtain the values for the pre-factor $\tilde{I}_0$, which are approximately −8.68 pA and −11.4 nA for the higher and lower bias levels, respectively. The obtained activation energies were 105.8 meV and 299.7 meV for the higher and lower bias levels, respectively. The interpretation of the pre-factor $\tilde{I}_0$ is difficult since it consists of many unknown parameters. Thus, for an accurate physical description one needs more information, e.g., about defects and traps in both semiconducting materials. However, the obtained activation energies may give some insights into the carrier transport physics. For the higher bias level, the value of approximately 100 meV fits to the value obtained recently by Daus et al. [18] for a MoS_2 based temperature sensor. In this case, the model used to fit the reverse current is valid to some extent. On the other hand, the obtained value of approximately 300 meV for the lower bias level is close to the conduction band offset of MoS_2 and WSe_2 [38]. This may give also a hint on the current transport mechanism, e.g., thermionic field emission, but further investigations are necessary to fully understand the device behavior. Additionally, one can also distinguish for the higher bias level between an activation energy for temperatures below and above 100 K, with a slightly higher value of approximately 143 meV in the latter case. This is also very close to the values obtained by Daus et al. [18].

Using (2) and (3), one can empirically describe the temperature-dependent voltage drop of the diode biased by a constant current I by

$$V(T) \approx nk_B/q[\ln(-I) - \ln(-\tilde{I}_0)]T - nE_A/q. \tag{4}$$

As can be seen, in this simplified equation the voltage drop V depends linearly on the temperature as long as the temperature dependence of the ideality factor is not dominant. For that, we used an average value of n for both bias levels namely $\bar{n}_{hb} = 5.5$ and $\bar{n}_{lb} = 3.7$, respectively. Hence, we can use the diode as linear temperature sensor as described below.

IV. TEMPERATURE SENSOR PERFORMANCE

Fig. 8 shows the *V-T* characteristics for temperatures between 10 K and 300 K and ten different bias currents in the range of −0.1 nA and −1 nA. Assuming a linear dependence between temperature and voltage drop, we can rewrite (4) as follows:

$$V(T) = S(I)T + V_0 \tag{5}$$

with the temperature sensor's sensitivity S and the offset voltage V_0. The value of latter is typically equivalent to the

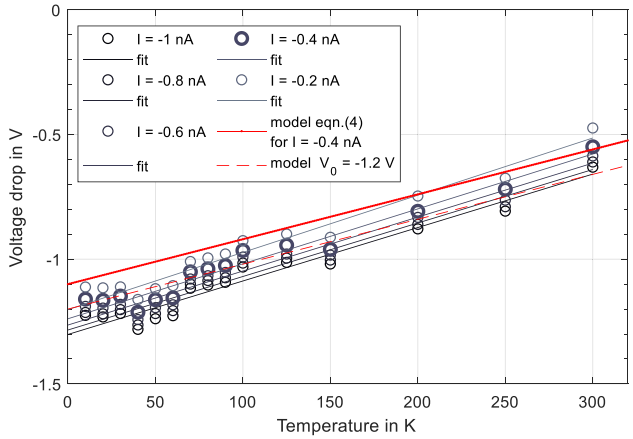

FIGURE 8. ***V-T*** **characteristics for** $I = -1$ **nA,** $I = -0.8$ **nA,** $I = -0.6$ **nA,** $I = -0.4$ **nA,** $I = -0.2$ **nA as well as respective linear fits and fits to the model (cf. (4)).**

TABLE 1. Model and fit parameters for I_0 varying between −0.1 nA and −1 nA.

I (nA)	S_{fit} (mV/K)	$S_{\text{eqn(4),lb}}$ (mV/K)	$V_{0,\text{fit}}$ (V)	$V_{0,\text{eqn (4),lb}}$ (V)	R^2 (-)
-0.1	2.4	1.2	-1.2		0.963
-0.2	2.3	1.5	-1.2		0.963
-0.3	2.2	1.7	-1.2		0.963
-0.4	2.2	1.8	-1.2		0.961
-0.5	2.2	1.9	-1.2	-1.1	0.961
-0.6	2.2	2.0	-1.3		0.959
-0.7	2.2	2.1	-1.3		0.957
-0.8	2.1	2.1	-1.3		0.957
-0.9	2.1	2.2	-1.3		0.956
-1.0	2.1	2.3	-1.3		0.956

bandgap for forward biased pn-junction diodes. This is why the term 'bandgap-reference' is frequently used for similar structure in circuit design [23]. In case of our device, this offset can be estimated by $-n\ E_A/q$. Since the current transport mechanism is bias level dependent and the ideality factor shows a temperature dependence, this offset differs for different bias conditions. We could not observe a relation to the bandgaps of either semiconductor that we used. However, by using an averaged ideality factor, the V-T-characteristics can be described using (5) and shows a somewhat linear behavior as can be seen in Fig. 8. Furthermore, the sensitivity $S_{\text{eqn(4),lb}}$ can be estimated by the first term in (4) and is found to be approximately 1.2 mV/K for −0.1 nA up to 2.3 mV/K for 1 nA and an ideality factor $\overline{n}'$of 3.7. The actually obtained sensitivity S_{fit} vary between 2.4 mV/K for −0.1 nA and 2.1 mV/K for −1 nA. While for higher currents, the matching is quite good, the discrepancy for lower currents can be ascribed to the imperfect description of the device current by the simple model (cf. (2)) and noise limitations. One can see that the behavior generally follows the theoretical line with $\tilde{I}_0$ and $\overline{n}'$ being the only empirical parameters as shown in Fig. 7 exemplary for a current of −0.4 nA. However, one can observe that the offset V_0 calculated by (4) using the mean ideality factor is underestimated by ∼100 meV. This is probably caused by imperfect contacts or leakage paths as well as the upon-mentioned simplifications. If we shift the model line by −0.1 V, the matching is quite well, but another empirical correction is used. If we fit complete empirical linear regression lines following (5) with S and V_0 as free parameters to the measurements, we can describe and evaluate the temperature sensor performance, e.g., regarding linearity. The linearity of these fits represented by the coefficient of determination R^2 is ∼0.96 and comparable to other novel nanodevice-based temperature sensors like [39], while for carbon-nanotube based sensors already values above 0.997 were achieved [40], but this device was not ready for an application as fully flexible sensor. Here, also traditional semiconductors like Si or emerging technologies like SiC come into play. There, values >0.999 were shown in literature [11], [12]. The sensitivity of our sensor is comparable to Si devices as discussed above, while it is higher than the obtained values of several other innovative nanosensors, like [41]. The observed values of our sensor are summarized in Table 1.

V. CONCLUSION AND OUTLOOK

We demonstrated a fully-2D diode based on a MoS_2/WSe_2 heterojunction for temperature sensing in cryogenic regimes. The fitting of the data using a standard diode equation gives a consistent picture describing the sensor behavior seems consistent but although the results are promising and the obtained values of the sensitivity are close to that known from Si, i.e., ∼2 mV/K, the linearity of our device's *V-T* characteristics needs improvement. As next steps we propose the following: 1) Find and validate a physical device model. It requires more effort since it is much more complex, but it will offer better insights in the device behavior and prediction of the same then the simply fitting approach used here. 1) Measure the sensor's performance at elevated temperature and investigate current transport mechanism in this case. 2) Improve technology to achieve better contacts, especially WSe_2-contact. 3) We will also investigate the influence of the additional front and back gate, which were not used for the measurements shown here. It may be possible to tune the electric fields, bands and barriers. 4) Finally, we will use a more advanced concept for current sensing based on two diodes driven with different constant currents or different active areas, respectively while measuring the voltage difference. This concept is called "Proportional-To-Absolute Temperature" (PTAT) [23], since the saturation currents cancel each other out leading to an offset V_0 of 0 V in ideal case. On the other hand, some non-idealities and process variations may contribute stronger in the *V-T* characteristics, but we think this concept is worth for further investigation.

APPENDIX

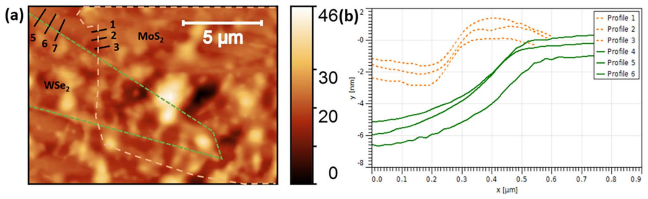

FIGURE A1. (a) AFM scan of the active region indicating the flake boundaries of WSe2 and MoS2 flakes. (b) Extracted height profiles in the positions marked with numbers in (a).

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