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Scalable Small Signal and Noise Modeling of InP HEMT for THz Application

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ABSTRACT Scalable small signal and noise modeling for 90nm InP high electron mobility transistor (HEMT) is proposed in this paper. Analytical expressions for the noise parameters of the intrinsic part are derived from an accurate small signal and noise equivalent circuit model. The experimental and theoretical results show that at the same bias condition, good scaling can be achieved between the HEMTs with different gate widths. Model verification is carried out by comparison of measured and simulated S-parameters up to 325 GHz and noise parameters up to 40GHz. Good agreement is obtained for 90 nm gate-length devices of gate widths including 2×15 μm, 2×20 μm and 2×25 μm gate width (number of gate fingers $\times$unit gate width $\times$cells). The proposed model can be used to predict the S-parameters and noise performance of HEMTs with different geometry accurately.

INDEX TERMS Equivalent circuit model, high electron mobility transistor, semiconductor device modeling, parameter extraction, noise modeling.

I. INTRODUCTION

InP-based high electron mobility transistors are superior in terms of their excellent microwave and noise performance and are good choices for space-based millimeter wave receivers with low DC power consumption [1], [2]. A noise figure as low as 11.1 dB at 850GHz has been achieved as reported in [3].

Most monolithic microwave and millimeter-wave integrated circuits consist of HEMTs with different sizes, the scalable models are powerful computer-aided design tools for optimizing such circuits. Scaling of the small-signal equivalent circuit model dependent on the sizes of gate-length and gate-width regions has been investigated [4], [5], [6]. For a state-of-art process, the most important task is to build a gate-width scalable model, since the reason is the gate-length is fixed normally. Based on the physical scaling rules of small size devices, the performance of large size devices can be evaluated [7], [8], [9], [10] and provide feedback for process control data.

In this paper, the scalable noise and small signal model for InP HEMTs devices have been developed. Based on an improved extrinsic elements extraction procedure has been proposed. The main contribution of this paper is the scalable rules for small signal model and noise parameters up to 325 GHz are given in detail, and three extrinsic resistances can be obtained from the pinch-off (gate-to-source voltage is less than threshold voltage) and zero-biased (gate-to-source voltage is larger than threshold voltage) S-parameters measurements. It can be observed that the HEMTs with different gate width fabricated utilizing the same process can be described by the consistent equivalent circuit model. The proposed model can be used to predict the S-parameters and noise performance of HEMTs with different geometry accurately.

This paper is organized as follows. Section II describes the determination of extrinsic model parameters, and the intrinsic and noise model parameters are given in Section III, and the scaling rules for extrinsic and intrinsic elements are given

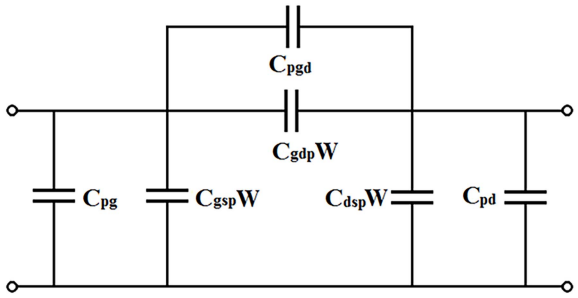

FIGURE 1. Cutoff model at low frequencies.

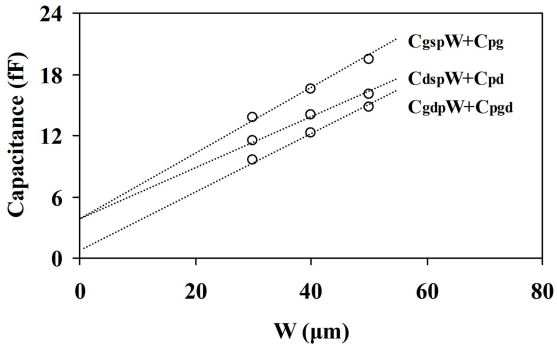

FIGURE 2. Frequency response of imaginary parts of Y-parameters versus gate width.

in detail. The comparison of gate width scaled small signal and noise parameters with the measured data to verify the validity of the technique. The conclusions are discussed in Section V.

II. DETERMINATION OF EXTRINSIC MODEL PARAMETERS

A. PAD CAPACITANCES

Fig. 1 depicts the equivalent circuit model under cutoff bias condition ($V_{gs} < V_{th}$ and $V_{ds} = 0$V) in the low frequency ranges (less than 3GHz normally). It is obvious that the equivalent circuit exhibits a pure capacitive behavior.

The imaginary parts of Y-parameters can be written as:

$$\frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega} = C_{pg} + C_{gsp}W \tag{1}$$

$$\frac{\mathrm{Im}(Y_{22}+Y_{12})}{\omega} = C_{pd} + C_{dsp}W \tag{2}$$

$$-\frac{\mathrm{Im}(Y_{12})}{\omega} = C_{pgd} + C_{gdp}W \tag{3}$$

where C_{pg}, C_{pd} and C_{pgd} are the pad capacitances. C_{gsp}, C_{gdp} and C_{dsp} are the gate width normalized intrinsic capacitances under cutoff bias condition. $W$is the gate width of the PHEM. C_{pg}, C_{pd} and C_{pgd} can be obtained from the interceptions of the three linear regression lines versus gate width simultaneously, as illustrated in Fig. 2.

B. FEEDLINE INDUCTANCES

The extrinsic network of the HEMT device is displayed in Fig. 3, where L_g, L_d and L_s represent the feedline inductances, respectively. The extrinsic inductances are obtained

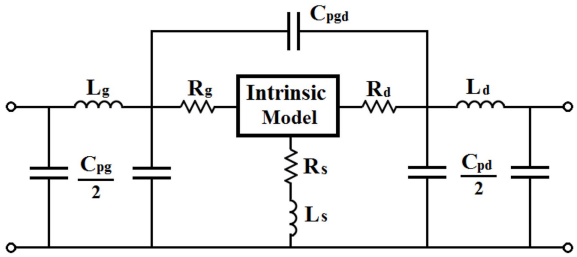

FIGURE 3. Extrinsic network of HEMT device.

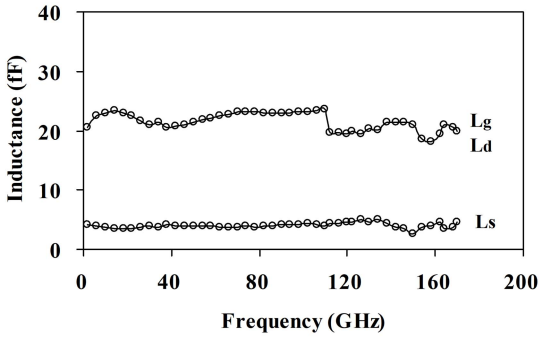

FIGURE 4. Extracted feedline inductances versus frequency.

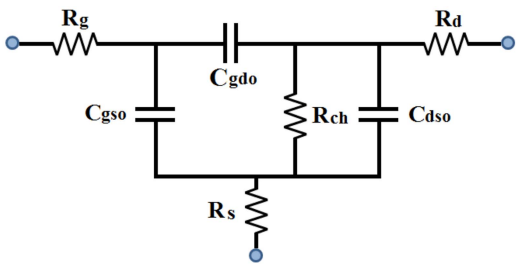

FIGURE 5. Equivalent circuit model under $V_{gs} = 0$ and $V_{ds} = 0$ at low frequencies.

directly from the Z-parameters of the short test structure. The extracted feedline inductances versus frequency are given in Fig. 4. Constant values are observed from 1 GHz to 170 GHz with the deviations from the mean values being less than 10% for feedline inductance L_g and L_d.

C. DETERMINATION OF R_S

After de-embedding the pad capacitances and feedline inductances, the equivalent circuit model under $V_{gs} = 0$ and $V_{ds} = 0$ bias condition is provided in Fig. 5, where R_g, R_d and R_s are the extrinsic resistances, and R_{ch} is the channel resistance. As gate-to-source voltage V_{gs} becomes larger than the threshold voltage V_{th} (V_{th} less than -1V), the channel inversion charge density increases, which increases the channel conductance.

Since the intrinsic capacitances C_{gso} and C_{gdo} dominate the Y_{11} and Y_{12} parameters at low frequencies, we have:

$$C_{gso} = \frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega} \tag{4}$$

$$C_{gdo} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{5}$$

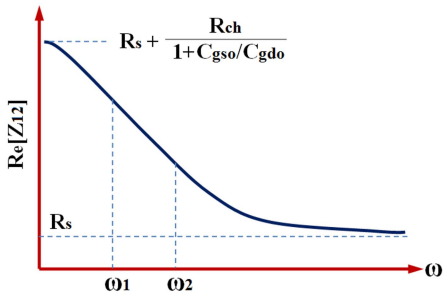

FIGURE 6. Plot of $\mathbf{Re}[Z_{12}]$ versus angular frequency.

Note that the impedance of C_{dso} and channel resistance R_{ch} are compatible, hence it is difficult to determine C_{dso} directly.

The real part of Z_{12} is given by:

$$Re[Z_{12}] = R_s + \frac{R_{ch}}{\left(1 + C_{gso}/C_{gdo}\right)\left[1 + \omega^2 R_{ch}^2 \left(C_{dso} + C_{gdo}\right)^2\right]} \quad (6)$$

The frequency response of $\mathrm{Re}[Z_{12}]$ is portrayed in Fig. 6. When the angular frequency is close to zero, the relationship between R_s and R_{ch} can be obtained:

$$A = R_s + \frac{R_{ch}}{1 + C_{gso}/C_{gdo}} = \mathrm{Re}[Z_{12}]|_{\omega \to 0} \quad (7)$$

Select two frequency points with large differences in frequency response amplitude, such as ω_1 and ω_2. We have:

$$B_1 = A - x + \frac{x}{1 + \omega_1^2 y} \quad (8)$$

$$B_2 = A - x + \frac{x}{1 + \omega_2^2 y} \quad (9)$$

with

$$x = \frac{R_{ch}}{1 + C_{gso}/C_{gdo}}$$

$$y = R_{ch}^2 \left(C_{dso} + C_{gdo}\right)^2$$

Combining (8) and (9), we have:

$$y = \frac{M - 1}{\omega_2^2 - M\omega_1^2} \quad (10)$$

with

$$M = \frac{\omega_2^2}{\omega_1^2} \frac{B_1 - A}{B_2 - A}$$

If $\omega_2 = 2\omega_1$, Eq. (10) can be simplified as follows:

$$y = \frac{M - 1}{(4 - M)\omega_1^2} \quad (11)$$

Substituting y into Eq. (8), x can be determined directly:

$$x = (A - B_1) \frac{1 + \omega_1^2 y}{\omega_1^2 y} \quad (12)$$

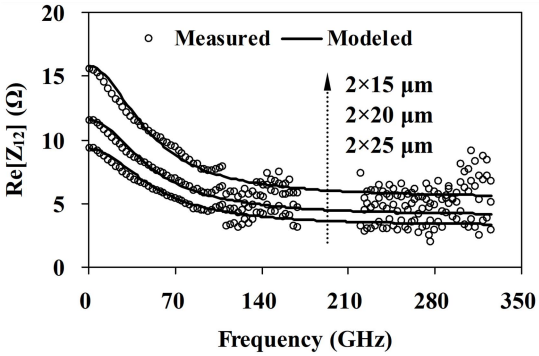

FIGURE 7. Measured $\mathbf{Re}[Z_{12}]$ versus frequency.

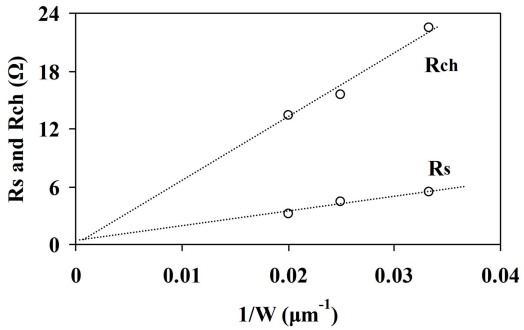

FIGURE 8. Extracted R_s and R_{ch} versus gatewidth.

In the frequency of 1-325 GHz, the modeled and measured $Re[Z_{12}]$ versus frequency is plotted in Fig. 7. Good agreement between modeled and measured data is obtained. The extracted R_s and R_{ch} versus gatewidth is shown in Fig. 8. As seen, R_s and R_{ch} are inversely proportional to the gate width.

D. DETERMINATION OF R_D AND R_G

The real part of Z_{22} can be expressed as follows:

$$Re[Z_{22}] = R_d + R_s + \frac{R_{ch}}{1 + \omega^2 R_{ch}^2 \left(C_{dso} + C_{gdo}\right)^2} \quad (13)$$

At low frequencies, the drain extrinsic resistance R_d can be determined:

$$R_d = \mathrm{Re}[Z_{22}]|_{\omega \to 0} - (R_s + R_{ch}) \quad (14)$$

The real part of Z_{11} can be expressed as follows:

$$\mathrm{Re}[Z_{11}] = R_g + R_s + \frac{R_{ch} C_{gdo}^2 / \left(C_{gso} + C_{gdo}\right)^2}{1 + \omega^2 R_{ch}^2 \left(C_{dso} + C_{gdo}\right)^2} \quad (15)$$

In the high frequency ranges (above 100GHz), the gate resistance is:

$$R_g = \mathrm{Re}[Z_{11}] - R_s \quad (16)$$

For three devices with different gate width, the extracted $R_g + R_s$ in the frequency of ranges 1-170GHz is exhibited in Fig. 9. Furthermore, the extracted R_g and R_d versus gate

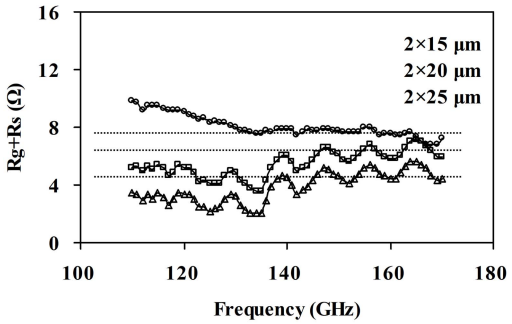

FIGURE 9. Extracted $R_g + R_s$ versus frequency.

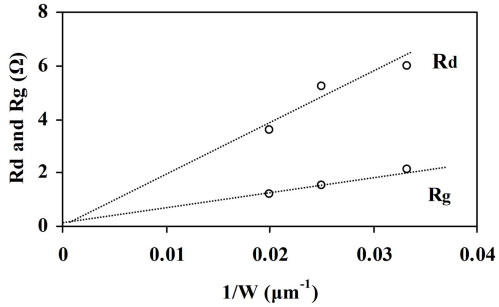

FIGURE 10. Extracted R_g and R_d versus gatewidth.

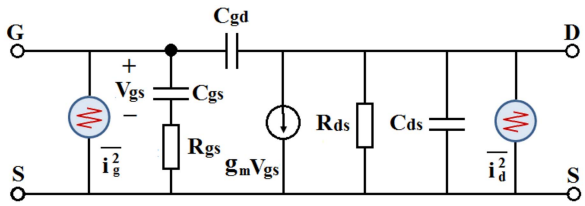

FIGURE 11. Intrinsic small signal and noise model.

width is illustrated in Fig. 10, it is apparent that R_g and R_d are inversely proportional to the gate width.

III. DETERMINATION OF INTRINSIC AND NOISE MODEL PARAMETERS

The intrinsic small signal and noise model is sketched in Fig. 11. After de-embedding all the extrinsic elements, three intrinsic capacitances (gate-to-source capacitance C_{gs}, gate-to-drain capacitance C_{gd} and drain-to-source capacitance C_{ds}), as well as transconductance, output conductance, time delay, and intrinsic gate resistance, form the intrinsic small signal part. Noted that, compared with the impedance of C_{gd}, intrinsic feedback resistance R_{gd} is very small, and can be neglected.

Fig. 12–Fig. 14 display the extracted results versus gate width, it can be clearly observed that the intrinsic capacitances and transconductance are proportional to the size of device, and the intrinsic resistances are inversely proportional to the size of device. Note that the time delay associated with transconductance remains invariant.

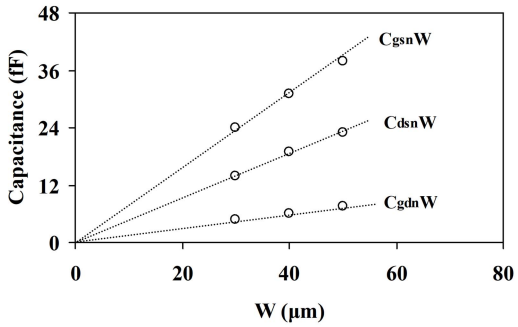

FIGURE 12. Extracted intrinsic capacitances versus gate width.

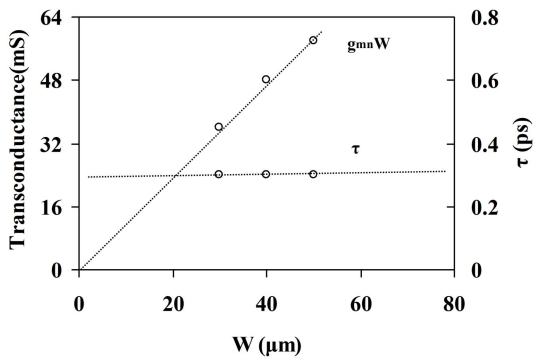

FIGURE 13. Extracted transconductance and time delay versus gate width.

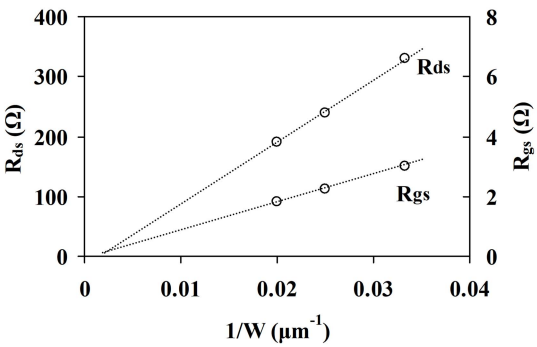

FIGURE 14. Extracted intrinsic resistances versus gatewidth.

The scaling formulas are determined as:

$$\begin{bmatrix} C_{gs} \\ C_{gd} \\ C_{ds} \\ g_m \\ \tau \\ R_{ds} \\ R_{gs} \end{bmatrix} = \begin{bmatrix} W & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & W & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & W & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & W & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & W^{-1} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & W^{-1} \end{bmatrix} \begin{bmatrix} C_{gsc} \\ C_{gdc} \\ C_{dsc} \\ g_{mc} \\ \tau_c \\ R_{dsc} \\ R_{gsc} \end{bmatrix} \quad (17)$$

Subscript c denotes the normalized elementary model parameters.

Based on the Pucel et al.'s model (also called PRC model) and the effect of gate leakage, the corresponding admittance

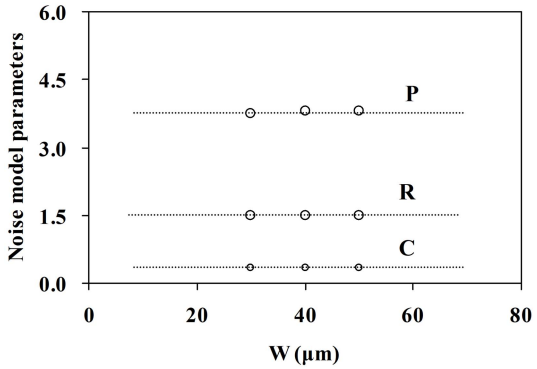

FIGURE 15. Extracted noise model parameters.

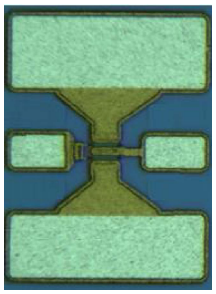

FIGURE 16. Test layout of InP HEMT devices.

noise correlation matrix can be expressed [11], [12]:

$$C_Y = 4kT_o\begin{bmatrix} (\omega C_{gs})^2 R/g_m & j\omega C_{gs}C\sqrt{PR} \\ -j\omega C_{gs}C\sqrt{PR} & g_m P \end{bmatrix} + \begin{bmatrix} 2qI_{gL} & 0 \\ 0 & 0 \end{bmatrix} \tag{18}$$

where R and P are the gate and drain noise model parameters, C represents the correlation coefficient, k represents Boltzmann's constant, and T_o represents the ambient temperature. It can be noticed that the influence of gate leakage currents becomes significant under high drain and gate bias condition. An additional noise current source I_{gL} is needed in parallel with the noise current source at the input port for the PRC noise model [13], [14].

A large size device normally consists of multiple elementary cells with the same gate width connected in parallel [15]:

$$C_Y = WC_{Yc} \tag{19}$$

with

$$C_{Yc} = 4kT_o\begin{bmatrix} (\omega C_{gsc})^2 R_c/g_m & j\omega C_{gsc}C_c\sqrt{P_cR_c} \\ -j\omega C_{gsc}C_c\sqrt{PR} & g_{mc}P_c \end{bmatrix}$$

Substituting (19) in (18), we have:

$$\begin{bmatrix} P \\ R \\ C \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} P_c \\ R_c \\ C_c \end{bmatrix} \tag{20}$$

Fig. 15 gives the extracted noise model parameters versus gate width for InP HEMT devices.

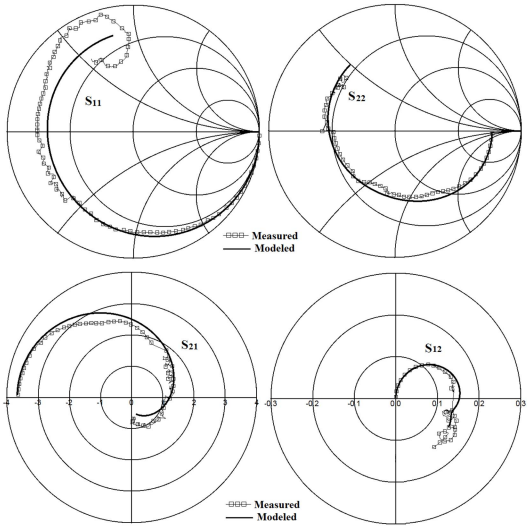

FIGURE 17. Comparison of modeled and measured S-parameters for 2×20 μm HEMT. Bias: $V_{gs} = -0.2$V, $V_{ds} = 1.0$V.

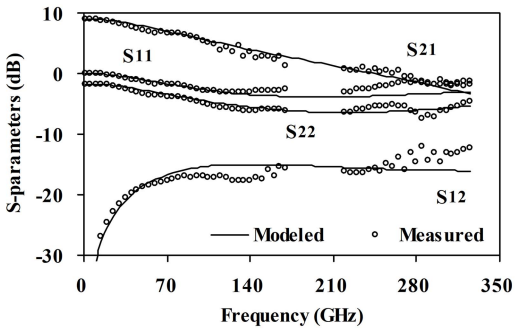

FIGURE 18. Comparison of modeled and scaled S-parameters for 2×15 μm HEMT. Bias: $V_{gs} = -0.2$V, $V_{ds} = 1.0$V.

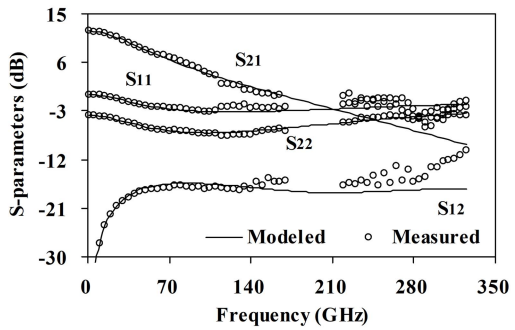

FIGURE 19. Comparison of modeled and scaled S-parameters for 2×25 μm HEMT. Bias: $V_{gs} = -0.2$V, $V_{ds} = 1.0$V.

IV. EXPERIMENTAL VERIFICATION

In order to verify the above results, three 90 nm InP HEMTs with different size 2×15 μm, 2×20 μm and 2×25 μm have been used to demonstrate the proposed model. Microwave S-parameters are carried out on wafer over the frequency range 1-325 GHz, and noise parameter measurements over

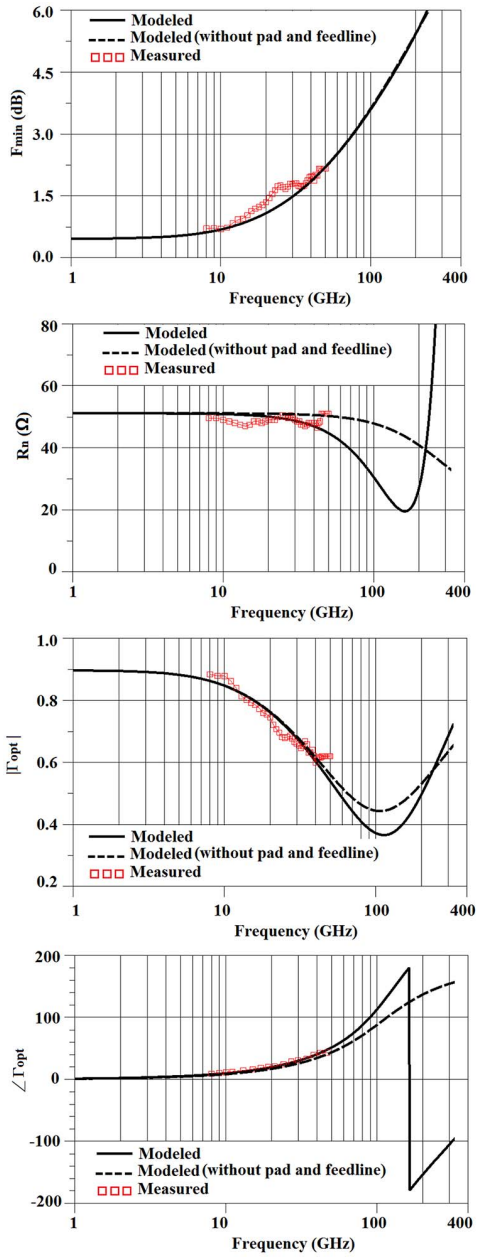

FIGURE 20. Comparison of noise parameters between measured and scaled data for 2×20 μm HEMT device. Bias: $V_{gs} = -0.2$V, $V_{ds} = 1.0$V.

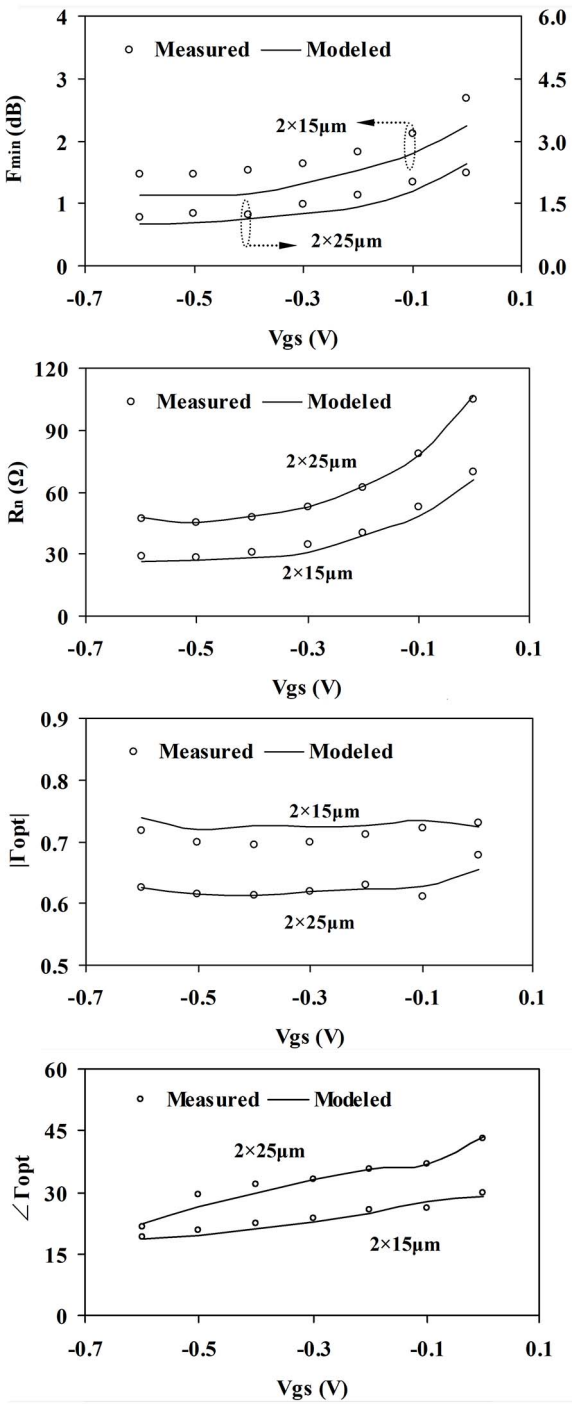

FIGURE 21. Comparison of noise parameters between measured and scaled data for 2×15 μm and 2×25 μm HEMT devices.

the frequency range 8-45GHz. The test layout of InP HEMT devices is shown in Fig. 16 [16].

A. SMALL SIGNAL MODEL VERIFICATION

In the frequency range of 1GHz to 325 GHz, Fig. 17 plots the comparison between the measured and modeled S-parameters for the 2×15 μm HEMT device under bias condition of $V_{gs} = -0.2$V and $V_{ds} = 1.0$V. The good agreement in S-parameters between the measured and the scaled models determined by using the scaling rules for 2×15 μm and 2×25 μm HEMT devices are displayed in Fig. 18 and Fig. 19.

B. NOISE MODEL VERIFICATION

For 2×20μm HEMT device, Fig. 20 shows the modeled noise parameters up to 325 GHz utilizing the whole noise model and without pad and feedline parasitics under bias condition of $V_{gs} = -0.2$V and $V_{ds} = 1.0$V. It can be found that the effect of the pad and feedline can be neglected in the frequency of 1-30 GHz when the pad capacitances and

feedline inductances are as small as enough. The modeled noise parameters are also compared with measured data, in the frequency of 8-45GHz, and good agreement is obtained. Fig. 21 depicts the comparison of measured and modeled noise parameters as a function of gate-to-source voltage by utilizing the scaling rules for $2\times15\mu$m and $2\times25\mu$m HEMT devices under V_{ds} =1.0V bias condition. The noise parameters have been obtained using the tuner-based method. Unfortunately, the optimization techniques may cause ripples in the measured data.

V. CONCLUSION

A scalable noise and small signal model for 90nm InP HEMT is presented in this paper. The experimental and theoretical results show that at the same bias condition, good scaling of the noise and small signal model parameters can be achieved. The validity of the new approach is proven by comparison with measured S- and noise-parameters. The proposed model can be used to predict the S-parameters and noise performance of HEMTs with different geometry accurately.

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