Compensation of Hot Carrier Degradation Enabled by Forward Back Bias in π-GAA-π MOSFET

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ABSTRACT Forward back biasing (FBB) technique is considered as a potential solution for aging compensation in silicon on insulator (SOI) MOSFET. However, traditional SOI devices under FBB would suffer from extra off-state leakage current (I_{off}) and undesirable static power consumption. In this work, we studied the hot carrier degradation and FBB compensation in π-GAA-π MOSFET. With the unique hybrid gate structure, the performance degradation is found to be less severe than pure π gate device; and moreover it can be partially recovered by FBB without the sacrifice of I_{off}. The presence of π gates offer the back gate tunability that is not provided by pure GAA gate; while the GAA gate component can effectively prevent the impact of FBB from affecting the surface potential. Our findings in π-GAA-π hybrid gate MOSFETs would be beneficial for device reliability improvement.

INDEX TERMS Forward back biasing technique, aging compensation, hot carrier degradation, off-state leakage current.

I. INTRODUCTION

HOT CARRIER degradation (HCD), as one of the most important time-dependent reliability issues, is becoming even more serious as the feature size of MOSFETs keeps shrinking [1], [2]. It causes the aging of device parameters, including the decrease of on-state current (I_{on}), the increase of threshold voltage (V_{th}) and subthreshold swing (SS), *etc*. Traditional methods, such as the adoption of light doped drain (LDD) [3] and the lowering of power supply [4], are not adequate to suppress HCD anymore in the advanced technology node.

Adaptive voltage scaling [5], by simply tuning operational voltage, is initially shown as an effective post-silicon tuning method to compensate device performance degradation [6]. Consequently, body biasing is proposed as an alternative strategy since the requirement of higher operation voltage can often in turn accelerate HCD [7]. Under either forward or backward biasing, the threshold voltage can be effectively changed. Recently, SOI structure with the buried oxide layer (BOX) as a good isolation, is introduced for its negligible back gate leakage to eliminate the existence of additional body current. Accordingly, a modified technique, *i.e.*, back biasing, comes up to modulate the *I-V* responses for either ultralow leakage or high-performance requirements [8], [9]. Enabled by forward back biasing (FBB), the efficient increase of I_{on} alongside with the reduction of V_{th}
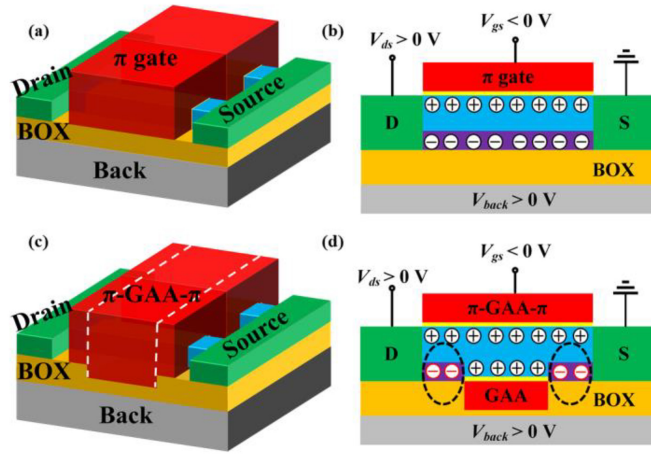
FIGURE 1. (a) Schematics of pure π gate device; (b) Schematics of surface inversion under FBB in pure π gate device; (c) Schematics of π-GAA-π gate device; (d) Schematics of surface inversion under FBB in π-GAA-π gate device.

intuitively offers a solution to compensate device degradation. This has readily attracted great attention in the field of device reliability [6], [10], [11]. However, in traditional SOI MOSFETs illustrated in Figs. 1(a) and 1(b), the generation of a second conduction channel by back gate would weaken the controllability of front gate, which causes the significant increase of SS, I_{off} and static power consumption.

In this work, we propose that such drawback could be settled in the π-GAA-π hybrid gate devices [see Fig. 1(c)] that were developed on void embedded SOI (VESOI) substrates earlier [12]. As illustrated in Fig. 1(d), the presence of central GAA gate can effectively prevent the formation of back conduction channel that sacrifices the off-state stability. And the π gates offer the degree of freedom to modulate the on-state performance by FBB that is not present in pure GAA devices. It is also found that the GAA gate component offers more resistance to hot carrier stress (HCS) as manifested in the more than 33% reduced V_{th} drift than pure π gate device. More importantly, by applying FBB onto the hybrid gate, we could achieve the full recovery of I_{on}, while still maintaining I_{off} at a lower level. In comparison, due to the generation of back conduction channel, I_{off} in pure π gate device is inevitably increased by several orders, together with the dramatic deterioration of SS. Our results on π-GAA-π gate devices fabricated on VESOI substrates can benefit the aging compensation design in integrated circuits.

II. FBB IN HYBRID GATE DEVICES
Device simulation was performed first to verify the FBB scheme using Sentaurus TCAD tool [13], and the results are plotted in Figs. 2(a)-2(c) for π-GAA-π, π gate and GAA devices at $V_{back} = 0$ and 6 V, respectively. Drift-Diffusion model was adopted in simulation with doping dependence mobility and SRH recombination models embedded. The off-state electrostatic potential (φ_{off}) of π-GAA-π device is similar before and after FBB due to the negative bias provided by GAA gate component [see Fig. 2(a)].

The interruption from surface inversion in the middle GAA region can efficiently lower (if not eliminate) any possible leakage at the back, which is also manifested in the simulated I_d versus V_{gs} characteristics for π-GAA-π device (shaded region) at $V_{back} = 0$ and 6 V. On the other hand, for pure π gate devices, φ_{off} is increased by FBB so that a second back conduction channel is eventually formed [see Fig. 2(b)]. This leads to an inevitable increase of I_{off} as manifest in I_d versus V_{gs} characteristics (shaded region) for π gate device at $V_{back} = 6$ V. Moreover, for pure GAA device, an enclosed gate structure can always fix the on-state electrostatic potential in the channel before and after FBB [see Fig. 2(c)]. Despite the better drive current, there is no back gate tunability with the GAA gate structure as evident by the overlapped curves before and after FBB in Fig. 2(c) (shaded region). It is this unique FBB scheme of the π-GAA-π gate that motivates us to examine its capability for possible device performance compensation.

III. RESULT AND DISCUSSION
A. EXPERIMENTAL SETUP
Fig. 3(a) shows the cross-sectional transmission electron microscope (TEM) image of the n-type π-GAA-π gate device as an example. Detailed fabrication process can be found in our previous work [12]. As can be seen, the hybrid poly-silicon gate structure consists of one GAA gate (500 nm) sandwiched by two π gate components (400 and 100 nm) at the sides. Further miniaturization of the channel length is limited by the improvement of VESOI substrates [12] that still requires extensive experimental efforts. The device width is 4.56 μm, and the thickness of gate oxide, GAA and π channel components is 5.6, 48, and 76 nm, respectively [see Figs. 3(b) and 3(c)]. It should be noted that the pure π device for comparison purpose was fabricated with the same designed physical parameters.

We performed a combined proof-of-concept experimental measurement including hot carrier stress (HCS) induced aging and FBB compensation. After withstand voltage test [14], the drain stress voltage is selected as 8 V for accelerated degradation purpose. And then we select $V_{gs} = 1/2\ V_{ds} = 4$ V empirically where maximum substrate current usually happens in long channel device [15]. HCS aging process was then performed for a total duration of 1000 s stress time with periodic interruptions for measurements of I_d -V_{gs} curves in both linear ($V_{ds} = 0.1$ V) and saturation ($V_{ds} = 2.5$ V) regions. Note that V_{back} is always kept at 0 V during the aging process. In the subsequent compensation process, we measured I_d -V_{gs} curves in both linear and saturation region with different applied V_{back} from 0 V to 6 V. All the measurements were done using Keysight B1500A semiconductor analyzer at room temperature.

B. DISCUSSION OF HCD AND FBB COMPENSATION
Fig. 4 shows the stress time evolution of I_d -V_{gs} in both linear and saturation region for fresh π-GAA-π [see Figs. 4(a) and 4(b)] and π gate [see Figs. 4(c) and 4(d)] devices at
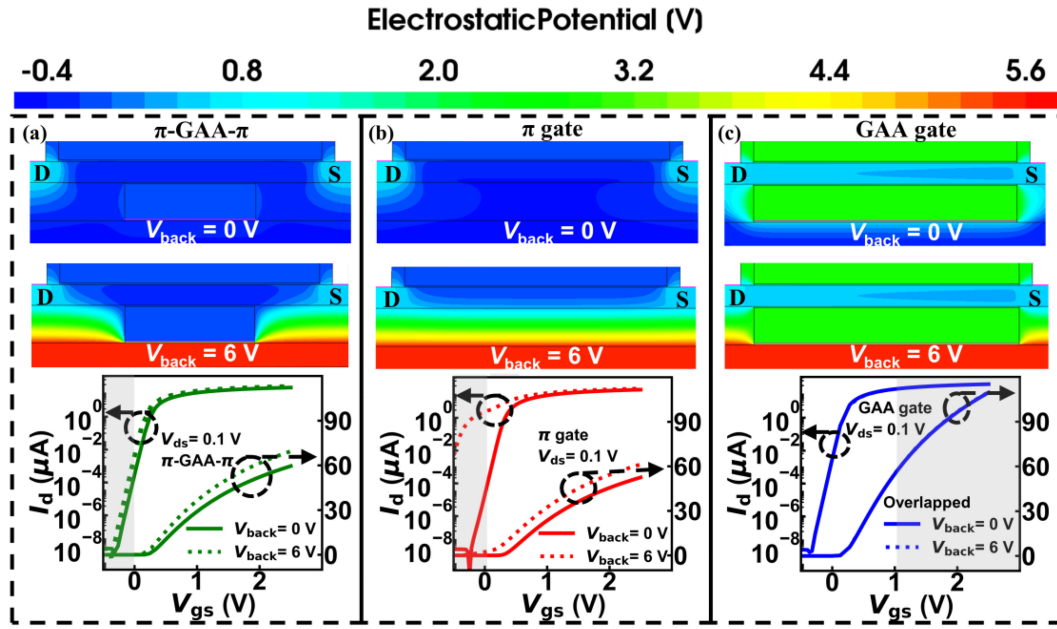
FIGURE 2. (a) Simulated off-state electrostatic potential profile and I_d-V_{gs} with V_{back} = 0 V and 6 V in (a) π-GAA-π gate device; (b) π gate device; and (c) GAA gate device (overlapped curves). Note that the bias condition of electrostatic potential images in (a) and (b) is V_{gs} = −0.5 V, V_{ds} = 0.1 V, and that in (c) is V_{gs} = 2.5 V, V_{ds} = 0.1 V.
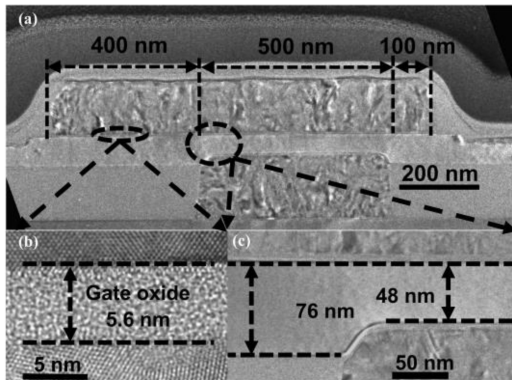

FIGURE 3. (a) Cross-section TEM image of π-GAA-π gate device; (b) Enlarged view of gate oxide; (c) Enlarged view of GAA and π channel.

V_{back} = 0 V. The curve shift of both devices follows the conventional HCD behavior observed in MOSFETs [16], [17], [18]. It can also be seen that HCD induced curve shift in π gate device is severe than the one in π-GAA-π device. Subsequently, the FBB compensation was conducted in Figs. 4(e)-4(h) by applying V_{back} up to 6 V. Indeed, the I_d -V_{gs} curves of both π-GAA-π device [see Figs. 4(e) and 4(f)] and π gate devices [see Figs. 4(g) and 4(h)] can be gradually shifted back under FBB in both linear and saturation region.

More quantitatively, the stress time/FBB dependences of ΔI_{on} (including both ΔI_{dlin} and ΔI_{dsat}), ΔV_{th} (including both ΔV_{thlin} and ΔV_{thsat}), average ΔSS (including both ΔSS_{lin} and ΔSS_{sat}) and I_{off} ratio (including both I_{offlin} ratio and I_{offsat} ratio) were extracted from Fig. 4 and plotted in Fig. 5, respectively. These four parameters (especially ΔI_{on}

and I_{off} ratio) are selected to reflect the stress time dependent degradation of device on-state performance and static power consumption. In particular, the parameters extracted in the saturation region are more meaningful since the operation point of MOSFET in real circuits is mostly in this region. V_{th} at different V_{ds} can be used to reflect the drain induced barrier lowering (DIBL) effect; and SS represents the gate control capability from surface accumulation to surface inversion. As can be seen, I_{dlin} and I_{dsat} decrease by 1.1% and 3.6% in π-GAA-π device, while the decrease is 2.0% and 5.8% in pure π gate device. I_{dlin} and I_{dsat} in both two devices can be fully recovered by applying around 2.5 V FBB [see Figs. 5(a) and 5(b)]. Moreover, ΔV_{thlin} and ΔV_{thsat} are 66.6 mV and 47.0 mV in π-GAA-π device, and the shifts are considerable larger in pure π gate device as 101.6 mV and 99.0 mV, respectively. Both parameters can only be partially compensated in π-GAA-π device at V_{back} = 6 V, but a full recovery can be achieved for π gate one with the presence of full BOX layer at V_{back} > 4 V [see Fig. 5(c) and 5(d)]. On the other hand, SS_{lin} and SS_{sat} are increased by 9.1 mV/dec and 3.7 mV/dec in π-GAA-π device after HCD, while an even larger increase of 15.3 mV/dec (SS_{lin}) and 13.4 mV/dec (SS_{sat}) is observed in pure π gate device [see Fig. 5(e) and 5(f)]. As can be further seen, since FBB only provides an additional current rather than recovering the induced traps, neither SS_{lin} nor SS_{sat} can be compensated in π-GAA-π or π gate devices. In fact, with the generation of back channel current at V_{back} > 2 V, SS is even more dramatically deteriorated in π gate device. Finally, both I_{offlin} and I_{offsat} in π-GAA-π gate device decrease to 25% and 56% of the initial values accompanied by the increase of V_{th} after HCD. Similar situation is also observed in pure
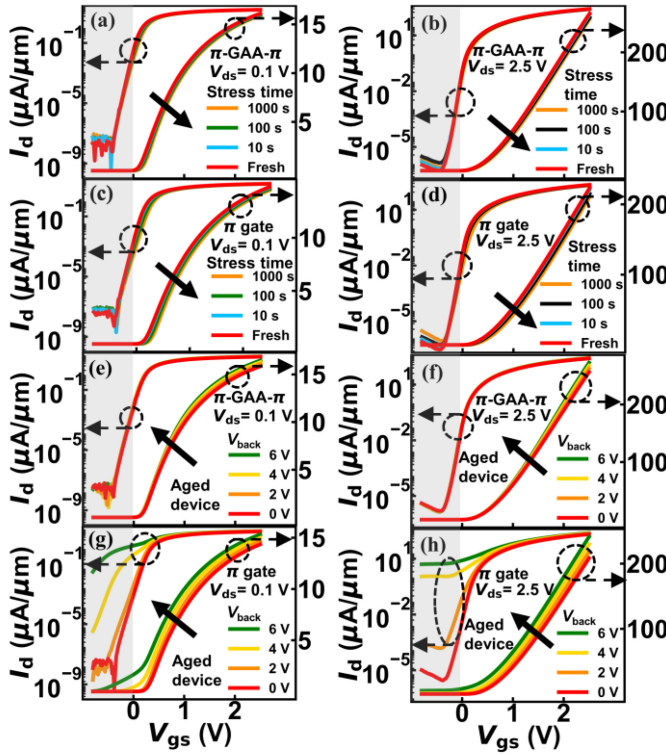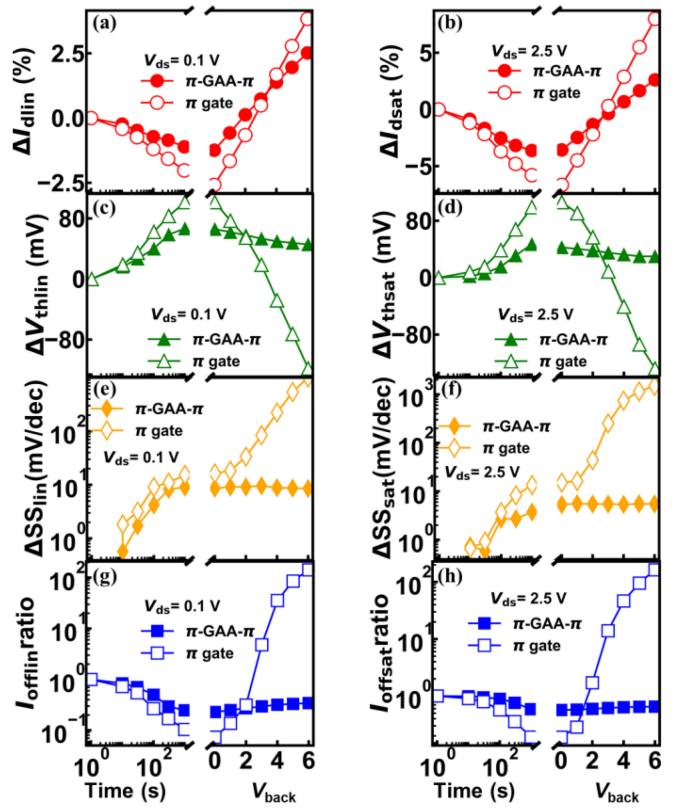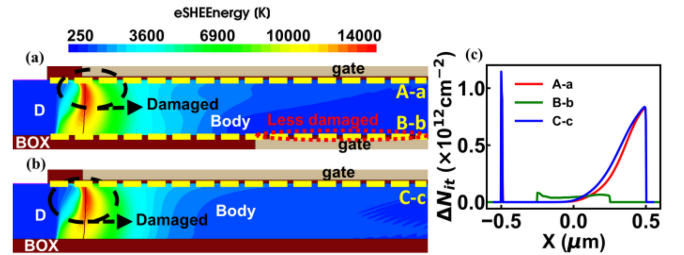
FIGURE 4. Experimental results of the stress time dependent I_d versus V_{gs} curves: fresh π-GAA-π gate device with (a) $V_{ds} = 0.1$ V (linear region) and (b) $V_{ds} = 2.5$ V (saturation region), respectively; and fresh π gate device with (c) $V_{ds} = 0.1$ V (linear region) and (d) $V_{ds} = 2.5$ V (saturation region), respectively. Note that the measurement time stamp is taken at 0, 10, 100, 1000 s, respectively. Experimental results of the back gate dependent I_d versus V_{gs} curves after 1000 s stress time: aged π-GAA-π gate device with (e) $V_{ds} = 0.1$ V (linear region) and (f) $V_{ds} = 2.5$ V (saturation region), respectively; and aged π gate device with (g) $V_{ds} = 0.1$ V (linear region) and (h) $V_{ds} = 2.5$ V (saturation region), respectively. Note that V_{back} is taken at 0, 2, 4, 6 V, respectively.

FIGURE 5. Device performance parameters in HCS aging and subsequent FBB compensation process for π-GAA-π and π gate devices at $V_{ds} = 0.1$ V (linear region) and 2.5 V (saturation region), respectively: (a) ΔI_{dlin}; (b) ΔI_{dsat}; (c) ΔV_{thlin}; (d) ΔV_{thsat}; (e) ΔSS_{lin}; (f) ΔSS_{sat}; (g) I_{offlin} ratio; (h) I_{offsat} ratio. Note that ΔI_d is defined as [I_d (time, V_{back}) − I_d (0, 0)] / [I_d (0, 0) × 100%] with $V_{gs} = 2.5$ V. ΔV_{th} is the HCS or V_{back} induced threshold voltage shift extracted by linear exploration method (Note that time zero V_{thlin} are 72 and 112 mV, and V_{thsat} are −47 and −13 mV in π-GAA-π and π gate devices, respectively). ΔSS is the HCS or V_{back} induced change of subthreshold swing averaged between the range of I_d from 10^{-6} to 10^{-2} μA/μm. I_{off} ratio is defined as I_d (time, V_{back}) / I_d (0, 0) with $V_{gs} = 0$ V. Note that the subscript "lin" (or "sat") indicates the parameter extracted from the linear (or saturation) region.

π gate device but with a more decrease of I_{offlin} and I_{offsat} to about 10% and 19% of their initial values [see Fig. 5(g) and 5(h)]. However, during FBB compensation, I_{offlin} and I_{offsat} in our π-GAA-π device can be maintained at a low level with negligible increase due to the switch-off of back channel by GAA gate component. In contrast, both parameters increase dramatically by tens and even hundreds of times in pure π gate device. This sharp difference of I_{off} again corroborates that the GAA gate is dominated in the hybrid gate structure. More importantly, it can be used as a good shield to prevent the impact from substrate, especially at the off-state region.

It is also interesting to find that both ΔV_{thlin} and ΔV_{thsat} in π-GAA-π gate device is only $\sim$ 2/3 and $\sim$1/2 of that in π gate ones. This improvement can be understood from the simulated electron energy and eInterfaceTrappedCharge distribution (ΔN_{it}) [19], [20], [21] in Fig. 6. Hydrodynamics model is used with doping dependence mobility and SRH recombination embedded. Spherical-Harmonics Expansion method is used to calculate carrier energy distribution with HCSDegradation model for transient 1000 s HCS simulation. As can be seen from Figs. 6(a) and 6(b), the similar electron


FIGURE 6. Electron energy distribution of π-GAA-π (a) and π gate device (b), respectively (only drain half is shown). Note that bias condition is: $V_{ds} = 8$ V, $V_{gs} = 4$ V, $V_{back} = 0$ V; (c) Simulated HCS induced eInterfaceTrappedCharge (ΔN_{it}) along the front and bottom surfaces as indicated by the dashed lines in (a) and (b).

energy near the drain side for both devices (dashed circle) agrees with the normal view that localized damages happen at the drain side where carriers obtain enough energy for injection [22], [23]. While since the bottom surface of GAA gate is far away from the drain side, the carrier energy there
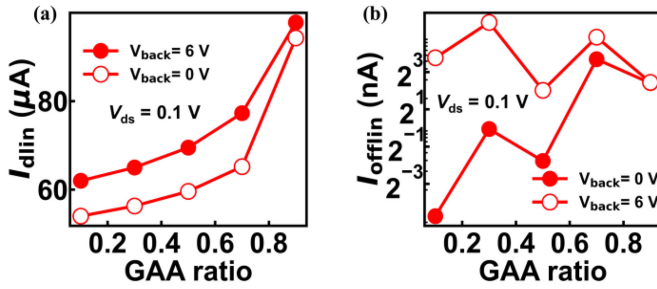
FIGURE 7. (a) I_{dlin} versus different GAA ratios at $V_{back} = 0$ V and 6 V, respectively. (b) I_{offlin} dependence on different GAA ratios at $V_{back} = 0$ V and 6 V, respectively. Note that the GAA ratio is defined as the GAA length divided by the total channel length (fixed at 1 μm).

FIGURE 8. Simulated results of device parameters in π-GAA-π device with reduced channel lengths. (a) I_{dlin}, (b) ΔV_{thlin}; (c) SS_{lin}; (d) I_{offlin}.

is maintained at a relatively low level (dotted circle). This naturally results in a less damaged bottom gate region [see Fig. 6(c)] with an overall reduced equivalent HCS induced trapped charge sheet density (ΔN_{eq}) [24], as the damage process depends on the carrier energy (single-particle mechanism) [25] in long channel devices. Note that for simplicity ΔN_{eq} can be considered as the simulated ΔN_{it} averaged over the gate length. It can be further correlated to HCS induced threshold voltage shift ΔV_{th} via the expression $\Delta V_{th} = q\Delta N_{eq}/C_{ox}$ [26], where q is elementary charge and C_{ox} is oxide capacitance. Therefore, the reduced ΔN_{eq} in π-GAA-π device is mainly responsible for the less ΔV_{th} as compared to the pure π one. It is now clear that our hybrid gate device can inherently harness the advantages of both FBB technique and strong gate control ability for improved reliability.

C. TCAD INVESTIGATION ON π-GAA-π DEVICE OPTIMIZATION

It is critical to investigate the modulation capability with different ratios of GAA and π channel components for further trade-off between performance and tunability. By using the same physical model as Fig. 2, we varied the GAA ratio, defined as the GAA length divided by the total channel length, while maintaining the total length at 1 μm. As an example, Fig. 7 (a) shows the linear drain current (I_{dlin}) dependence on the GAA ratio. It increases when the device structure evolves more towards pure GAA device for high performance; and meanwhile the modulation capability of I_{dlin} decreases as manifested by the gradual approaching of the two curves at $V_{back} = 0$ V and 6 V. Following the traditional reliability standard [27], if we consider the threshold ratio as that can boost I_{dlin} by 10% at $V_{back} = 6$ V [i.e., I_{dlin} ($V_{back} = 6$ V) $- I_{dlin}$ ($V_{back} = 0$ V) $\geq$ 10% I_{dlin} ($V_{back} = 0$ V)], the modulation capability would become insufficient to compensate the potential I_{dlin} degradation when the GAA ratio is larger than $\sim$0.8. On the other hand, the off-state current (I_{offlin}) at $V_{back} = 6$ V remains to be stable at around 8 nA regardless of the GAA ratio [see Fig. 7 (b)]. This again suggests that the main advantage of hybrid gate device is to efficiently suppress the leakage current by FBB.

To further show the device scaling capability, we performed TCAD simulation with the same physical model
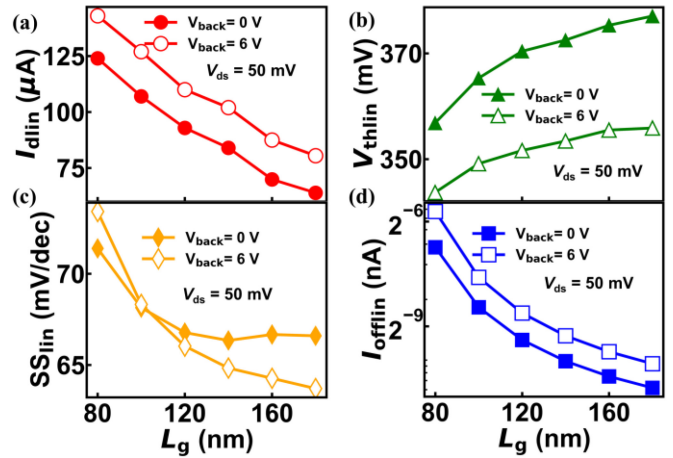
setup as before to investigate the back gate tunability of device parameters under different channel lengths. It should be noted that further scaling down usually requires the extra optimization from FDSOI to Ultra-thin body and BOX (UTBB) SOI device, e.g., doping concentration, body and BOX thickness. For simplicity, here we fixed the doping concentration, thickness of body and BOX at 10^{17} cm^{-3}, 40 nm and 30 nm, respectively. The I_d-V_{gs} curves with $V_{ds} = 50$ mV were then simulated for different channel length (L_g) between 80 nm to 180 nm with a fixed middle GAA component ratio of 50%. As can be seen, the impact of FBB on I_{dlin} boosting keeps stable along with the device scaling down [see Fig. 8(a)], while its improvement on V_{thlin} and SS_{lin} is attenuated [see Figs. 8(b) and 8(c)] due to the relatively thicker channel and BOX thickness that lower the impact of FBB on front gate control capability. Finally, it is worth pointing out that the increase of I_{off} under FBB, almost immune to the reduction of channel length, is only a factor of 2 [see Fig. 8(d)], which is still a relatively small value in comparison with the traditional SOI device.

Before ending this section, it is necessary to summarize the optimization guideline for future π-GAA-π device design. First, it is clear that the scaling of VESOI substrates with narrower void widths is demanded for device miniaturization. While for the optimization of GAA ratio, the margin to suppress I_{off} is quite large as long as the generation of back channel can be interrupted. Most of the consideration would thus lie on the trade-off between the device performance and tunability. In fact, similar to FinFlex™ technology [28], our π-GAA-π device also provides the flexibility for circuit designers to dive into different applications with a proper choice of GAA gate ratio. For example, a relatively large GAA ratio is favored for performance boosting; while a lowered ratio is useful for process and temperature variation tightening or reliability improvement [11].

IV. CONCLUSION

Hot carrier degradation and the associated compensation by FBB were investigated on π-GAA-π gate device on VESOI

substrates through both experiment and simulation. Both I_{on} and V_{th} from HCD can be partially compensated under FBB due to the existence of π gates; while the GAA gate can fix φ_{off} to prevent the undesirable increase of I_{off}. This can lead to lowered standby power consumption that is not found in conventional SOI technology. Although the damage cannot be eliminated under FBB, the device lifetime can be extended by real-time degradation monitoring and adaptive FBB modulation [6], [9], [10]. This capability can continuously sustain with device scaling down until the limitation of body and BOX thickness. Besides, the HCD in hybrid gate device is also much milder than the one with full BOX, which can be attributed to the less damaged region near the bottom GAA gate. This unique advantage, achieved by the simultaneous cooperation of π and GAA gates, offers an additional degree of freedom to modulate device performance. Although this modulation/compensation capability is achieved at the cost of lowering initial drive current in comparison with pure GAA device, as an intermediate structure between SOI and GAA technology, it is expected to be further optimized by a fine-tuning of the GAA/π gate components along the channel under the requirements of either higher performance or better reliability.

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