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Over 10W/mm High Power Density AlGaN/GaN HEMTs With Small Gate Length by the Stepper Lithography for Ka-Band Applications

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ABSTRACT This study reports AlGaN/GaN high-electron-mobility transistors (HEMTs) fabricated by the Stepper Lithography on a 4-inch wafer for Ka-Band applications. Small gate length (L_G) of 100 nm was achieved through a 2-Step Photolithography Process and the gate region of the AlGaN/GaN HEMT was defined by using two lithography steps to form gamma-shaped gates. The 4-inch AlGaN/GaN HEMT wafer demonstrated high electrical performance uniformity with respect to the maximum drain-source current density (I_{DSS}), the peak extrinsic output transconductance (G_m), and the threshold voltage (V_{th}). At $V_{DS} = 20$ V, the AlGaN/GaN HEMT exhibits an I_{DSS} of 1004.2 mA/mm, a Gm value of 363.6 mS/mm, a maximum output power density ($P_{OUT\ (MAX)}$) of over 10 W/mm, and a power gain of 8.8 dB with a maximum 51.1% Power-added efficiency (PAE) at 28 GHz in Continuous Wave (CW) mode. The results show the potential of AlGaN/GaN HEMT fabrication with high yield and outstanding RF performance using Stepper Lithography for 5G applications.

INDEX TERMS 5G, high uniformity, output power, stepper lithography, small gate length.

I. INTRODUCTION

Gallium Nitride, with its outstanding characteristics by forming 2-Dimensional Electron Gas (2DEG) through piezoelectric and spontaneous polarizations using AlGaN/GaN heterojunction, was used for power high-electron-mobility transistor (HEMT) devices with multi-gigahertz frequency range in the year of 2005 by Eudyna Corporation in Japan [1]. Later, with its high mobility, high bandgap and high thermal conductivity features [2], the GaN HEMT devices became popular worldwide for RF applications due to the inherent material properties which include high breakdown voltage, high current density, low thermal resistance, and low substrate parasitic capacitances [3], [4]. GaN-based HEMTs outperform Si and GaAs-based devices [5] owing to their higher output power characteristics and higher thermal resistance. With the increasing demands of RF power devices at Ka-Band and beyond for applications such as 5G, military radars, satellites, and networks for advanced communication systems, it is essential to reduce the GaN high frequency device manufacturing cost by increasing the device yield and to improve the device DC and RF performance.

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Traditionally, researchers fabricate small gate length (L_G) devices with the E-beam Lithography System [6], [7], [8], [33]. However, for mass production of the GaN HEMT for 5G commercial applications, the E-beam Lithography Process is complicated, high cost, and time consuming. Therefore, it is essential to develop more efficient and economical methods with higher yield to meet the industrial needs.

Over the past few decades, Steppers, also known as the Step-and-Repeat Lithography System, have been widely adopted for large scale commercial application of III-V semiconductor integrated circuits for its' simple and direct process steps and capability to utilize a fine reticle with less particles [9], [10], [11]. However, for the conventional stepper process, it is difficult to achieve submicron gate lengths to reduce gate resistance, increase cut-off frequency, and switching speed for high frequency applications.

To scale down the L_G with the Stepper, a 2-Step Photolithography Process is introduced in this study. High performance Ka band HEMT devices on a 4-inch SiC wafer with excellent wafer uniformity using the Stepper Lithography is realized by the approach in this paper.

II. DEVICE FABRICATION

To provide high 2DEG density for the device for high RF power operation, wafers with AlGaN/AlN/GaN layers grown on top of the SiC substrate by the metal organic chemical vapor deposition (MOCVD) system were used. The epitaxy of the SiC wafer includes a 0.3 μm Fe-GaN buffer layer with doping concentration of 1×10^{18} cm^{-3}, a 0.9 μm i-GaN buffer layer, a 0.8-nm AlN layer, and a 17-nm AlGaN barrier layer to realize the heterojunction structure. A 2DEG density of 1.3×10^{13} cm^{-2} and an electron mobility of 2300 $cm^2/V\cdot s$ were obtained based on the Hall measurement of the structure.

Standard fabrication steps of source/drain ohmic contact formation, device isolation, gate Schottky contact formation, passivation and contact via hole formation were processed. After the wafer cleaning process by Acetone (ACE) and Isopropyl alcohol (IPA), the wafer was then immersed in a 10% Hydrochloric acid (HCl) solution to remove the native oxides.

Transfer length method (TLM) was used for the extraction of R_C. The contact resistance was 0.35 $\Omega\cdot$mm, and the contact resistivity is 2.6×10^{-6} $\Omega\cdot cm^2$, as shown in Fig. 4. The Ti/Al/Ni/Au ohmic contact was then deposited by the E-gun evaporator (E-gun) and then annealed at 850 °C for 30 s in N_2 ambient for alloying.

Device isolation was defined by Boron implantation. The gate formation process is shown in Fig. 1. A 150-nm thick SiN_x film was first deposited with Plasma-Enhanced Chemical Vapor Deposition System (PECVD) on the wafer. Then, the first stepper lithography process was done and Position 1 was defined after ICP etch. To ensure the 1st nitride etch reach the barrier layer, the SiN_x layer was etched with CF_4 plasma [12]. The second photolithography step begins with a shifted gate mask, which is the patterning of the 2nd photoresist layer. Finally, a small opening in the etched SiN_x (Position 2) is defined by the 2nd stepper lithography process. Gate formation was completed by the deposition of Ni/Au stack metal using E-gun. SiN_x passivation layer was grown by the PECVD to protect the wafer surface [13] after gate metal deposition. To reduce the skin effect at high frequency operation, 2μm thick metal interconnects were evaporated on the device contact pads.

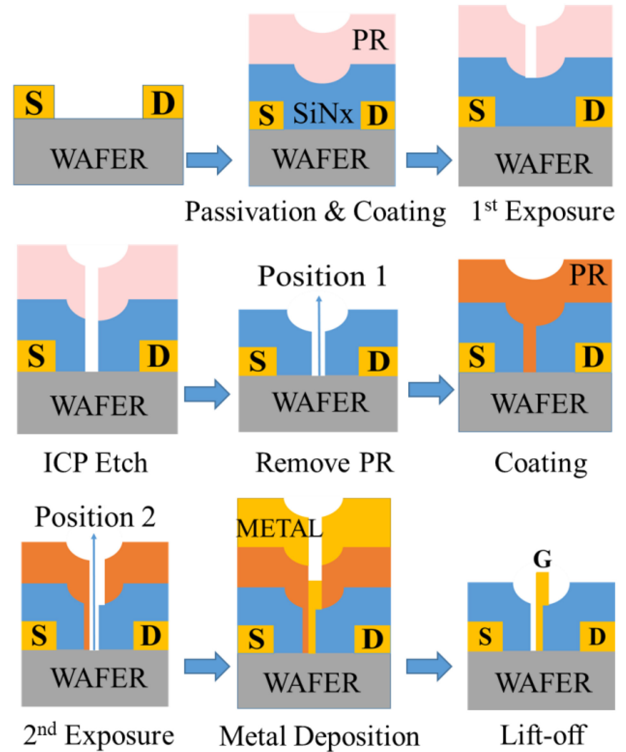

FIGURE 1. 2-Step Photolithography Process shown with its cross section of AlGaN/GaN HEMTs.

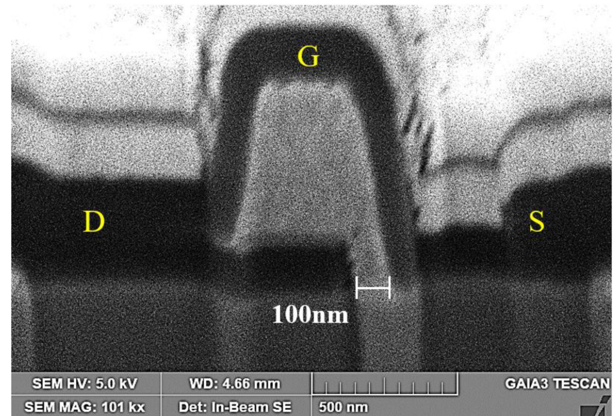

FIGURE 2. SEM image of the gate cross section with gate length of 100 nm.

The SEM image of the gate is shown in Fig. 2. The bottom of the gate is firmly deposited on the 100 nm opening and the top L_G distribution is defined by the lateral etching of SiN_x

layers [14]. The charges accumulated on the SiN_x surface edges may deflect the incoming ions, leaving a trapezoidal-shaped top gate [15].

III. RESULTS AND DISCUSSION

The I_{DS}-V_{GS}, I_{DS}-V_{DS} and pulsed I_{DS}-V_{DS}, and the transfer characteristics in semi-log scale at V_{DS}=10 V and 1 V of the 2×25 μm AlGaN/GaN HEMT with a L_G of 100 nm, a source-drain spacing (L_{SD}) of 2.250 μm, a gate-drain spacing (L_{GD}) of 1.425 μm, and a gate-source spacing (L_{GS}) of 0.725 μm, as shown in Fig. 3 (a), (b), and (c) respectively.

With the 2-Step Photolithography Process, a maximum drain-source current density of 1004.2 mA/mm and a peak extrinsic transconductance of 363.6 mS/mm were measured. The AlGaN/GaN HEMT DC performance shows the potential of using the proposed lithography method to realize high RF performance Ka band transistors.

The I_{DS}-V_{DS} curves for the 100-nm device with and without pulsed biases ($V_{GS,Q}$ =0V, $V_{DS,Q}$=0V) have been measured and shown in Fig. 3 (b), which show little current dispersion. The pulsed I_{DS}-V_{DS} measurement has a pulse width of 200 ns and a duty cycle of 0.1%. The applied pulse width of 200 ns is shorter than the time constant of most traps, therefore could eliminate thermal and trap effects [36].

Fig. 3 (d) shows the transfer characteristics in semi-log scale at V_{DS}=10 V and 1 V of the 2×25 μm AlGaN/GaN HEMT. In this study, drain induced barrier lowering (DIBL) is defined as $\Delta V_{th}/\Delta V_{DS}$ with V_{th} defined as the gate voltage at I_{DS}=1 mA/mm. A DIBL value of 15 mV/V is further extracted from V_{DS}=10 V and 1 V, showing an increased DIBL due to smaller gate length and smaller gate-to-channel aspect ratio compared to the 150 nm devices [35].

DC mapping for 2×25 μm devices was done to confirm the high wafer uniformity of the 4-inch wafer fabrication with the Stepper lithography, and is shown in Fig. 5. The I_{DSS}, G_m and V_{th} mapping results were shown in Fig. 4(a), (b), and (c), respectively. More than 85% of the AlGaN/GaN HEMTs on the wafer exhibited an I_{DSS} value between 910 to 1000 mA/mm. More than 90% of the AlGaN/GaN HEMTs on the wafer exhibited a G_m value between 310 to 350 mS/mm and more than 95% of the AlGaN/GaN HEMTs on the wafer exhibited a V_{th} value between −4.0 to −3.4 V. The high uniformity is attributed to both the reproducibility of the Stepper Lithography [10] and the simplicity of the 2-Step Photolithography Process.

The device off-state breakdown voltage is measured as shown in Fig. 10. The three terminal breakdown voltage measurement were done on a 2-step photolithography HEMT device with 2×25 μm gate width, L_{SD}=2.25 μm. The device shows a breakdown voltage at I_{DS}=1 mA/mm of 64 V at off-state (V_{GS}= −5 V), which demonstrates the potential of GaN HEMT device for high power Ka-band applications.

To investigate the RF characteristics of the AlGaN/GaN HEMTs with the 2-Step Photolithography Process, S parameter results of the AlGaN/GaN HEMT and large signal characteristics of a the AlGaN/GaN HEMT at 28GHz were examined.

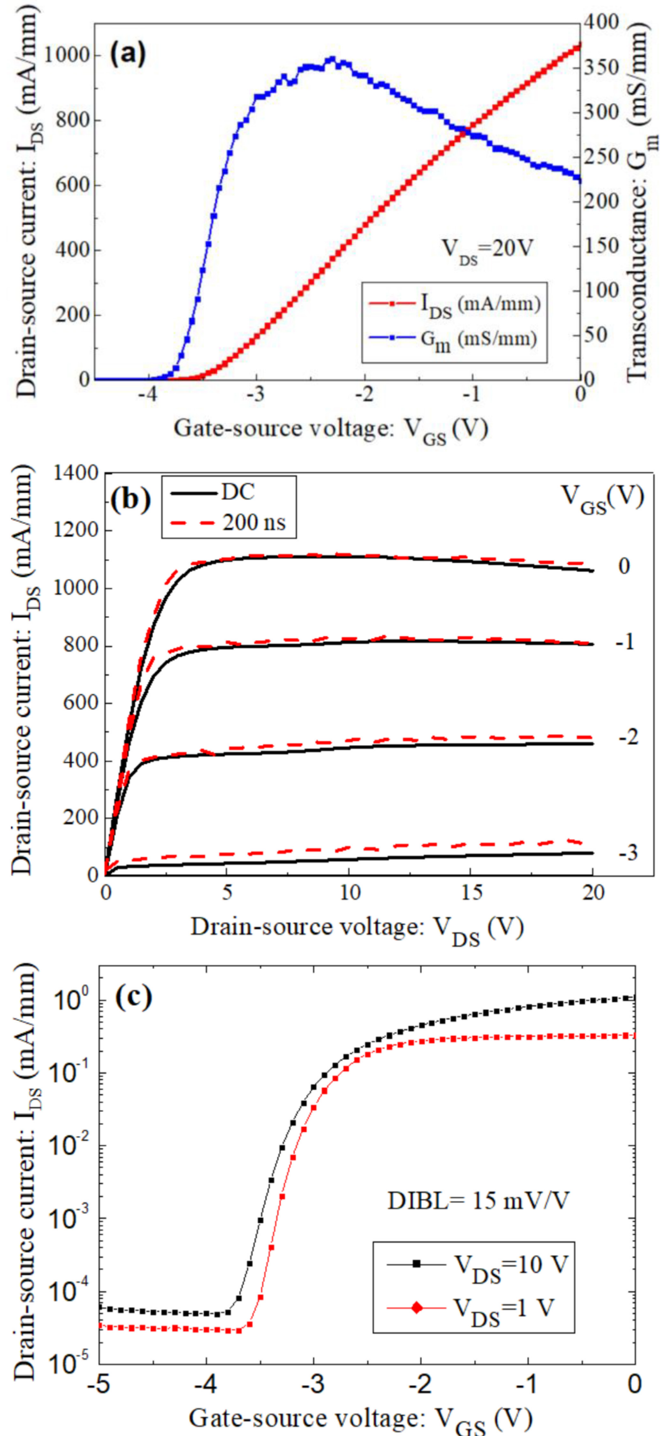

FIGURE 3. (a) I_{DS}-V_{GS}, (b) I_{DS}-V_{DS} and pulsed I_{DS}-V_{DS} curves, and (c) the transfer characteristics in semi-log scale at V_{DS}=10 V and 1 V of the 2×25 μm AlGaN/GaN HEMT.

S-parameters results were measured on-wafer using the N5227B PNA Microwave Network Analyzer and shown in Fig. 8 after de-embedding. The system was calibrated with a

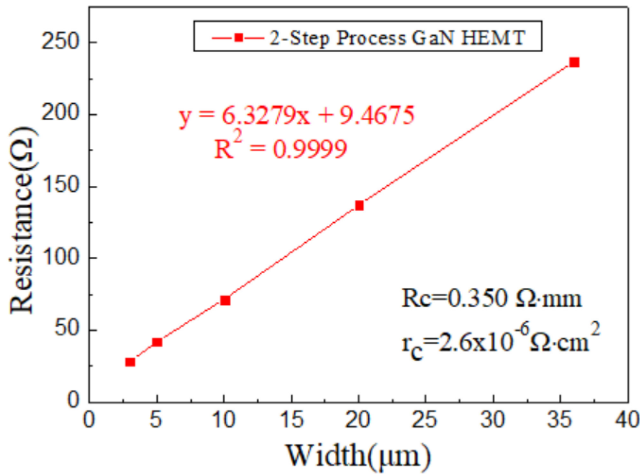

FIGURE 4. TLM results of the AlGaN/GaN HEMT for the 2-Step Photolithography Process.

short-open load-through calibration standard. The calibration accuracy was verified by insuring that both S_{21} and S_{12} of the through standard are less than ±0.01 dB and that both S_{11} and S_{22} are less than −45 dB within the measured frequency range after calibration [30].

The current gain cut-off frequency (f_t) of 63 GHz, the unilateral power gain (U) curve, and the maximum oscillation frequency (f_{max}) of 171 GHz for the 2×50 μm AlGaN/GaN HEMT with L_{SD}=2.5 μm using the 2-Step Photolithography Process are shown in Fig. 8.

For large signal characteristics, the 3dB compression point power density ($P_{OUT(P3dB)}$) of 4.3 W/mm, maximum power density ($P_{OUT\ (Pmax)}$) of 10.8 W/mm, and maximum PAE of 51.1% of the 2×25 μm device with L_{SD}=2.25 μm were measured at V_{DS} = 20 V and V_{GS}=−1.58 V (I_{DS}= 460 mA/mm) in Continuous Wave (CW) mode Load Pull measurement, as shown in Fig. 6.

28 GHz CW mode Load-pull measurement tests have also been performed on the 2×50 μm, 8×50 μm, and 8×75 μm devices, as shown in Fig. 7 (a), (b), and (c). The 2×50 μm device with L_{SD}=2.5 μm measured at a bias of V_{DS}=28 V and V_{GS}=−1.66 V (I_{DS}=41.1 mA/mm) exhibits an output power density of 8.1 W/mm. The 8×50 μm device with L_{SD}=2.5 μm measured at a set bias of V_{DS}=28 V and V_{GS}=−2.5 V (I_{DS}=252.5 mA/mm) exhibits an output power of 1.85 W. Moreover, to further increase the output power performances of the 2-Step Process devices, the 8×75 μm device with L_{SD}=3.0 μm and with the increased gate width of 25 μm compared to the 8×50 μm devices have been fabricated and has demonstrated an output power of 2.25 W under 28 GHz load pull measurements with V_{DS}=28 V and V_{GS}=−2.6 V (I_{DS}=233.3 mA/mm).

The RF performance of these devices shows the capability of the 2-Step Photolithography Process to be applied on larger gate periphery devices, while maintaining high wafer yield through a high uniformity analyzation. The decrease of the output power density of the 2-Step devices

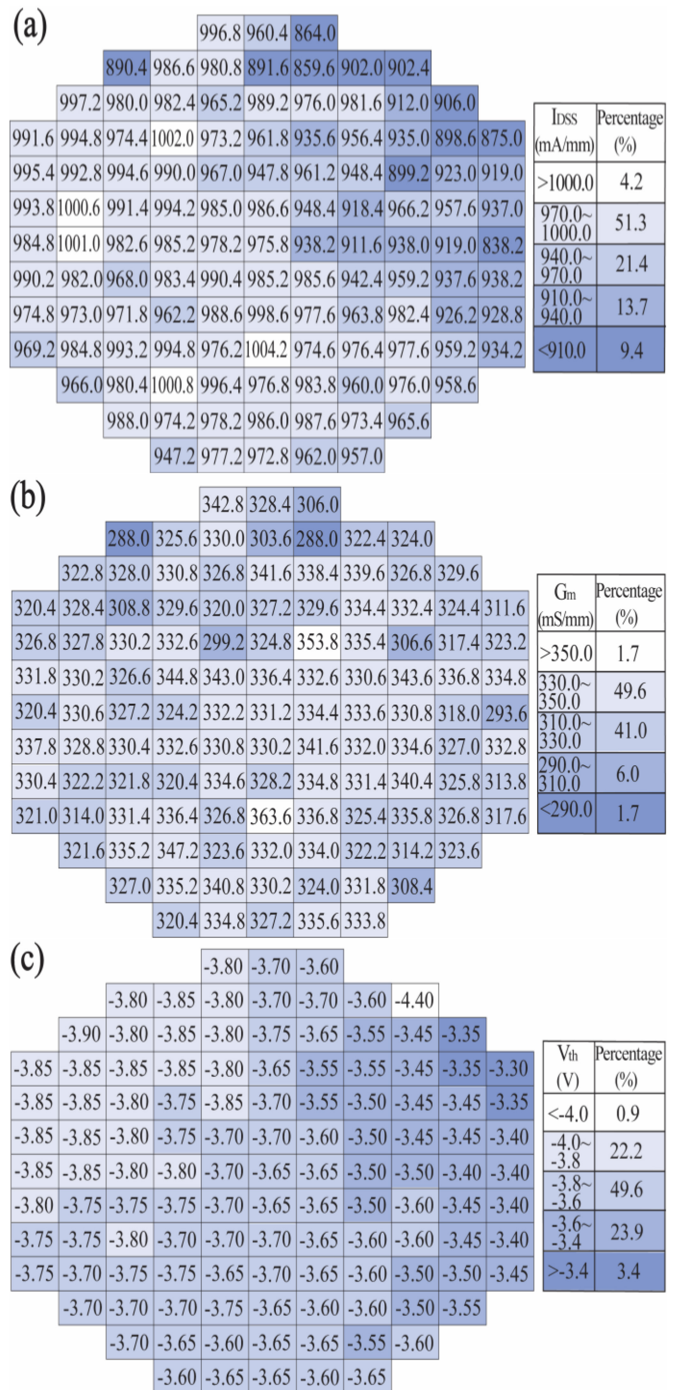

FIGURE 5. The 4-inch wafer uniformity of a 2×25 μm device on (a) I_{DSS} value, (b) G_m value and (c) V_{th} value.

with increased device single gate width may result from the increased gate resistance (R_g). The effect of gate width concerning the R_g has been done in detail by Palacios et al. [31]. Palacios et al. shows that for AlGaN/GaN HEMT devices, the R_g scales linearly with the gate width for a device with gate lengths of around 150 nm, and has an important effect on the device RF performances, such as f_{max}.

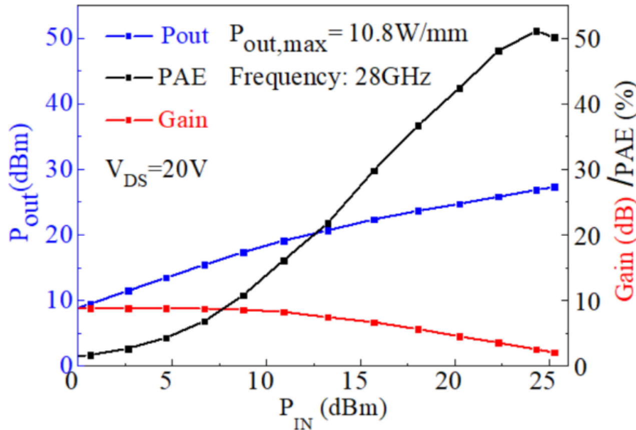

FIGURE 6. Large signal results of a 2×25 μm AlGaN/GaN HEMT for the 2-Step Photolithography Process.

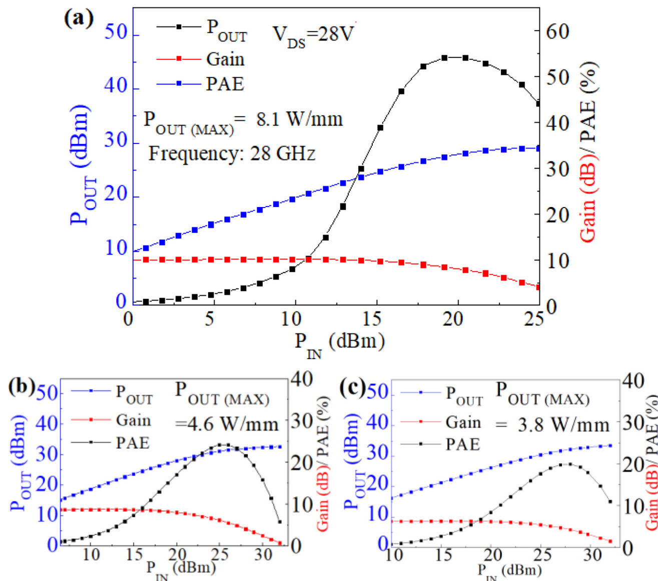

FIGURE 7. Large signal results of the (a) 2×50 μm, (b) 8×50 μm, (c) 8×75 μm AlGaN/GaN HEMTs for the 2-Step Photolithography Process.

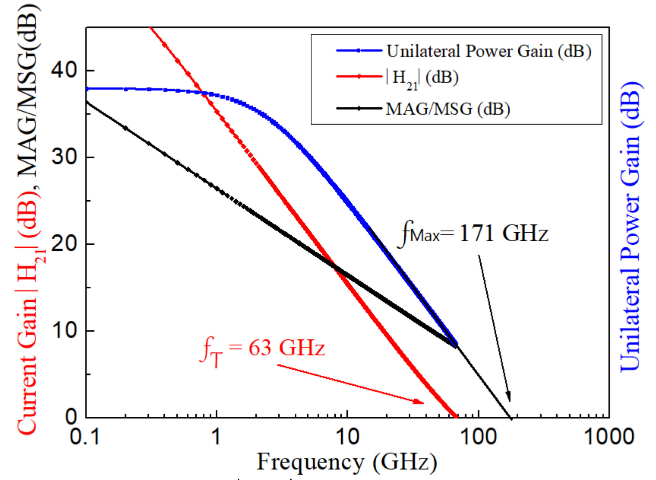

FIGURE 8. Current-gain $|H_{21}|$, unilateral power gain (U), and MAG/MSG vs. Frequency plot for the 2×50 μm AlGaN/GaN HEMT with the 2-Step Photolithography Process.

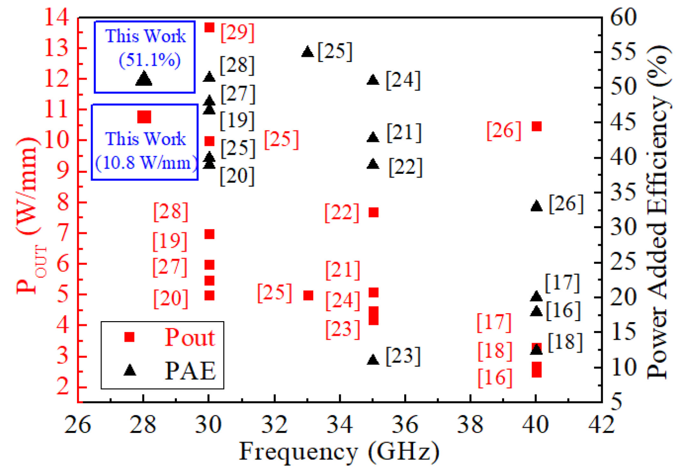

FIGURE 9. Benchmark of the 2-Step device and published results.

The effects of gate width on f_t and f_{max} are also discussed with the small signal of the 2×50 μm and 8×50 μm devices. The f_t and f_{max} values of 43 GHz and 200GHz, respectively, for the 8×50 μm AlGaN/GaN HEMT are shown in Fig. 11.

Compared to the 2×50 μm device in Fig. 8, the 8×50 μm device exhibits a lower f_t value, which may be due to increased gate capacitance from the larger gate width. However, the 8×50 μm device has a higher f_{max} value, which is mainly due to the reduced R_g from increased gate fingers [34].

The decrease of output power density of the devices with more gate fingers in this study may be due to the increase of self-heating effect [32], showing that the increase of self-heating effects with gate fingers during on-wafer measurement reduces the output power density of the SiC MESFET devices, despite the high thermal conductivity of SiC substrates.

The RF power performance of the device with a highest output power density in this study is compared with other published results, as shown in Fig. 9. At Ka-Band, the RF results of a 2×25 μm using the 2-Step Photolithography Process exhibited an outstanding $P_{OUT\ (MAX)}$ among representative published papers. The RF power characteristic shown in this work exhibits over 50% PAE, and a record high output power density of 10.8 W/mm for devices fabricated using only the stepper phtolithography system for L_G definition. Within published Ka band frequency devices [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], the output power density of this work not only standout among state-of-the-art results, but also shows potential for the mass production of high output power density GaN HEMT wafers without using the conventional E-beam lithography system.

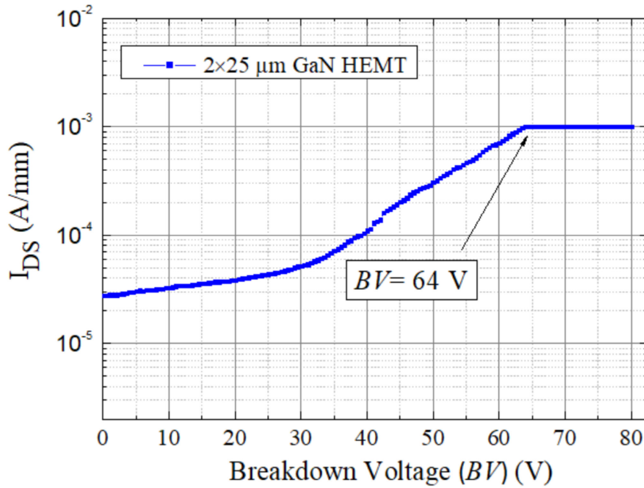

FIGURE 10. Breakdown Voltage measurement result of the 2×25 μm HEMT device at $V_{GS} = -5$ V.

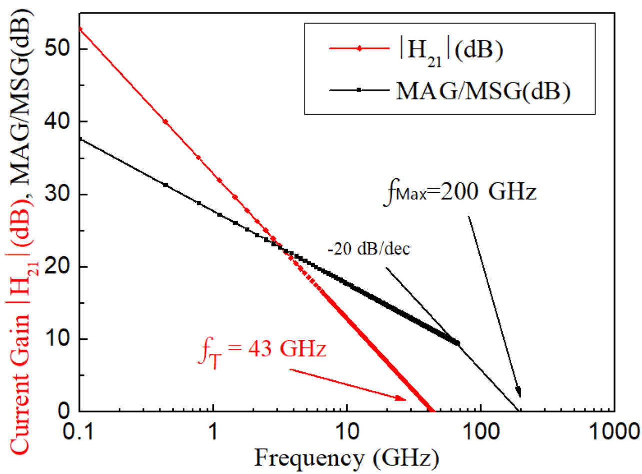

FIGURE 11. Current-gain $|H_{21}|$ and MAG/MSG vs. Frequency plot for the 8×50 μm AlGaN/GaN HEMT with the 2-Step Photolithography Process.

IV. CONCLUSION

We have demonstrated AlGaN/GaN HEMTs fabricated by the Stepper Lithography, and with the 2-Step Photolithography Process, we have achieved small gate lengths and achieved high wafer uniformity on the 4-inch wafer with high I_{DSS}, G_m and V_{th} values. At V_{DS} = 20 V, the AlGaN/GaN HEMT exhibits an I_{DSS} of 1004.2 mA/mm, a G_m value of 363.6 mS/mm, a maximum output power density ($P_{OUT\ (MAX)}$) of 10.8 W/mm, and a power gain of 8.8 dB with a maximum Power-added efficiency (PAE) of 51.1% at 28 GHz in CW mode. Overall, the high wafer uniformity and the outstanding RF power performance together makes the process applicable for Ka-band device fabrication, and has the potential to mass production on 6- and 8-inch wafers.

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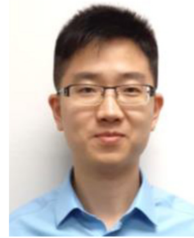

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