Received 7 April 2023; accepted 4 May 2023. Date of publication 9 May 2023; date of current version 15 May 2023.
The review of this article was arranged by Editor M. T. A. Rahimo.

Digital Object Identifier 10.1109/JEDS.2023.3274133

Four Hybrid Gates SOI Lateral Insulated Gate Bipolar Transistor With Improved Carrier Controllability

JIE MA[1], YONG GU[1], CHENGWU PAN[1], LONG ZHANG[1] (Member, IEEE), GUIQIANG ZHENG[1], SIYANG LIU[2] (Member, IEEE), WEIFENG SUN[2] (Senior Member, IEEE), CHANGYUAN CHANG[1], AND SEN ZHANG[3]

1 National ASIC System Engineering Research Center, School of Microelectronics, Southeast University, Nanjing 210096, China
2 National ASIC System Engineering Research Center, School of Electronic Science and Engineering, Southeast University, Nanjing 210096, China
3 Department of Technology Design, CSMC Technologies Corporation, Wuxi 214061, China

CORRESPONDING AUTHORS: L. ZHANG AND S. LIU (e-mail: longzh@seu.edu.cn; liusy2017@seu.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 62274032 and Grant 62174029; in part by the Distinguished Young Scholars Program, Southeast University under Grant 2242022R40010; and in part by the Technological Achievements of Jiangsu Province under Grant BA2022005.

ABSTRACT Easy inter-connection is a crucial advantage of the single-chip power ICs, which makes power devices with multiple ports easy to improve carrier controllability without increasing process difficulty. Electrical characteristics of the power devices get further improved thanks to the advanced carrier controllability. In this paper, a silicon-on-isolator lateral IGBT (SOI-LIGBT) featured four hybrid gates is proposed to obtain outstanding carrier controllability in turn-on, turn-off and short-circuit conditions for the first time. Four hybrid gates include three planar gates (G_1, G_2 and G_3) and a trench gate (G_4), of which G_3 and G_4 are grounded gate to lower saturation current and suppress latch up. Low turn-off time (t_{OFF}), di/dt and improved short-circuit withstanding capability are obtained through providing different input signals to these gates. In the turn-on, G_2 is pre-charged to a stable voltage equal to gate voltage (V_{G1}) to suppress the high di/dt before V_{G1} starts to rise. In the turn-off, a P-type inversion is induced by the negative voltage of G_2 (V_{G2}), which provides a low-resistance hole current path to extract the stored holes. In the short-circuit condition, G_3 and G_4 are both shorted to the ground to lower the saturation current and suppress the activation of parasitic NPN transistor, resulting in an improved short-circuit withstanding time (t_{SC}). Compared with the conventional SOI-LIGBT, t_{OFF} and di/dt are reduced by 43.6% and 53.08%, and t_{SC} is prolonged from 3.04μs to 8.89μs at DC bus voltage of 400V.

INDEX TERMS Hybrid gates, carrier controllability, turn-on, di/dt, turn-off time, short-circuit, short-circuit withstanding time, SOI, lateral IGBT, LIGBT, SOI-LIGBT.

I. INTRODUCTION

Single-chip power IC is popular for its significant advantage of easy inter-connection [1], [2], [3]. Many power devices featured multiple ports or integrating MOS and diodes can be manufactured to obtain better carrier controllability. Advanced carrier controllability, such as adjusting local carrier concentration, changing current path and enhancing or suppressing the effect of moving carriers, is the root of improving electric characteristics in power stage devices.

Recent years, many novel IGBTs with multiple ports or integrated devices have been reported to improve the carrier controllability in different transients. In the turn-on transient, better dv/dt or di/dt controllability can be achieved by controlling the hole concentration beside gate polysilicon [4], [5] or suppressing the effect of displacement current on gate voltage [6], [7]. In the turn-off transient, fast electron/hole extraction or decreasing stored carriers is crucial to achieve low turn-off loss (E_{OFF}). Short anode technology [8], [9] is a common method to accelerate the electron

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

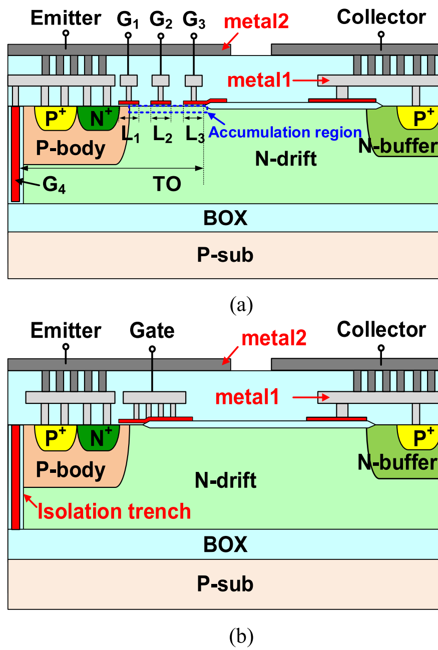

FIGURE 1. (a) Cross-section view of the proposed SOI-LIGBT with four hybrid gates and (b) the conventional SOI-LIGBT.

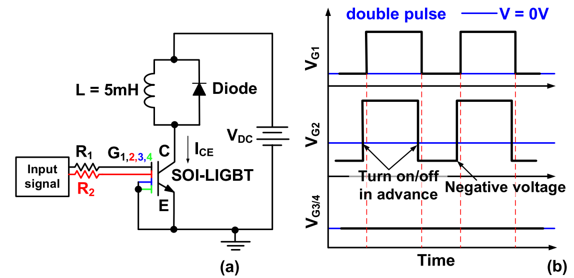

FIGURE 2. (a) The equivalent circuit and (b) input signals of hybrid gates for double pulse clamped inductive switching measurement and simulation.

extraction by adopting a N+ region in the collector side, however, resulting in a snapback. Then, a small-scale circuit composed of MOSFETs or diodes is added to further control the extraction of carriers without snapback in [9], [10], [11]. SOI-LIGBTs with inserted dual or triple deep oxide trenches in the N-drift are reported in [12], [13], [14] to achieve a better trade-off between on-state voltage (V_{ON}) and E_{OFF} by enhancing the conductivity modulation in the on-state and assisting in voltage sustaining in the off-state. In the short-circuit condition, the most failures of devices are attributed to the activation of parasitic transistor, and adjusting hole current path is an efficiency way to suppress the latch up. The most effective approach to prevent the latch up is lowering the saturation current (*Isat*) through employing series diodes or MOSs to extract holes in drift region [15], [16], [17].

In this paper, a novel four gates SOI-LIGBT with outstanding carrier controllability is proposed and investigated. In Section II, the structure and main key design parameters of the proposed SOI-LIGBT are illustrated. The mechanism of carrier controllability in the turn-on, turn-off and the short-circuit conditions are discussed through TCAD simulations. In Section III, the improvement of electrical characteristics in the proposed SOI-LIGBT is verified through the double-pulse switching and short-circuit measurements.

II. STRUCTURE AND MECHANISM

The cross-section view and the key design parameters of the proposed SOI-LIGBT are shown in Fig. 1 (a). Four hybrid gates, three planar gates (G_1, G_2, G_3) and a trench gate (G_4), are adopted in the proposed SOI-LIGBT. Three planar gates are formed by one-step etching after the deposition of polysilicon. G_1 is responsible for the formation of the inversion channel. G_2 - G_4 play a role of improving carrier controllability, and G_4 also acts as an isolation trench. The length of G_1, G_2, and G_3 is L_1, L_2 and L_3, respectively. G_4 is filled by the polysilicon that is surrounded by 80nm-thick sidewall oxide, and the polysilicon is connected to the emitter by interconnection metal. The distance from right side of G_4 to the left-side bird's beak is TO. The thickness and the length of the N-drift region are 18μm and 45μm, respectively, and the thickness of the BOX is 3.5μm. As shown in Fig. 1 (b), a conventional SOI-LIGBT with only one planar gate is fabricated for comparation.

Fig. 2 (a) shows the schematic circuit for double pulse clamped inductive switching measurement and simulation. The input signals are transmitted to G_1 and G_2 through series resistors R_1 and R_2 (R_1>>R_2), respectively. In this work, R_1 is set as 200?, and the R_2 is set as 1/100 of R_1. G_3 and G_4 are shorted to the emitter directly. Inductive load of 5mH is used and a fast recovery diode is anti-parallel to the inductance as freewheeling diode. As shown in Fig. 2 (b), two different input signals (V_{G1} and V_{G2}) of double pulse are applied to G_1 and G_2. V_{G1} and V_{G2} have the same positive voltage of 15V, and the low-level voltages of V_{G1} and V_{G2} are 0V and ~ -5V, respectively. Moreover, V_{G1} is delayed by $\sim 1\mu s$ than V_{G2}.

In the turn-on transient, for conventional SOI-LIGBT, holes injecting from collector will elevate the electric potential in the accumulation region (shown in Fig. 1 (a)), and the displacement current composed of these holes can overcharge gate, resulting in high di/dt and gate overshoot (in Fig. 3 (a)) [7]. As shown in Fig. 3 (b), the hole density in the accumulation region in the turn-on transient decreases significantly when G_2 is pre-charged. Pre-charged G_2 has constant electric potential of 15V in advance, which can repel hole. In addition, G_2 is the part most seriously affected by holes in the accumulation region. Owing to the non-connection between G_1 and G_2 (shown in Fig. 1 (a)), G_1 is protected from the impact of G_2. Therefore, the impact of hole displacement current on G_1 is further weakened. To further verify the repulsion of G_2 to hole, G_2 is shorted to G_1 for comparation in TCAD simulation. Compared with SOI-LIGBT with pre-charged G_2, repulsion of G_2 to hole is weakened severely when G_1 and G_2 are shorted (red line).

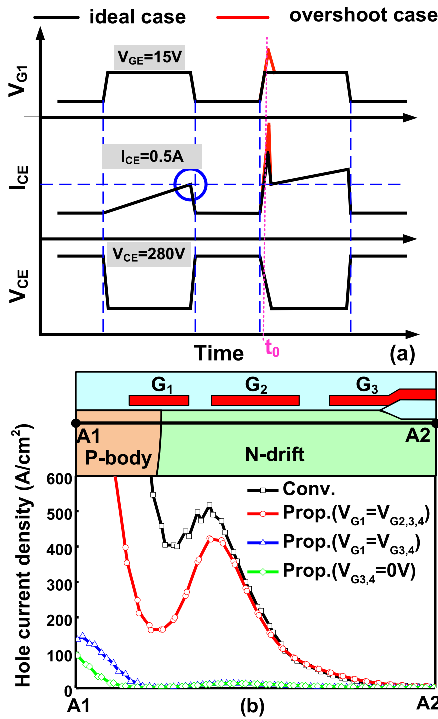

FIGURE 3. (a) Schematic turn-on curves of the conventional SOI-LIGBT at I_{CE} = 0.5A (b) Hole current distribution along line A1-A2 of the proposed and the conventional SOI-LIGBTs in the turn-on transient at V_G = 16.5V, V_{DC} = 150V (at t_0 time instant shown in Fig. 3 (a)).

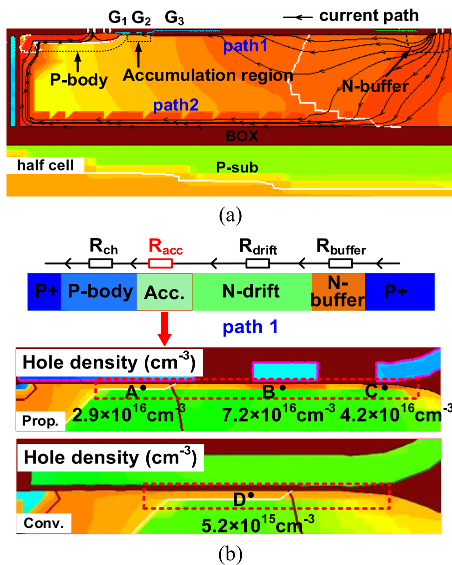

FIGURE 4. (a) Hole current paths in the turn-off at V_G = 15V and V_{DC} = 280V. (b) Equivalent resistance distribution model and hole density distribution at the emitter side of the proposed SOI-LIGBT in the turn-off transient.

Moreover, whether G_3 and G_4 are grounded (green line) or connected to G_1 (blue line) has no effect on the repulsion of G_2 to hole of G_2.

In the turn-off transient, V_{G2} falls firstly to negative voltage of −5V, and then G_1 starts to turn off as shown in Fig. 2 (b). Stored holes and electrons in the drift region are extracted to the emitter and the collector electrodes, respectively. As shown in Fig. 4 (a), most of holes are extracted from along path1. Fig. 4 (b) illustrates the equivalent resistance distribution model and hole density distribution in the turn-off transient. The equivalent resistance of path1 composes of channel resistance (R_{ch}), accumulation region resistance (R_{acc}), drift resistance (R_{drift}) and buffer resistance (R_{buffer}). Negative V_{G2} induces a hole accumulation layer in the accumulation region, which reduces R_{acc} significantly. The hole accumulation layer provides a low-resistance hole current path (path1), resulting in a reduced t_{OFF}.

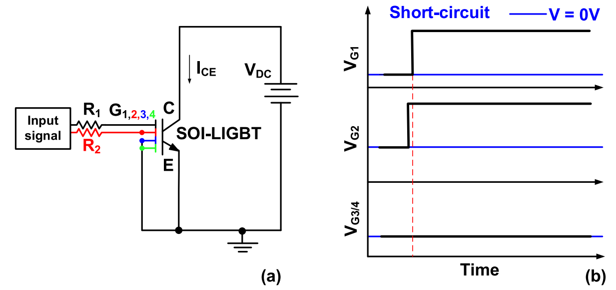

FIGURE 5. (a) The equivalent circuit and (b) input signals of hybrid gates for short-circuit measurement and simulation.

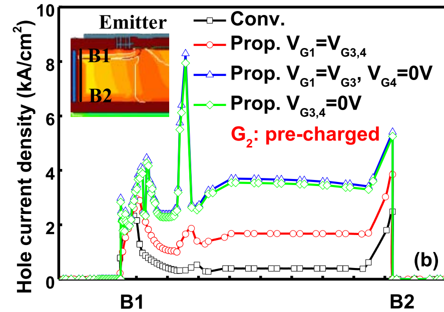

FIGURE 6. The hole density distribution along line B1-B2 of the proposed and the conventional SOI-LIGBT in the short-circuit condition at J_{CE}=450A/cm^2, V_{DC} = 400V and V_G=15V.

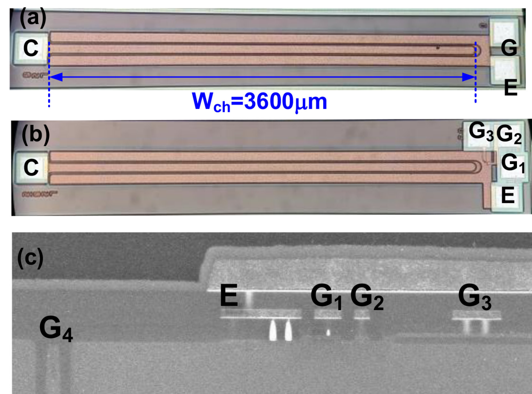

FIGURE 7. Photos of the fabricated (a) proposed and (b) conventional SOI-LIGBTs. (c) The SEM photo of four gates in the proposed SOI-LIGBT.

As shown in Fig. 5 (a) and Fig. 5 (b), G_3 and G_4 are shorted to the ground in the short-circuit measurement and

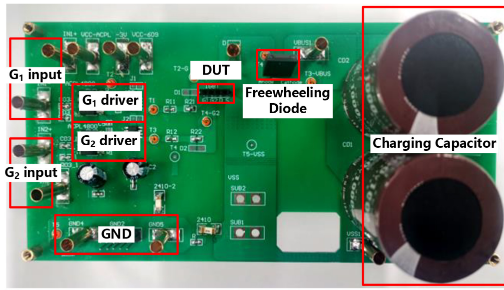

FIGURE 8. The printed circuit board for double pulse clamped inductive switching measurements and short-circuit measurements.

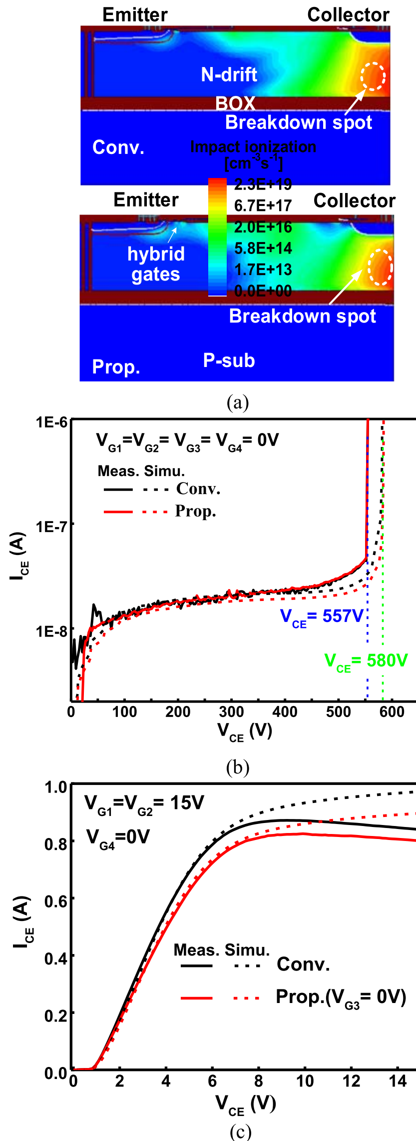

FIGURE 9. (a) Impact ionization distributions of the conventional and the proposed SOI-LIGBTs. Measured (b) off-sate and (c) on-state I-V curves of the fabricated devices with different gate connections at room temperature.

simulation. The injection effect in the accumulation region is weakened considerably due to the grounded G_3. The *Isat* of the proposed SOI-LIGBT is lower than that of the conventional SOI-LIGBT when G_3 is grounded. In addition, holes from P+ collector are attracted to the grounded G_4 in the short-circuit condition as shown in Fig. 6. More holes flow along G_4 at same current rating, which can suppress the activation of parasitic NPN transistor. However, the attraction of G_4 to holes is greatly weakened when G_4 is connected to G_1 or floating (conventional SOI-LIGBT). Compared with the conventional SOI-LIGBT, the proposed SOI-LIGBT with grounded G_3 and G_4 obtains a significantly improved short-circuit withstanding capability.

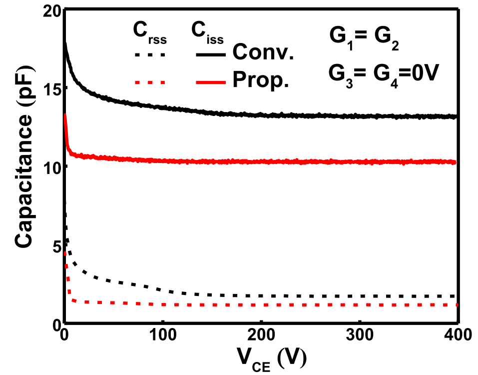

FIGURE 10. Measured C-V curves of the proposed and the conventional SOI-LIGBTs.

III. MEASUREMENT RESULTS

In order to verify the improved carrier controllability of the proposed SOI-LIGBT with hybrid gates, devices are fabricated at TO = 13μm, L_1 = 3μm, L_2 = 1.1μm, and L_3 = 0.9μm on the 550V SOI Bipolar-CMOS-DMOS-IGBT platform, in which SOI-LIGBT and driver circuits can be integrated in a single chip. Photos of fabricated proposed and conventional SOI-LIGBTs are shown in Fig. 7 (a) and Fig. 7 (b). The SEM photo of four gates in the proposed SOI-LIGBT is shown in Fig. 7(c). Three planar gates are connected to pads through interconnection metal, respectively. G_4 is connected to emitter directly. The total device width of fabricated samples is 3600μm.

In Fig. 8, a special printed circuit board is designed for double pulse clamped inductive switching measurement and short-circuit measurement. Two input signals provided by a signal generator (Tektronix AFG3102C) are applied to G_1 and G_2. In addition, the driver chip to drive G_2 supports negative voltage, and the negative voltage is provided by a Keithley source meter. A commercial fast recovery diode is used as freewheeling diode in the double pulse clamped inductive switching measurement, while shorted in the short-circuit tests. After each measurement, a fresh sample is used in the next measurement. It should be pointed out that driver circuits used in the printed circuit board and SOI-LIGBT can be integrated in a single chip, and thus the gate input signals can be provided easily.

As shown in Fig. 9 (a), the starting positions of avalanche of the conventional and proposed SOI-LIGBTs both locate at the bottom of the collector side, and the breakdown point

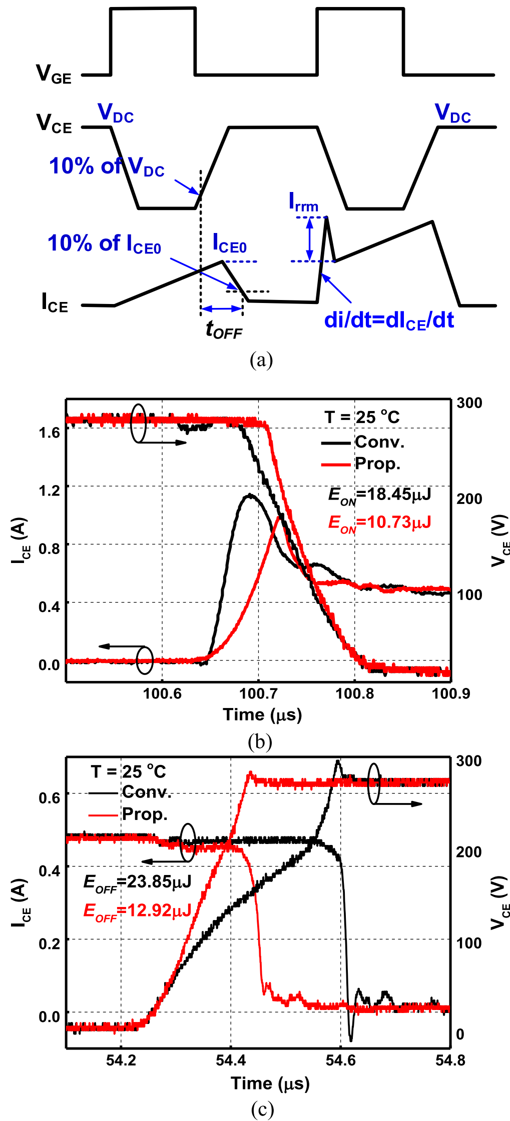

FIGURE 11. **(a) Definition of turn-off time (t_{OFF}), maximum reverse recovery current (I_{rrm}) and di/dt. Curves of the conventional and the proposed SOI-LIGBTs in the (b) turn-on and (c) turn-off transients.**

is indeed far from hybrid gates in the proposed SOI-LIGBT. Thus, the conventional and proposed SOI-LIGBTs have the similar impact ionization rate distributions and breakdown voltage (*BV*). Fig. 9 (b) shows the measured and simulated off-state I-V curves of fabricated devices at the room temperature. Adopting separated gates in the proposed SOI-LIGBT has no effect on the *BV*. The proposed and the conventional devices obtain the same *BV* of 557V. Fig. 9 (c) shows the measured and simulated on-state I-V curves. The electron accumulation effect is weakened at $V_{G3} = 0\text{V}$, which results in a low *Isat* and an increased V_{ON}.

Input capacitance (C_{iss}) and reverse transfer capacitance (C_{rss}) of the conventional and the proposed SOI-LIGBTs are measured at frequency of 1MHz. As shown in Fig. 10, the proposed SOI-LIGBT obtains reduced C_{iss} and C_{rss} at $V_{CE} = 280\text{V}$ thanks to the split gates. Fig. 11 (a) shows the

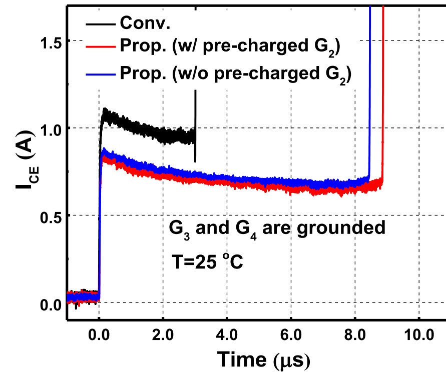

FIGURE 12. **Short-circuit curves of the conventional and the proposed SOI-LIGBTs at $V_{DC} = 400\text{V}$.**

definition of turn-off time (t_{OFF}), maximum reverse recovery current (I_{rrm}) and di/dt. The proposed and the conventional devices begin to turn off at $V_{DC} = 280\text{V}$ and $I_{CE0} = 0.5\text{A}$. t_{OFF} is defined as the phase from the 10% of V_{DC} (28 V) to the 10% of I_{CE0} (0.05 A). I_{rrm} is defined as the difference between I_{CE} peak and I_{CE0}. di/dt is defined as the current change per unit time. Curves of the conventional and the proposed SOI-LIGBTs in the turn-on transient are shown in Fig. 11 (b). Thanks to the separated gates and pre-charged G_2, the effect of the displacement current composed of the holes in the accumulation region is significantly weakened in the proposed SOI-LIGBT. The proposed device exhibits a decreased di/dt and I_{rrm}. Compared with the conventional device, the proposed device obtains 53.08% reductions in di/dt and 23.8% reduction in I_{rrm}. Fig. 11 (c) shows the turn-off curves of the proposed and the conventional devices. The proposed device obtains a faster turn-off speed than the conventional device thanks to the low-resistance hole extraction path. As a result, the proposed device achieves 43.6% decrease in t_{OFF} and 41.8% reduction in E_{OFF} in comparison with the conventional device.

The fabricated devices are packaged to compare short-circuit withstanding capability. As shown in Fig. 5 (a), the packaged devices are measured with no load, thus the DC bus voltage (400V) is applied to the collector directly. The connections of hybrid gates are shown in Fig. 5 (b). Fig. 12 shows the short-circuit curves of the conventional and the proposed devices. The proposed devices are measured at the conditions of G_2 is pre-charged (w/ pre-charged G_2) and shorted to G_1 (w/o pre-charged G_2). Short-circuit withstanding times (t_{SC}) of the proposed device measured with and without pre-charged G_2 are improved to 8.46μs and 8.89μs, respectively. In summary, integrated platform can further improve the electric characteristics of a single power device by integrating circuits or other devices easily.

IV. CONCLUSION

Integration makes multi-port devices easy to control and improve carrier controllability. A novel structure with hybrid gates is proposed in this paper. Carrier controllability is

obviously improved in turn-on, turn-off and short-circuit conditions thanks to the separated gates and different gate input signals. Compared with the conventional SOI-LIGBT, the proposed SOI-LIGBT obtains 53.08% reduction in di/dt, 43.6% reduction in t_{OFF} and 225% improvement in t_{SC}. In addition, adjusting the length of G_1, G_2 and G_3 or the gate input signals may further improve the transient electric characteristics in different conditions, and it will be investigated in our future work.

REFERENCES

[1] K. Hara et al., “600V single chip inverter IC with new SOI technology,” in *Proc. 26th ISPSD*, Jun. 2014, pp. 418–421, doi: 10.1109/ISPSD.2014.6856065.

[2] W. Sun et al., “A novel silicon-on-insulator lateral insulated-gate bipolar transistor with dual trenches for three-phase single chip inverter ICs,” *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 693–695, Jul. 2015.

[3] A. Nakagawa, H. Funaki, Y. Yamaguchi, and F. Suzuki, “Improvement in lateral IGBT design for 500 V 3 A one chip inverter ICs,” in *Proc. 11th ISPSD*, May 1999, pp. 321–324, doi: 10.1109/ISPSD.1999.764125.

[4] W. Saito and S.-I. Nishizawa, “Alternated trench-gate IGBT for low loss and suppressing negative gate capacitance,” *IEEE Trans. Electron Device*, vol. 67, no. 8, pp. 3285–3290, Jun. 2020, doi: 10.1109/TED.2020.3002510.

[5] Y. Ikura, Y. Onozawa, and A. Nakagawa, “IGBT structure with electrically separated floating-p region improving turn-on dVak/dt controllability,” in *Proc. 30th ISPSD*, May 2018, pp. 168–171, doi: 10.1109/ISPSD.2018.8393629.

[6] K. Ohi et al., “Ultra low Miller capacitance trench-gate IGBT with the split gate structure,” in *Proc. 27th ISPSD*, May 2015, pp. 25–28, doi: 10.1109/ISPSD.2015.7123380.

[7] J. Ma et al., “Simulation study of novel trench gate U-shaped channel SOI lateral IGBTs with suppressed gate voltage overshoot and reduced di/dt,” *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 3930–3935, Aug. 2021, doi: 10.1109/TED.2021.3084578.

[8] W. Chen, B. Zhang, and Z. Li, “Area-efficient fast-speed lateral IGBT with a 3-D n-region-controlled anode,” *IEEE Electron Device Lett.*, vol. 31, no. 5, pp. 467–469, May 2010, doi: 10.1109/LED.2010.2043638.

[9] L. Sun, B. Duan, and Y. Yang, “Novel snapback-free SOI LIGBT with shorted anode and trench barriers,” *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2408–2413, May 2021, doi: 10.1109/TED.2021.3064790.

[10] H. Hu, M. Kong, J. Wu, B. Yi, and X. B. Chen, “A novel low turn-off loss and snapback-free reverse-conducting SOI-LIGBT with integrated polysilicon diodes,” *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4296–4301, Oct. 2019, doi: 10.1109/TED.2019.2936515.

[11] J. Wu, H. Huang, B. Yi, H. Hu, H. Hu, and X. B. Chen, “A snapback-free and low turn-off loss reverse-conducting SOI-LIGBT with embedded diode and MOSFET,” *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1013–1017, 2019, doi: 10.1109/JEDS.2019.2939223.

[12] L. Zhang et al., “Low-loss SOI-LIGBT with dual deep-oxide trenches,” *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3282–3286, Aug. 2017, doi: 10.1109/TED.2017.2712568.

[13] L. Zhang, J. Zhu, M. Zhao, S. Liu, W. Sun, and L. Shi, “Low-loss SOI-LIGBT with triple deep-oxide trenches,” *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3756–3761, Sep. 2017, doi: 10.1109/TED.2017.2731518.

[14] L. Zhang et al., “U-shaped channel SOI-LIGBT with dual trenches to improve the trade-off between saturation voltage and turn-off loss,” in *Proc. 29th ISPSD*, May 2017, pp. 291–294, doi: 10.23919/ISPSD.2017.7988961.

[15] H. Hu, M. Kong, B. Yi, and X. Chen, “A novel double-RESURE SOI-LIGBT with improved V_{ON}-E_{OFF} tradeoff and low saturation current,” *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 1059–1065, Mar. 2020, doi: 10.1109/TED.2020.2964944.

[16] B. Zhang, M. Kong, B. Yi, and X. Chen, “A novel no Miller plateau SOI-LIGBT with low saturation current and improved switching performance,” *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 2066–2070, May 2020, doi: 10.1109/TED.2020.2982656.

[17] B. Yi, J. Lin, B. Zhang, J. Cheng, and Y. Xiang, “Simulation study of a novel snapback free reverse-conducting SOI-LIGBT with embedded p-type Schottky barrier diode,” *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 2058–2065, May 2020, doi: 10.1109/TED.2020.2982615.