Received 8 April 2023; accepted 24 April 2023. Date of publication 27 April 2023; date of current version 4 May 2023.
The review of this article was arranged by Editor N. Collaert.

Digital Object Identifier 10.1109/JEDS.2023.3271063

Demonstration of HfO_2-Based Gate Dielectric With ~0.8-nm Equivalent Oxide Thickness on $Si_{0.8}Ge_{0.2}$ by Trimethylaluminum Pre-Treatment and Al Scavenger

MENG-CHIEN LEE [1,2], WEI-LUN CHEN [1,2], YI-YANG ZHAO [1,2], SHIN-YUAN WANG [1,2], GUANG-LI LUO [3], AND CHAO-HSIN CHIEN [1,2] (Member, IEEE)

1 Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan
2 Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan
3 Taiwan Semiconductor Research Institute, Hsinchu 30078, Taiwan.

CORRESPONDING AUTHORS: C.-H. CHIEN AND G.-L. LUO (e-mail: chchien@nycu.edu.tw; glluo@narlabs.org.tw)

This work was supported in part by the Ministry of Science and Technology, Taiwan, under Grant 109-2221-E-009-028-MY3.

ABSTRACT We disclosed HfO_2-based dielectric of superb electrical properties on p-type $Si_{0.8}Ge_{0.2}$ substrate using an interfacial layer (IL) formed by trimethylaluminum (TMA) pre-treatment and Al scavenger. Our results revealed that the interface trap density (D_{it}) value and the gate leakage current (J_G) could be improved about 60 times and 100 times by tuning the gate electrode composition without sacrificing equivalent oxide thickness (EOT) performance. The mechanism underlying the D_{it} improvement of the SiGe metal-oxide-semiconductor capacitors (MOSCAPs) might be owing to the Al metal scavenger and the minimization of the oxygen atoms diffusing to the high-κ/SiGe IL, verified by x-ray photoelectron spectroscopy (XPS) analyses. In addition, the hysteresis levels of SiGe capacitors with various gate electrodes were measured to find out the optimized configuration of metal electrodes. This work demonstrated the Al scavenger effect from the aspects of both material and electrical properties and achieved an impressive EOT value of ~0.8nm for the capacitors fabricated on the SiGe substrate.

INDEX TERMS Low EOT, Al scavenger, TMA pre-treatment, SiGe channel.

I. INTRODUCTION

As one of the high-mobility materials, SiGe is regarded as the most promising candidate for 3nm technology node and beyond, which possesses the lowest lattice mismatch with Si [1], [2], [3], [4], [5]. While different from Si substrates, SiGe substrates need a specific interface treatment to solve their interface issue, easily showing high interface trap density (D_{it}) due to surface Si and Ge atoms [6], [7], [8], [9], [10]. Therefore, our group studied the composition and quality of the $Si_{0.5}Ge_{0.5}$ interfacial layer (IL) by tuning the various IL annealing temperatures and fabricated the $Si_{0.8}Ge_{0.2}$ p-MOSFET with TMA pre-doping and NH_3 plasma IL treatment [11], [12]. The former research shows that the optimized IL annealing temperature might be 800 °C, and the 99.8% silicon oxide in IL could be obtained without relaxation and dislocation. The latter demonstrates that the IL of the SiGe device composed of Si–N and Al–O bonds could be the high-quality interface, exhibiting the low gate leakage current and high I_{on}/I_{off} ratio. However, IL thermal treatment and nitridation could not reach the equivalent oxide thickness (EOT) scaling less than 1 nm due to the thicker low-κ IL. As a result, to yield more drive current enhancement, the SiGe IL formation with low EOT and controlled leakage is highly desirable [13]. Recently, the SiGe gate stack composed of trimethylaluminum (TMA) interface treatment and in-situ high-dielectric Y_2O_3 deposition was reported to demonstrate the EOT scaling down to 1 nm with ultralow D_{it}, which could be attributed to the minimization of Ge-O bonds in $SiGeO_x$ ILs and the Y_2O_3 thickness reduction [14], [15]. However, the EOT value needs to be improved to meet the International Roadmap for Devices and Systems (IRDS) targets [16]. Hence, the advanced SiGe gate stack

utilizing the higher dielectric with low gate leakage current is urgently demanded.

On the other hand, our previous research reported that a high-quality SiGe interface could be achieved by inserting the barrier layer TiN metal and the oxygen-scavenging effect of the upper-metal Al [17]. Moreover, another group also demonstrates low-EOT performance through Ti scavenging effect [18]. However, the solid evidence of several studies about the high-performance according to the scavenging effect is deficient, which might be due to the complex analyses of the gate stack with metal-capped.

In this study, we successfully demonstrated the Al scavenging effect on the electrical characteristics of atomic layer deposition (ALD) HfO_2-based $Si_{0.8}Ge_{0.2}$ metal–oxide–semiconductor capacitors (MOSCAPs) using TMA pre-treatment for IL formation [14], [17]. We further fabricated SiGe capacitors with various gate electrode compositions to investigate the oxygen-scavenging process of the SiGe gate stacks due to the Al scavenging effect. In addition, x-ray photoelectron spectroscopy (XPS) would be employed to confirm the SiGe interface transition during various capping conditions. The electrical results revealed that the SiGe capacitor with TMA IL treatment and Al capping exhibited an ultralow EOT value of ~0.8 nm with a good gate leakage current.

II. EXPERIMENTAL DETAILS

A. SIGE CAPACITORS FABRICATION

The experiments involved a 100-nm-thick in-situ boron-doped $Si_{0.8}Ge_{0.2}$ layer that was epitaxially grown on (100) orientation p-Si wafer with a doping concentration of 1×10^{15} cm^{-3} by low-pressure chemical vapor deposition (LPCVD, ASM Epsilon-2000 Reactor). After diluted HF eliminated the native oxides, the samples were immediately transferred to an ALD system. The SiGe gate stacks, including different IL and HfO_2 thicknesses, were established by various cycle numbers of TMA pre-treatment followed by cyclic ALD with tetrakis(ethylmethylamino)hafnium and H_2O as precursors. A 50-nm-thick TiN was sputtered to form the reference electrode afterward. Moreover, to comprehensively investigate the effect of Al scavenger on the underneath SiGe gate stack, various metal compositions of Al and TiN were sputtered. Furthermore, a backside metal contact (Ti/Al) was formed to minimize the backside contact resistance. Finally, the follow-up post-metal annealing (PMA) at 300 °C for 1 min in N_2 ambient was performed for all SiGe samples.

B. SIGE CAPACITORS CHARACTERIZATION

The SiGe capacitors' multi-frequency capacitance-voltage (C–V) characterizations were measured at room temperature using an Agilent 4284A LCR meter. The hysteresis (ΔV_{FB}) was defined as the difference of Flat-band voltage (V_{FB}) extracted from the C–V curves measured at 500 kHz with opposite sweeping directions. Next, the D_{it} value was extracted by the conductance method at a temperature of 300 K [19]. Finally, the EOT value was calculated using the Schred simulator on the nanoHUB website [20], which considers the quantum confinement effect in the SiGe substrate.

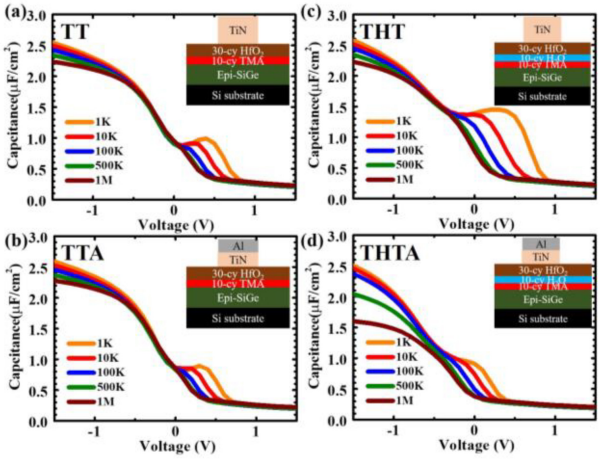

FIGURE 1. Multi-frequency C–V characteristics of the 30-cycle HfO_2/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ MOS capacitors with (a) only TiN (TT) and (b) Al/TiN (TTA) gate electrodes. Multi-frequency C–V characteristics of the 30-cycle HfO_2/10-cycle H_2O precursor/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ MOS capacitors with (c) only TiN (THT) and (d) Al/TiN (THTA) gate electrodes.

C. XPS SAMPLES PREPARATION

To investigate the effect of Al scavenger on the material composition of the underneath SiGe gate stack, XPS analyses were performed with an X-ray source of Al Kα (1486.6 eV). Moreover, to focus on the SiGe gate stacks, the XPS samples were soaked in APM (NH_4OH: H_2O_2: H_2O = 1:2:5) at room temperature for 25 minutes to remove the TiN metal and the Al metal above it [8].

III. RESULTS AND DISCUSSION

A. OXYGEN-SCAVENGING PROCESS OF AL METAL SCAVENGER

Figs. 1 (a)-(d) illustrate the multi-frequency C–V characteristics and the schematic diagrams of the $Si_{0.8}Ge_{0.2}$ MOS capacitors with different gate stacks and gate electrodes. For clarity, the samples were named by abbreviation according to their structures, as in Table 1. The purpose of varying the gate electrode structure and gate stack was to investigate the oxygen scavenging process caused by the presence of Al metal. To study the effect of metal engineering on the underlying gate stack, TiN of 50nm and Al/TiN of 25nm/25nm were deposited on different samples by sputtering. Moreover, an additional 10-cycle H_2O precursor was inserted in the deposition of the gate stacks in the THT and THTA cases during ALD to introduce more oxygen atoms. The extracted electrical parameters of SiGe capacitors are listed in Table 1, noting that all the samples were subjected to the PMA at 300 °C for 1 min in N_2 ambient.

We observed that, first, the cases with Al/TiN gate electrodes (TTA and THTA) showed smaller humps at the depletion region, exhibiting better interface quality obtained

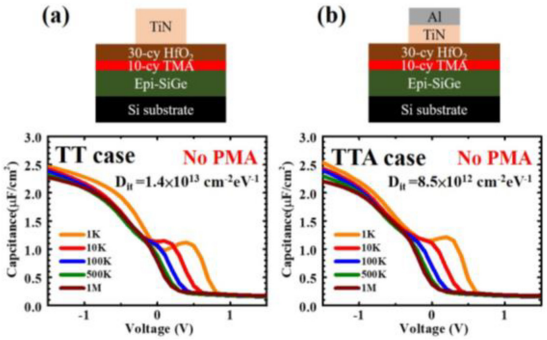

FIGURE 2. 1 kHz–1 MHz C-V characteristics of the unannealed 30-cycle HfO_2/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ MOS capacitors with (a) only TiN of 50 nm and (b) Al/TiN of 25nm/25nm.

through the scavenging process; the TTA case exhibited a relatively low EOT value of less than 1nm and a smaller D_{it} value of ~3.8 x 10^{12} $cm^{-2}eV^{-1}$. Second, the THTA case showed more significant frequency dispersion at the accumulation region, which might result from the series resistance effect due to the Al oxide formed on top of the TiN metal [21]. More significant frequency dispersion also proved that the oxygen atoms in the gate stack would be driven through the scavenging effect. In contrast, the TT and THT cases without Al capping displayed the individual humps at the depletion region, implying the TiN metal was unable to induce the oxygen scavenging process and the high-κ/SiGe interface quality was sensitive to the oxygen atoms.

In order to figure out when the oxygen scavenging occurred during our processing, PMA was skipped for the TT and TTA samples. Figs. 2 (a)-(b) illustrate the corresponding multi-frequency C–V characteristics of the $Si_{0.8}Ge_{0.2}$ MOS capacitors. We clearly saw that the TT case without the PMA process depicted distinct frequency dispersion behavior in the C-V curves that the low-frequency (1 kHz) CV curve did not merge with other curves at the gate voltage of −1V to 0 V, indicating the worse interface quality. In addition, a higher D_{it} value of ~1.4 × 10^{13} $cm^{-2}eV^{-1}$ of the SiGe MOSCAP was obtained showing the interface deterioration during TiN sputtering [22]. On the other hand, as the Al/TiN was adopted, the SiGe interface could be slightly cured owing to the elimination of oxygen atoms at the high-κ/SiGe interface by scavenging process [23] as shown in Fig. 2 (b). Upon PMA, the capacitors then revealed better frequency dispersion in the C-V curves and lower D_{it} values, which might manifest that the scavenging does happen during the PMA process [24], [25].

In order to further investigate the scavenging effect from the perspective of the material interaction at the SiGe gate stack by the XPS analyses, the overlying metal must be removed without affecting the underlying high-dielectric. Therefore, the soaking in APM solution (NH_4OH: H_2O_2: H_2O = 1:2:5) at room temperature for 25 minutes was implemented to dispose of the TiN and Al metals. Fig. 3

TABLE 1. Extracted electrical characteristics of SiGe MOS capacitors with different gate stacks and gate electrodes.

	Gate-stack	C_{acc} (μF/cm²)	EOT(nm)	D_{it} ($cm^{-2}eV^{-1}$)	J_g @V= -1.5V (A/cm²)
TT	TiN/HfO_2/TMA-IL/SiGe	2.34	1	4.5×10^{12}	1.9×10^{-3}
TTA	Al/TiN/HfO_2/TMA-IL/SiGe	2.42	0.96	3.8×10^{12}	1.6×10^{-3}
THT	TiN/HfO_2/H_2O/TMA-IL/SiGe	2.34	1	1.2×10^{13}	8.2×10^{-3}
THTA	Al/TiN/HfO_2/H_2O/TMA-IL/SiGe	2.04	1.28	4.6×10^{12}	1.7×10^{-3}

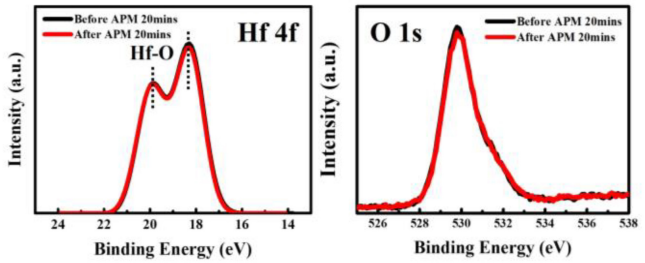

FIGURE 3. XPS spectra of Hf 4f and O 1s of the 30-cycle HfO_2/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ stack structures with and without soaking in APM (NH_4OH: H_2O2: H_2O = 1:2:5) at room temperature for 20 minutes.

displays the XPS spectra of O 1s and Hf 4f of the 30-cycle HfO_2/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ stack structures before and after soaking in the APM solution, which was employed to confirm whether or not the APM liquid would substantially affect the properties of the HfO_2 dielectric. The results confirmed that the HfO_2 dielectric was not detectably attacked after immersing in the APM solution for 25 minutes. Consequently, we applied this approach to remove the gate electrodes of the samples for the XPS analyses.

As mentioned above, the oxygen scavenging action caused by Al metal occurred through the PMA process. On purpose to have deep insight into the material interaction of the Al scavenging effect, the annealed and unannealed stack structures of the Al/TiN/30-cycle HfO_2/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ were used for the XPS analyses with removing the gate electrodes first by the APM solution; the condition for the annealed on was 300 °C PMA for 1 minute. Figs. 4 (a)-(d) depict the XPS spectra of the Si 2p, Al 2p, Hf 4f, and O 1s core levels [26], [27], [28]. In the Si 2p spectrum, higher binding energy and intensity of the SiO_x signal were observed for the annealed sample due to the Si oxidation during the PMA process [29]. On the other hand, the peak height of AlO_x was higher for the annealed sample, indicating that the Al-O bonds would form during the PMA process owing to the lowest Gibbs' free energy at the high-κ/SiGe interface [12]. It is worth mentioning that the XPS results of Hf 4f and O 1s did not demonstrate the apparent differences, as shown in Fig. 4 (c) and (d). Therefore, we supposed that the scavenging effect would only occur at the high-κ/SiGe interface.

B. ELECTRICAL CHARACTERISTICS OF SIGE MOSCAPS

Fig. 5 (a) depicts C–V curves of the $Si_{0.8}Ge_{0.2}$ capacitors measured at 500 kHz with low cycles (1/2/3/10-cycle) of TMA pre-treatment for IL formation to pursue thinner

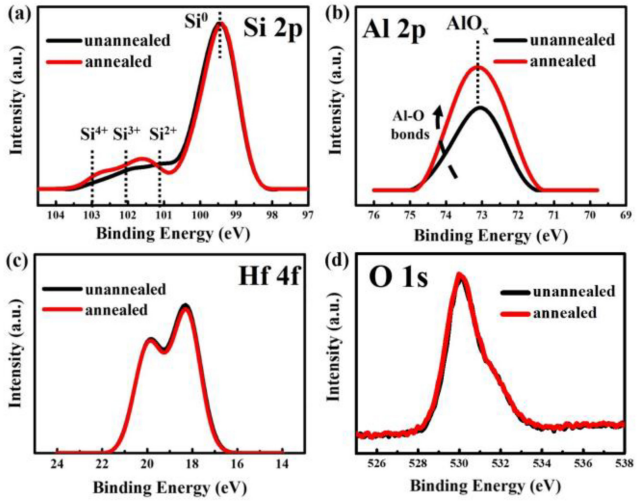

FIGURE 4. XPS spectra of the (a) Si 2p, (b) Al 2p, (c) Hf 4f, and (d) O 1s for the unannealed and annealed Al/TiN/30-cycle HfO_2/10-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ stack structures after soaking in APM.

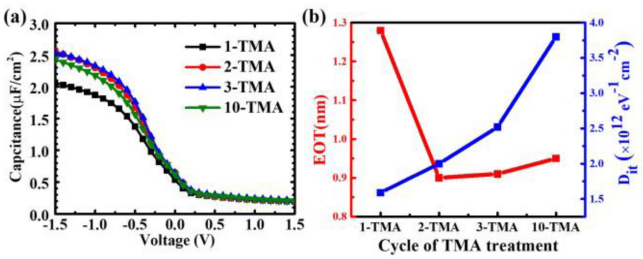

FIGURE 5. (a) 500 kHz-CV curves of the 30-cycle Al/TiN/HfO_2/TMA-IL/$Si_{0.8}Ge_{0.2}$ capacitors with various cycle numbers of TMA treatment for IL formation. (b) The extracted EOT and D_{it} values of the capacitors.

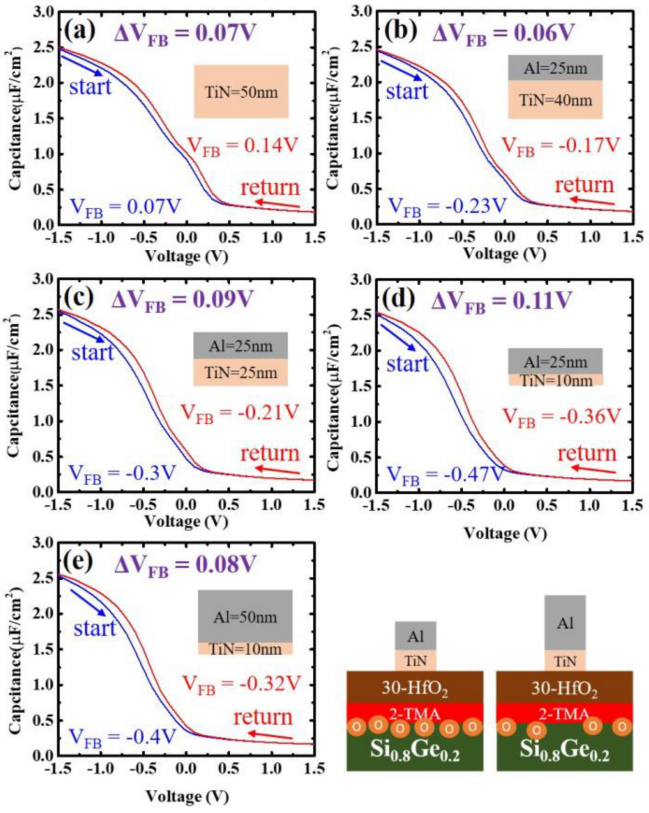

FIGURE 6. Hysteresis levels of the optimized 30-cycle HfO_2/2-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ MOS capacitors with various gate electrodes. (a) only TiN (b) Al/TiN=25/40nm (c) Al/TiN=25/25nm (d) Al/TiN=25/10nm, and (e) Al/TiN=50/10nm. The insets show the illustrative structure of the SiGe capacitor with Al/TiN=25/10nm and Al/TiN=50/10nm gate electrodes, respectively.

SiGe IL and scale down the EOT value. Note that all the capacitors were annealed, and the composite upper-metal Al/TiN of 25nm/25 nm was applied. The SiGe capacitor with 2-cycle TMA IL pre-treatment exhibited the highest accumulation capacitance (C_{acc}), i.e., an EOT value of ~0.9 nm, as presented in Fig. 5 (b). As the cycle number of TMA pre-treatment increased, the EOT value increased, which might stem from thicker SiGe IL formation (2-TMA, 3-TMA, and 10-TMA). However, when 1-cycle TMA pre-treatment was adopted, the SiGe capacitor displayed a much lower C_{acc} since we thought the IL formation reaction was incomplete since only a few Al atoms were present and the IL was prone to be mainly composed of a lower-κ dielectric, for example, resulting from Si-O and Ge-O bonds. However, this seemed beneficial to the D_{it} since the capacitor with 1-cycle TMA pre-treatment showed the lowest D_{it} value. As the cycle of TMA pre-treatment increased, the D_{it} value became larger accordingly. The underlying reason for the variation of the D_{it} performance was probably because more Ge dangling bonds were left as more Al-O bonds formed, the Al-induced increase in D_{it} [15]. Therefore, considering both EOT and D_{it} performances, 2-cycle TMA pre-treatment was thought to be the best IL pre-treatment condition.

In overview, through Al/TiN capping, the oxygen atoms in the SiGe gate stack might be gathered up through the Al scavenging effect, which resulted in the high-quality high-κ/SiGe interface; and 2-cycle TMA pre-treatment would make the low-EOT SiGe gate stack. However, it was verified that during the PMA process, the gate electrode of Al/TiN might also form the Al-O layer to block the oxygen inward diffusion and leave the oxygen vacancies unfilled, which would lead to hysteresis and reliability issues [17]. The hysteresis width could be a criterion to determine the number of the slow oxide traps and interface traps of the SiGe gate stack. When the hysteresis is large, it is likely due to the fuzzy high-κ/SiGe interface or many oxygen vacancies; meanwhile, when the hysteresis is small, it may be due to oxygen vacancies filled with numerous oxygen atoms. Too many oxygen atoms might also induce the SiGe reoxidation and deteriorate D_{it} performance [30].

Figs. 6 (a)-(e) illustrate the hysteresis widths of the capacitors subject to the scavenging effect with various gate electrode compositions. As seen in Fig. 6 (a), the capacitor with only sputtered TiN of 50nm displayed a hysteresis

TABLE 2. Extracted electrical characteristics of SiGe MOS capacitors with various gate electrodes.

Gate electrode (nm)	EOT(nm)	J_g@V_{FB}-1.5V (A/cm^2)	D_{it} (cm^{-2}eV^{-1})	D_{it}@E-E_v (eV)	V_{FB} (V)
Al/TiN=0/50	0.93	1.2×10^{-1}	5.8×10^{13}	0.3	0.07
Al/TiN=25/40	0.95	2.1×10^{-2}	2.7×10^{13}	0.32	-0.23
Al/TiN=25/25	0.91	1.1×10^{-2}	2×10^{12}	0.29	-0.3
Al/TiN=25/10	0.92	5.7×10^{-3}	1.4×10^{12}	0.29	-0.47
Al/TiN=50/10	**0.91**	$\mathbf{1.9\times10^{-3}}$	$\mathbf{9.7\times10^{11}}$	**0.28**	**-0.4**

width of 0.07 V and V_{FB} of 0.07 V in the forwarding sweep. While the Al capping metal was involved, the SiGe capacitors, in Figs. 6 (b)-(d), with the gate electrodes of Al/TiN of 25nm/40nm, 25nm/25nm, and 25nm/10nm showed larger hysteresis values, which might be owing to fewer oxygen atoms emerging at the high-κ/SiGe interface via scavenging. As the thickness of the bottom-metal TiN decreased, the hysteresis became more significant, and the V_{FB} value in the forward sweep shifted towards negative, which was thought to be related to more oxygen vacancies being generated due to a more effective scavenging process since the distance from the Al metal to the SiGe gate stack was shorter [31].

Meanwhile, Fig. 6 (e) shows the effect of increased upper-metal Al thickness (Al/TiN of 50nm/10nm) on the scavenging process. In our thoughts, the increased upper-metal Al thickness might bring about a more substantial scavenging effect making the hysteresis performance worse and generating more oxygen vacancies. Surprisingly, the smaller hysteresis width and the positive-shifted V_{FB} in the forwarding sweep were observed; this trend was opposed to those cases shown in Fig. 6 (b)-(d). Therefore, we speculated that the thicker Al capped metal of the SiGe capacitor likely prevented more oxygen atoms diffusing from ambient to the high-κ/SiGe interface, as illustrated schematically of the inset in Fig. 6; the capacitor with thinner Al capped metal perhaps allowed more oxygen atoms appeared at the high-κ/SiGe interface. Subsequently, when the PMA process was conducted, the number of generated oxygen vacancies at the high-κ/SiGe interface would originate from the number of oxygen atoms scavenged out. As a result, smaller hysteresis width and positive-shifted forward V_{FB} were attained.

In addition to the hysteresis performance results, more extracted electrical parameters of the SiGe capacitors with various gate electrodes are listed in Table 2. Comparatively low EOT values of less than 1 nm of all the SiGe capacitors were obtained with various gate electrode configurations, implying the 2-cycle TMA treatment could result in thinner IL and a smaller EOT value. Moreover, the sample with only sputtered TiN exhibited the highest D_{it} value, which meant the worst SiGe interface quality was obtained. When the Al capping was employed, the SiGe interface quality improved significantly. As the upper-metal Al thickness was fixed and the bottom-metal TiN thickness decreased, the D_{it} value became minor owing to the more superior oxygen scavenging ability.

Furthermore, different from the hysteresis tendency of the SiGe capacitors with increased Al upper-metal, that

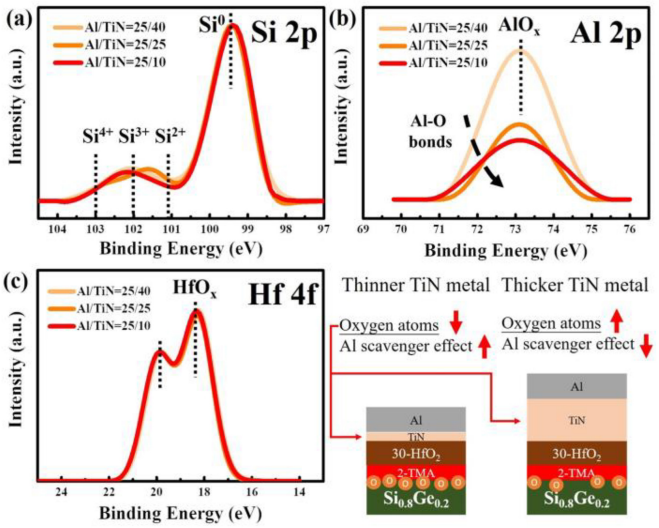

FIGURE 7. High-resolution XPS of the (a) Si 2p, (b) Al 2p, and (c) Hf 4f core-levels for the 30-cycle HfO_2/2-cycle TMA-IL /$Si_{0.8}Ge_{0.2}$ stack structures with various gate electrodes after soaking in APM (NH_4OH: H_2O_2: H_2O = 1:2:5) for 20 minutes to remove the gate electrodes.

with Al/TiN of 50nm/10nm exhibited the lowest D_{it} value, which was supposed to be the fewest oxygen content at the high-κ/SiGe interface caused by the combination of more substantial Al scavenging capability and thicker Al-O layer oxygen diffusion barrier. Therefore, fewer oxygens could lead to lessened SiGe reoxidation. Also, the D_{it} and J_G values showed the same trend among all the samples indicating the J_G might arise from the fuzzy SiGe interface, which could be cured through the oxygen-scavenging process. Furthermore, it was found that the D_{it} values and the J_G values could be improved about 60 times and 100 times around SiGe capacitors with various metal compositions, respectively, which had similar trends in our previous study [17].

Figs. 7 (a)-(c) depict the XPS spectra of Si 2p, Al 2p, and Hf 4f for the Al/TiN/HfO_2/2-cycle TMA-IL/$Si_{0.8}Ge_{0.2}$ stack structures with various gate electrodes compositions (Al/TiN of 25nm/40nm, 25nm/25nm, and 25nm/10nm) to demonstrate the effect of the scavenging on the material interaction with the entire gate stack. The XPS analyses were conducted on the samples after removing the top gate by soaking in APM, the same experimental procedure in Fig. 4. For the Si 2p spectrum, the peak positions of the samples with various top metal compositions were observed around the Si^{2+} and Si^{3+} signals with similar peak intensity. In addition, the peak positions of SiO_x were observed at random binding energies, indicating that the scavenging strength might not affect the Si oxidation at the high-κ/SiGe interface.

On the other hand, Fig. 7 (b) displays the peak heights of AlO_x binding energy of the samples; the peak height was lower when the bottom-metal TiN thickness was decreased. Therefore, we speculated that the oxygen atoms at the high-κ/SiGe interface might come from two paths. One is inward

TABLE 3. Normalized devolution results from O 1s XPS of HfO_2/ TMA-IL /SiGe stack structures with various gate electrodes.

Gate electrode (nm)	Metal-O (Hf-O & Al-O)	Oxygen Vacancy	Si-O
Binding Energy (eV)	530.7 eV	531.5 eV	532.6 eV
Al/TiN=25/40	79.8%	4.8%	15.4%
Al/TiN=25/25	77.4%	6.5%	16.1%
Al/TiN=25/10	76.3%	8.0%	15.7%

diffusion from the ambient through the PMA process, which might be greatly inhibited via Al capping. Another is the oxygen atoms accommodated inside the TiN metal, which downward diffuse through the PMA process [17]. With thinner TiN, fewer oxygen atoms are contained, and thus those oxygen atoms diffusing to the high-κ/SiGe interface and forming the Al-O bonds are correspondingly fewer. The XPS results of Al 2p spectra seemed able to explain the improvement in D_{it}, as shown in Table 2, as the TiN was thinner (Al/TiN of 25nm/40nm, 25nm/25nm, and 25nm/10 nm). Therefore, we thought that the high-quality high-κ/SiGe interface would be attributed to fewer Ge dangling bonds left because of the result arising from the formation of fewer Al-O bonds [15]. Besides, Fig. 7 (c) illustrates the XPS results of Hf 4f core levels, disclosing that the HfO_2 would not be influenced by the Al scavenging process during the PMA process. The finding of the XPS result clarified that the Al scavenging effect only affected the high-κ/SiGe interface but not the high-κ HfO_2 dielectric.

Furthermore, the normalized XPS devolution results of O 1s spectra are shown in Table 3. By looking into the difference in oxygen configuration, the scavenging strengths with different electrode structures could be clearly revealed. We found that the proportions of metal-oxygen, including Hf-O and Al-O bonds, located at 530.7 eV and 530.4 eV, were the least when the thinnest bottom-metal TiN thickness was applied (Al/TiN of 25nm/10nm), implying that the fewer Al-O bonds were formed [32], [33]. The XPS results also showed that the proportion of oxygen vacancies was increased with decreasing the bottom-metal TiN thickness [34], [35], which echoed the hysteresis width trend observed in Figs. 6 (b)-(d).

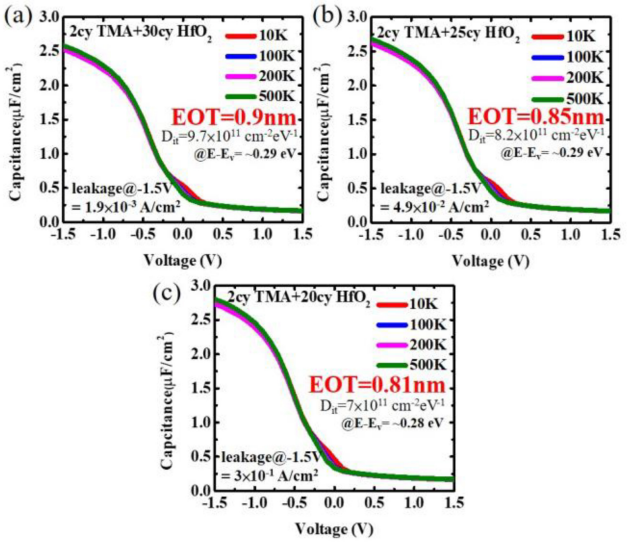

FIGURE 8. Multi-frequency C–V characterization of the $Si_{0.8}Ge_{0.2}$ capacitors with (a) 2-cycle TMA-IL + 30-cycle *HfO_2* (b) 2-cycle TMA-IL + 25-cycle HfO_2, and (c) 2-cycle TMA-IL + 20-cycle HfO_2. The metal composition of Al/TiN=50/10 were applied for all SiGe capacitors.

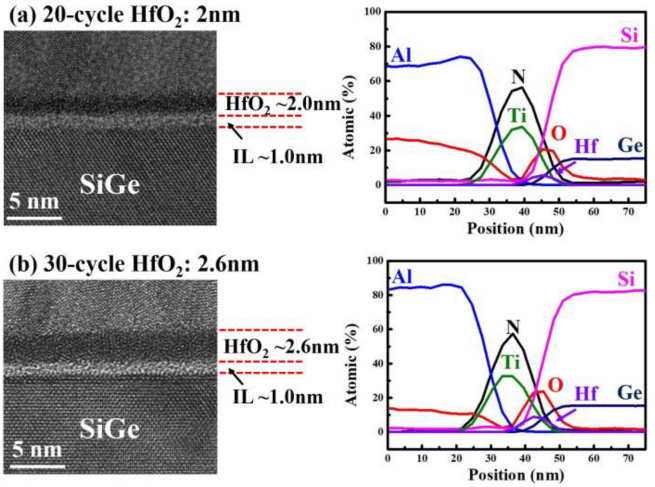

FIGURE 9. HRTEM images and EDX depth profiles of SiGe capacitors with (a) 2-cycle TMA-IL + 20-cycle HfO_2 and (b) 2-cycle TMA-IL + 30-cycle HfO_2.

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Fig. 8 depicts multi-frequency C–V characteristics of the $Si_{0.8}Ge_{0.2}$ capacitors with different HfO_2 (20-cycle, 25-cycle, and 30-cycle) thicknesses to demonstrate the feasibility of EOT scaling through TMA pre-treatment and Al capping. The optimized gate electrode of the Al/TiN of 50nm/10nm was applied for three SiGe capacitors with different HfO_2 thicknesses. We found the SiGe capacitors with thinner HfO_2 dielectric displayed relatively small humps at the depletion region and exhibited the low D_{it} value of 7×10^{11} $cm^{-2}eV^{-1}$, which might be due to the more substantial Al scavenger metal effect [36]. In addition, all the energy levels of minimum D_{it} values of fabricated SiGe capacitors were near E-E_v ~0.29 eV. By tuning down HfO_2 thickness, a pretty impressive EOT value of 0.81nm was achieved with the increase in J_G, resulting from the higher probability of direct tunneling [37].

Figs. 9 (a) and (b) present cross-sectional HRTEM images and Energy Dispersive X-ray Spectrometry (EDX) depth profiles of the SiGe gate stack with 20-cycle and 30-cycle HfO_2 depositions, respectively. We observed that the IL thickness of approximately 1.0 nm was formed for both gate stacks through 2-cycle TMA treatment. In addition, the thicknesses of the 20-cycle and 30-cycle HfO_2 depositions were 2 and 2.6 nm, respectively. Accordingly, the calculated dielectric constant of the TMA-treated IL and HfO_2 would be 8 and 23, respectively, meaning the EOT value could be improved

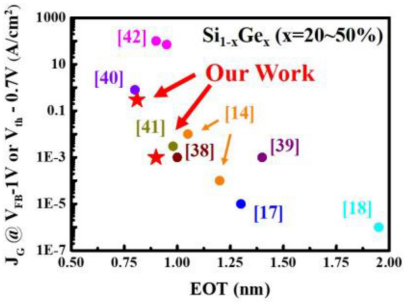

FIGURE 10. Benchmark of J_G as a function of EOT for $Si_{1-x}Ge_x$ devices.

through the dielectric constant of IL improvement by TMA pre-treatment.

Finally, Fig. 10 summarizes the benchmark of J_G at $V_{FB}-1V$ or $V_{th}-0.7V$ versus EOT for the Si-cap-free high-κ/SiGe stacks with Ge contents of SiGe from 20% to 50%. Among the high-κ/SiGe gate stacks with various Ge contents of SiGe reported [38], [39], [40], [41], [42], our advanced SiGe gate stacks composed of TMA pre-treatment and Al capping offered excellent EOT performance and relatively lower gate leakage current. The EOT of 0.81nm and 0.9nm with lower gate leakage currents were obtained by the HfO_2 thickness reduction.

IV. CONCLUSION

This study reported the Al scavenger effect on the HfO_2-based gate dielectric on the $Si_{0.8}Ge_{0.2}$ substrates with IL TMA pre-treatment. The aggressive EOT value of 0.81nm was obtained through the 20-cycle high-κ HfO_2 deposition. The D_{it} and J_G values could be improved about 60 times and 100 times by tuning the gate electrode composition without degrading the EOT performance. The XPS results revealed that the D_{it} improvement during the various gate electrodes applied might be owing to the Al metal scavenger and the minimization of the oxygen atoms' diffusing to the high-κ/SiGe IL during the PMA process. Moreover, the high-κ HfO_2 dielectric might not be affected via the oxygen scavenging process. Besides, the hysteresis levels of SiGe capacitors were also tested to optimize the metal composition of Al/TiN, which XPS results could verify. This study thoroughly examined the SiGe capacitor with TMA pre-treatment and Al metal-capped. As a result, a simple gate stack structure of high-performance SiGe devices could be obtained by optimizing TMA pre-treatment and gate engineering.

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