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High-Performance P-Type Germanium Tri-Gate FETs via Green Nanosecond Laser Crystallization and Counter Doping for Monolithic 3-D ICs

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ABSTRACT This paper proposed a fabrication of p-type Germanium (Ge) tri-gate field-effect transistors (Tri-gate FETs) via green nanosecond laser crystallization (GNSLC) and counter doping (CD). By using the GNSLC, the nano-crystalline-Ge (nc-Ge) with a grain size of 80 nm could be turned into polycrystalline Ge (poly-Ge) with that of above 1 μm. With the increase of laser power, the improved crystallinity and lower hole concentration of poly-Ge were also verified by Raman spectra and Hall measurement. To fabricate the high-performance Ge Tri-gate FETs, the chemical-mechanical planarization (CMP) and counter doping (CD) process would further be utilized. The CMP process eliminated the surface roughness of poly-Ge while the CD process decreased the hole concentration of poly-Ge or even converted that into an N-type one. The effect of the CD on the performance of p-type Ge Tri-gate FETs was further investigated. Consequently, the GNSLC Ge Tri-gate FETs showed threshold voltage (V_{th}) of -0.41 V, I_{ON} of 7.10×10^{-6}, and I_{OFF} of 1.28×10^{-9} respectively, indicating better crystallinity of the Ge channel.

INDEX TERMS Monolithic 3D integration, polycrystalline Ge (poly-Ge), tri-gate field-effect transistors (Tri-gate FETs), green nanosecond laser crystallization (GNSLC), counter doping (CD).

I. INTRODUCTION

Nowadays, the scaling of silicon complementary metal-oxide-semiconductor (CMOS) devices is reaching its physical limits. The interconnect delay and contact resistance severely degrade the performance of the integration circuits [1]. Therefore, three-dimensional integration circuits (3D ICs) and novel high-mobility channel materials have become more and more popular for future semiconductors and circuit architecture [2], [3]. Germanium (Ge) featuring higher mobility than Si and high compatibility with Si-based processes has attracted lots of interest for the next-generation channel material of nano-devices [4], [5]. Moreover, the temperature of Ge-based devices fabrication is typically lower than the Si ones. Hence the Ge-based devices were widely considered to be more suitable for monolithic 3D ICs [6], [7], which could provide a more convincing method for realizing monolithic 3D ICs by taking advantage of Ge-on-insulator (GeOI) transistors as the top-layer devices.

Published studies have purposed the fabrication of high-quality Ge as the GeOI devices for future ICs, such as solid-phase crystallization (SPC) [8], metal-induced crystallization (MIC) [9], lateral liquid-phase crystallization (LLPE) [10], [11], layer transfer technique [12], and laser crystallization (LC) [13], [14], [15]. Unfortunately, both SPC and MIC required long-time annealing, and the quality of crystallized Ge films was thought to be relatively poor; LLPE could attain high-quality Ge films, whereas its process temperature of nearly 1000 °C to melt the Ge was unfavorable for the monolithic 3D integration; the layer transfer technique suffered complicated fabrication process.

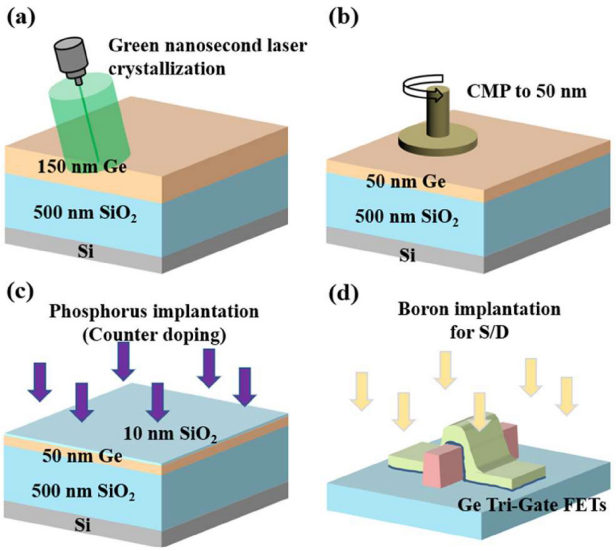

FIGURE 1. Schematics of the critical process of p-type GNSLC Ge Tri-gate FETs fabrication. (a) The as-deposited nc-Ge is crystallized by the green nanosecond laser. (b) The CMP process thinned the thickness and modified the morphology of GNSLC poly-Ge. (c) The poly-Ge with cap SiO_2 layer was subjected to the CD process. (d) The S/D regime doping of Ge Tri-gate FETs.

Among the techniques mentioned above, LC, especially short pulse laser, possessed the advantages of an extremely low thermal budget, a simple fabrication process, and relatively high-quality crystallized-Ge films. Consequently, these LC techniques were regarded as more adaptable to the application of 3D ICs. In addition, for the crystallized Ge, there would be a large amount of hole concentration regenerated from the defect in the Ge films [16]. Counter doping (CD) technique is one of the simplest methods to suppress this phenomenon [17], [18]. However, there were few studies discussing the effect of LC and CD techniques on the Ge Tri-gate FETs with narrower channel widths for future application in monolithic 3D ICs.

In this work, we utilized GNSLC to recrystallize the nc-Ge films, and the crystallinity and surface morphology were first verified by a materials analyzer. Subsequently, to fabricate the high-performance Ge Tri-gate FETs, the chemical-mechanical planarization (CMP) and CD process were also employed. Finally, these finished laser-crystallized Ge Tri-gate FETs were characterized and the effect of the CD technique on the Ge Tri-gate FETs' performance was further discussed.

II. PROCESS FLOW

The whole schematic process flow for the p-type Ge Tri-gate FETs via GNSLC and CD techniques was illustrated in Fig. 1. First, a 150-nm-thick nano-crystalline-Ge (nc-Ge) film was deposited on a Si wafer with a 500-nm-thick oxide by the plasma enhanced chemical vapor deposition (PECVD) at 375°C. Subsequently, the green nanosecond laser (wavelength of 532 nm) was performed to crystallize the nc-Ge into polycrystalline Ge (poly-Ge) at room temperature in the air ambiance as shown in Fig. 1(a). The Gaussian-energy-distribution laser beam with a size of 2190.6 μm on the long axis and 42.2 μm on the short axis and a 30-ns pulse duration was used to scan the nc-Ge films along the short axis. The power of the green nanosecond laser was varied from 3 W to 4.5 W and the scanning speed was 20 mm/sec with an each-shot overlap ratio of 97.6%. After the GNSLC process, the CMP process was employed to eliminate the surface roughness and thin down the poly-Ge to about 50 nm thick, as shown in Fig. 1(b). The samples next underwent the post-CMP clean (NH_3:H_2O=40:48) to remove the slurry and the particles. Afterward, as shown in Fig. 1(c), the flattened poly-Ge was capped by a 10-nm-thick oxide and was subjected to the CD process, phosphorus implantation with a dose of 1×10^{13}, 5×10^{13}, or 1×10^{14} cm^{-2} at an energy of 17 keV. These counter dopants were then activated at 500°C for 2 hrs in an N_2 ambiance. After the CD process, the 10-nm-thick oxide was removed by a diluted buffered oxide etch (BOE) solution (1:50), and the active region including the Ge channels was defined by the e-beam lithography and reactive ion etching. Then, after the pre-gate clean, a GeO_x passivation by rapid thermal oxidation (RTO) at 400°C for 30 sec, a 5-nm-thick AlO_x by plasma-enhanced atomic layer deposition and multi-layer metals of Ti(5 nm)/TaN(100 nm)/TiN(400 nm) by physical vapor deposition were executed to form the high-k/metal gate stacks. Next, the gate structure was fabricated by e-beam lithography and reactive ion etching. Subsequently, the S/D regions were defined by the boron implantation with a dose of 2×10^{15} cm^{-2} at an energy of 10 keV and were activated by rapid thermal annealing at 400 °C for 60 sec in N_2 ambiance, as displayed in Fig. 1(d). Finally, the standard passivation and metallization process was implemented to complete the fabrication of the counter-doping p-type Ge Tri-gate FETs.

III. RESULT AND DISCUSSION

Fig. 2 exhibits the top-view scanning electron microscopy (SEM) image of the nc-Ge and poly-Ge films after GNSLC at various laser powers. All of these samples were subjected to secco-etching to reveal the grain boundary of the Ge films. As indicated in Fig. 2(a), the average grain size of the as-deposited nc-Ge film was observed to be about 80 nm owing to these nc-Ge films deposited by PECVD (375 °C). After the nc-Ge was crystallized by the GNSLC, the grain size of Ge films became larger. As the laser power increased, the grain size of poly-Ge was gradually enlarged, as shown in Fig. 2(b) and (c). When the laser power reached 4 W, as displayed in Fig. 2(d), the significant grain growth of poly-Ge to above 1 μm was observed. Then, as the laser power further raised to 4.5 W, severe Ge agglomeration occurred and resulted in the formation of large holes in the poly-Ge film, as displayed in Fig. 2(e).

Accordingly, the crystallization behavior could be categorized into three regimes: partial-melting regime below 3.5 W, super-lateral-growth (SLG) regime at around 4 W, and Ge-agglomeration regime above 4.5 W. For the partial-melting

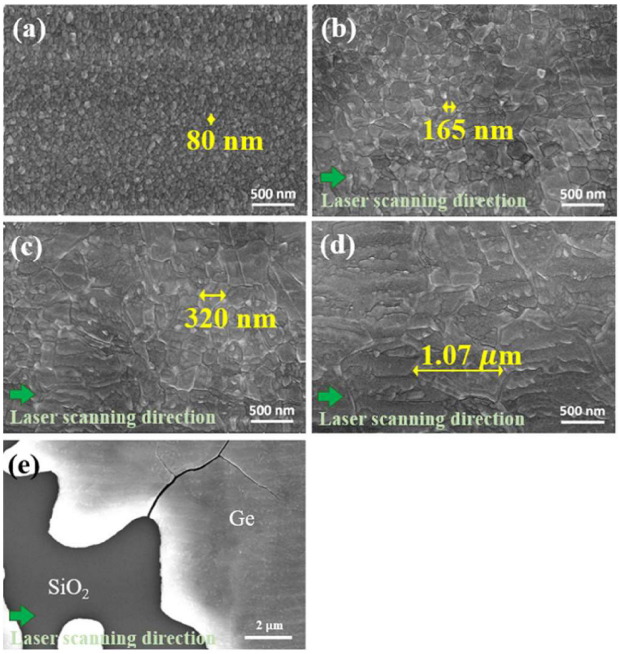

FIGURE 2. Top-view SEM images of secco-etched (a) as-deposited nc-Ge films and poly-Ge films via GNSLC of (b) 3 W, (c) 3.5 W, (d) 4 W, and (e) 4.5 W.

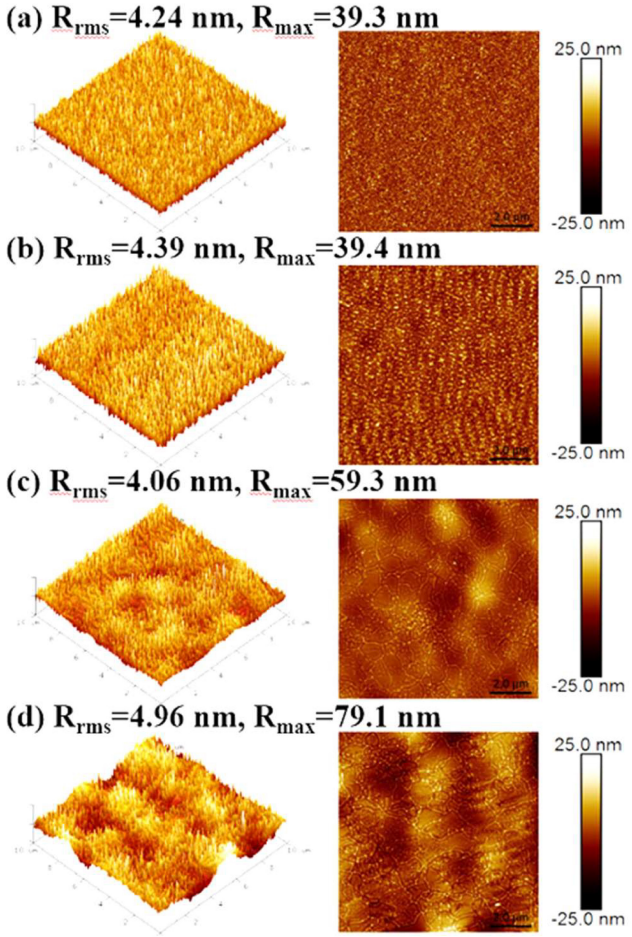

FIGURE 3. AFM images of (a) as-deposited nc-Ge film and poly-Ge film via GNSLC of (b) 3 W, (c) 4 W, and (d) 4.5 W laser powers.

regime, the average grain radius was approximately equal to the Ge films. It could be inferred that the Ge film was partially melted by the low laser power and the deep Ge was still non-melted. While the laser was off and the temperature began to drop, this non-melted Ge would act as seeds and rapidly cool down the melted Ge resulting in small grain [19]. For the SLG regime, the higher laser power near-completely melted the Ge film and remained a few discontinuous Ge solids as seeds. Hence, as the Ge film cooled down, the lateral growth from these solid seeds took place before the impingement of the grains occurred and the significant large-grained poly-Ge film could be finally obtained [19]. For further increased laser power, the Ge-agglomeration regime occurred. The severe Ge agglomeration could be attributed to the high interfacial energy between the Ge and SiO_2 underlayer induced by the excessively high laser power [20].

The lumpy surface of poly-Ge after GNSLC could be also aware in the SEM image above. Therefore, the surface morphologies of laser-crystallized poly-Ge were further investigated by atomic force microscopy (AFM), as displayed in Fig. 3. The root-mean-square roughness (R_{rms}) and maximum roughness (R_{Max}) of the as-deposited nc-Ge was about 4.24 nm and 39.3 nm, respectively. After the GNSLC, it could be observed that the R_{Max} of poly-Ge films increased with the higher laser power. This increased R_{Max} might be due to the increased interfacial energies between the molten Ge films and oxide underlayer as the laser power raising [21]. However, the R_{rms} of poly-Ge films evidently dropped to 4.06 nm at a laser power of 4W. From the top view of AFM in Fig. 3, it could be noted that the protrusions were mainly situated on the grain boundary of the poly-Ge films. The formation of these protrusions might be originated from the collision between lateral-grown grains while the smooth morphology inside a grain could be observed. Therefore, for the poly-Ge films at 4 W with a grain size (smooth morphology) of about 1 μm, as shown in Fig. 3(c), the lower R_{rms} could be obtained despite its large R_{Max} of 59.3 nm. These protrusions on the grain boundary of poly-Ge at 4W also demonstrated the occurrence of SLG [22].

The crystallinity of single-crystalline Ge wafer, nc-Ge, and GNSLC poly-Ge films was also clarified by the Raman spectra, as exhibited in Fig. 4. The full width at half maximum (FWHM) values and the peak position were also extracted, and shown in the inset table. The FWHM and peak position of a single crystalline Ge as reference was measured to be 4.3 cm^{-1} and 300.5 cm^{-1} respectively. First, the nc-Ge exhibited an FWHM of 6.2 cm^{-1} and peaked at a value of 299.4 cm^{-1}. This larger FWHM of nc-Ge than the single-crystalline Ge revealed poorer crystallinity. After the GNSLC, the poly-Ge possessed the lower FWHM. The fact implied the improved crystallinity due to the laser crystallization, which was also consistent with the results of SEM images in Fig. 2. In addition, the peaks of poly-Ge were red-shifted, indicating the larger tensile strain existing in the

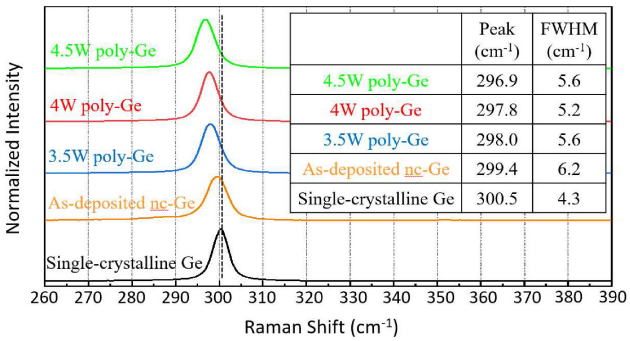

FIGURE 4. Raman spectra of single-crystalline Ge for reference, as-deposited nc-Ge, poly-Ge via various GNSLC.

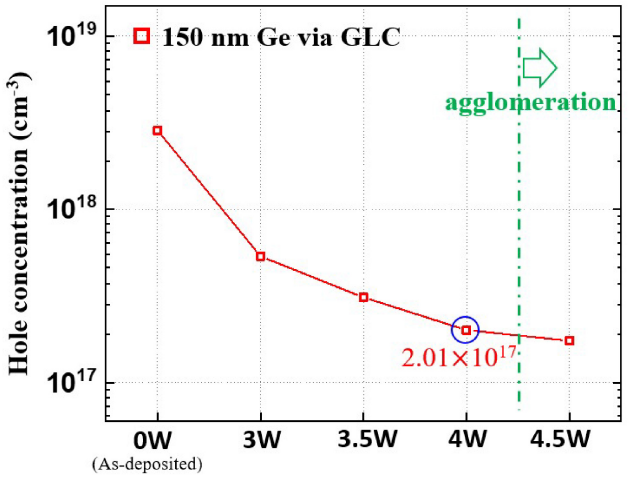

FIGURE 5. Dependence of carrier concentration of poly-Ge films on green nanosecond laser power.

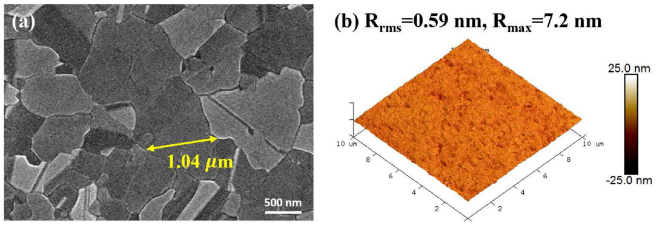

FIGURE 6. (a) Top-view SEM image (secco-etched) and (b) AFM image of poly-Ge films via GNSLC of 4 W after the CMP thinning to about 50 nm.

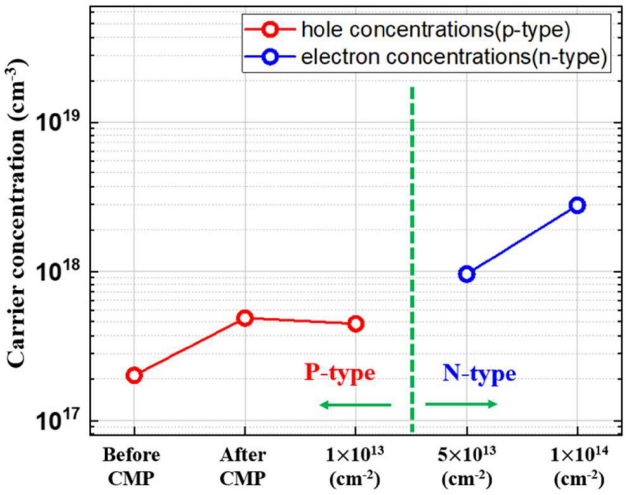

FIGURE 7. Carrier concentration of poly-Ge films (4W GNCLC) before CMP, after CMP, and after CMP and CD at doses of 1×10^{13}, 5×10^{13}, and 1×10^{14} cm^{-2}.

poly-Ge films. The results could be ascribed to the difference in the thermal expansion coefficient between the Ge films and the underlying SiO_2 during the Ge crystallization period [23]. Accordingly, the lowest FWHM, namely the superior crystallinity, was attained for the poly-Ge via GNSLC at 4 W. On the other hand, the poly-Ge of higher laser power at 4.5 W contrarily showed higher FWHM than that at 4W. The cause could be implied to be the severe agglomeration causing cracks and defects in the poly-Ge films as displayed in Fig. 2 (e).

Fig. 5 displayed the extracted hole concentration of the nc-Ge and poly-Ge at various laser powers by the Hall measurement. The hole concentration of the nc-Ge was 2.85×10^{18} cm^{-3}. After the laser crystallization, the hole concentration of the poly-Ge was observed to be significantly decreased. As the laser power reaching to 4 W, the hole concentration of that was lowered to 2.01×10^{17} cm^{-3}. The high hole concentration would originate from the acceptor-like defect in the Ge films [24]. Therefore, the lower hole concentration of the poly-Ge after the GNSLC implied improved crystallinity, which was also consistent with the results of SEM images and Raman spectra above.

According to the material analysis above, the poly-Ge via 4 W laser power possessing superior crystallinity and relatively low hole concentration was chosen to be the channel for further fabricating the p-type Ge Tri-gate FETs. However, the rough surface would degrade the device's performance [25]. Fig. 6(a) showed the secco-etched SEM image of the poly-Ge film after CMP. The thickness was reduced from 150nm to about 50 nm and the grain size almost remained the same. This further demonstrated the occurrence of SLG, concordant with the mechanisms mentioned above. Furthermore, after the CMP process, the sharply decreased R_{rms} and R_{Max} from 4.06 nm and 59.3 nm to 0.59 nm and 7.2 nm were also observed respectively. The flat surface would suppress the surface scattering of fabricated poly-Ge tri-gate FETs and thereby improve their performance.

Fig. 7 exhibited the extracted hole concentrations of the poly-Ge films via 4 W GNSLC before and after CD at doses of 1×10^{13}, 5×10^{13}, and 1×10^{14} cm^{-2}. All of the counter-doped samples were annealed at 500 °C for 2 hrs in N_2 ambiance to activate the dopants. Even though the grain size of poly-Ge after CMP was observed to remain the same, the extracted hole concentration increased from 2.01×10^{17} cm^{-3} to 4.86×10^{17} cm^{-3}. This might be inferred from the mechanical damage during the CMP thinning process [26]. After the CD at the dose of 1×10^{13} cm^{-2}, the

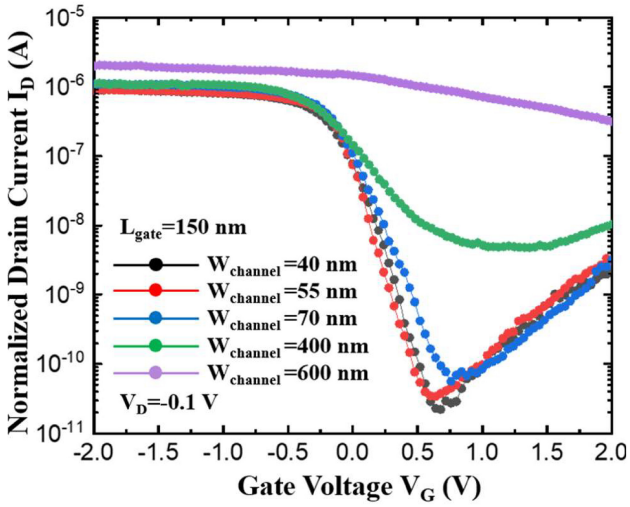

FIGURE 8. Transfer characteristics at V_D=−0.1 V of p-type Ge FETs with a gate length of 150 nm and different channel widths of 600, 400, 70, 55, and 40 nm.

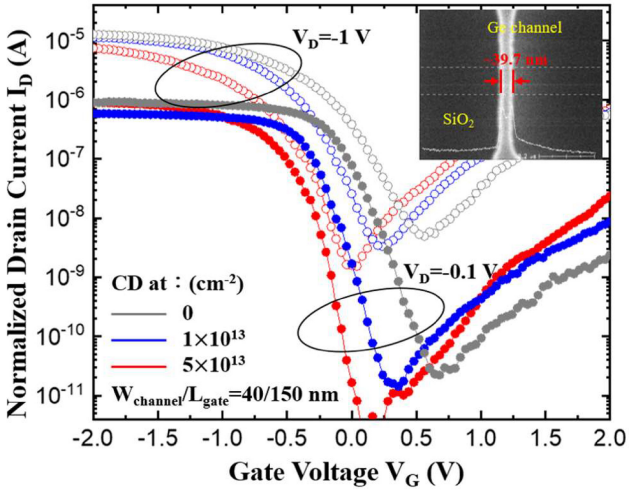

FIGURE 9. Transfer characteristics at V_D=−0.1 and −1 V of p-type Ge Tri-gate FETs with $W_{channel}/L_{gate}$=40/150 nm subjected to different CD at doses of 0, 1×10^{13}, 5×10^{13} and 1×10^{14} cm^{-2}.

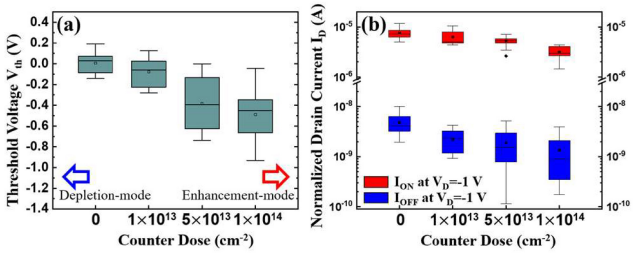

FIGURE 10. Dependence of (a) V_{th} and (b) I_{ON}/I_{OFF} at V_D=−1 V on the different CD at doses of 0, 1×10^{13}, 5×10^{13}, and 1×10^{14} cm^{-2}.

hole concentration of poly-Ge after CMP slightly decreased to 4.46×10^{17} cm^{-3}. As the counter dose were raised to 5×10^{13} and 1×10^{14} cm^{-2}, the poly-Ge films were successfully converted from p-type films into n-type ones and the electron concentrations respectively were 9.60×10^{17} and 2.78×10^{18} cm^{-3} identified by the Hall measurement. This fact meant that the innate hole concentration of poly-Ge films had been recombined with the counter dopants.

The transfer characteristics at V_D=−0.1 V of p-type Ge FETs with a gate length (L_{gate}) of 150 nm and different channel widths ($W_{channel}$) were displayed in Fig. 8. All of the p-type Ge FETs shown here were fabricated without the CD process. The Ge FETs with a channel width of both 600 nm and 400 nm exhibited a low on-off current ratio (I_{ON}/I_{OFF}) smaller than 10^2 at V_D=−0.1 V. As the channel width decreased, the extracted I_{ON}/I_{OFF} and subthreshold swing (S.S.) of the Ge FETs were obviously improved. While the channel widths were shrunk to 55 and 40 nm, the Ge Tri-gate FETs exhibited higher I_{ON}/I_{OFF} above 2×10^4 at V_D=−0.1 V and better S.S. of about 145 mV/dec. This strongly width-related performance was somewhat similar to the behavior of junctionless FETs [27]. By shrinking the channel width of p-type Ge FETs, the enhanced gate controllability and the fully-depleted channel could be achieved and its I_{ON}/I_{OFF} and S.S. were thereby improved.

Afterward, we utilized the CD process and attempted to further improve the performance of the p-type Ge Tri-gate FETs. Fig. 9 exhibited the transfer characteristics of the p-type Ge Tri-gate FETs with $W_{channel}/L_{gate}$=40/150 nm subjected to different counter doses of 0, 1×10^{13}, or 5×10^{13} cm^{-2}. From the curves, the threshold voltage (V_{th}) was extracted by the transconductance maximum method at V_D=−0.1 V, the I_{ON} (@V_g=V_{th}−1V) and I_{OFF} (@minimum I_D) were obtained at V_D=−1 V, and the S.S. were extracted at V_D=−0.1 V. For the p-type Ge Tri-gate FETs without CD process, it possessed V_{th} of 0.02 V, I_{ON} of 7.60×10^{-6}, I_{OFF} of 4.95×10^{-9}, and S.S. of 149 mV/dec., showing the normally-on characteristic (@Vg=0V). At a counter dose of 1×10^{13} cm^{-2}, the p-type Ge Tri-gate FETs showed V_{th} of −0.22 V, I_{ON} of 8.04×10^{-6}, I_{OFF} of 3.27×10^{-9}, and S.S. of 131 mV/dec. As the counter dose further raised to 5×10^{13} cm^{-2}, the V_{th} of −0.41 V, I_{ON} of 7.10×10^{-6}, I_{OFF} of 1.28×10^{-9}, and S.S. of 118 mV/dec. would be achieved, and these p-type Ge Tri-gate FETs with normally-off characteristics could be operated as an enhancement-mode device.

To further verify the effect of the CD process, the dependence of the p-type Ge Tri-gate FET electrical properties on different counter doses was plotted in Fig. 10. With the increase of counter dose, the negative shift of V_{th}, which gradually decreased I_{ON} and I_{OFF}, could be observed, especially the I_{OFF}. The lower I_{OFF} might be attributed to the Ge channel with lower hole concentration and even converted into n-type at the counter dose above 5×10^{13} cm^{-2}, consistent with the results of Hall measurement in Fig. 7. This converted n-type Ge channel would turn the Ge Tri-gate FETs into a normally-off device owing to the p-type source and drain (S/D). The PN junction between S/D and

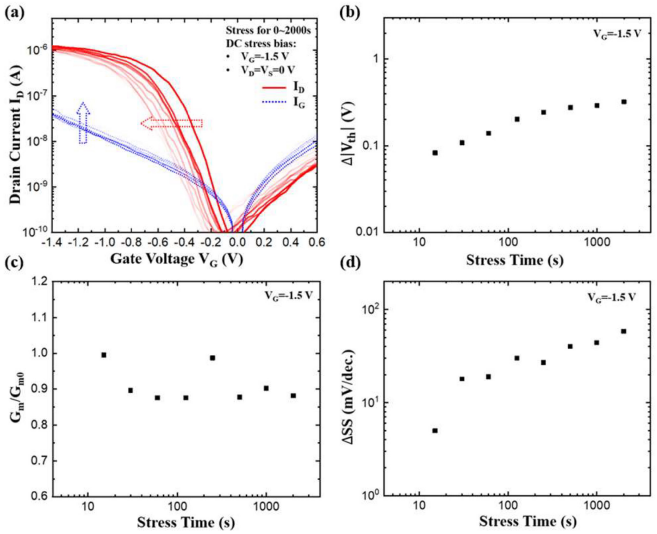

FIGURE 11. **(a) Transfer characteristics of Ge tri-gate FETs via GNSLC of 4 W with CD of 5×10^{13} cm^{-2} at V_D=−0.1V under different stress times. (b) $|\Delta V_{th}|$, (c) G_m/G_{m0}, and (d) ΔSS as a function of different stress times.**

TABLE 1. **Comparison of different fabrication of P-type Ge tri-gate FETs.**

	This work		Ref [31]		Ref [32]		Ref [33]	Ref [34]
Crystallization Method	GNS Laser Crystallization		Excimer Laser Crystallization		Solid Phase Crystallization		Liquid-Phase-Epitaxy	Single-Crystal Ge by Epitaxy
Width/Length	40/150 nm		0.5/0.5 μm		40 nm/ 10 μm	10 nm/ 10 μm	130 nm/ 4.5μm	40 nm/ 110 nm
Equivalent oxide thickness	~3.67 nm		50 nm		1.75 nm		20 nm	~0.8 nm
Counter Doping	w/o	w/	w/o	w/	w/o		w/	w/o
I_{ON}/I_{OFF} at V_D=-1V	1.5×10^3	5.6×10^3	7.7	1.7×10^3	<10	$>10^3$	~10^3	$>10^4$ @V_D=-0.5V
Subthreshold Swing (mV/dec.)	149	118	--	~700	--	~140	750	100

the channel acted as a barrier to suppress the leakage current at off-state. In addition, the lower I_{ON} of p-type Ge Tri-gate FETs at a higher counter dose might be ascribed to the increased concentration of counter dopants, which were considered as scattering centers in the Ge channel. Therefore, compared with the p-type Ge Tri-gate FETs at the counter dose of 5×10^{13} cm^{-2}, those at 1×10^{14} cm^{-2} showed obviously lower I_{ON}. Fig. 11 showed the negative bias instability (NBI) of Ge tri-gate FET via GNSLC of 4 W with CD of 5×10^{13} cm^{-2}. There were several studies reporting that the Ge pMOS FinFET NBTI response varies less with temperature (corresponding to smaller activation energy) than that of Si pMOS FinFETs [28], [29]. The Ge Tri-gate FET was subjected to different stress durations up to 3840 s at room temperature under gate biases V_g=−1.5V. After the stress for the 2000s, the Ge tri-gate FET possesses the negative V_{th} shift of about −0.3V, G_m/G_{m0} of about 0.9, and shift in SS of about 58 mV/dec. This NBI phenomenon could be ascribed to the scattering of channel carriers due to interface-trap generation [29], [30]. This implied the interface of Ge/GeO_x/AlO_x stacking should be further improved.

Table 1 displayed the comparison of p-type Ge tri-gate FETs via different crystallization methods. Thanks to the high-quality Ge films by GNSLC, the narrower width of tri-gate FET, and the CD process, the Ge tri-gate FET possessed comparable I_{ON}/I_{OFF} and S.S. to the single-crystal Ge one by epitaxy. In summary, the enhancement-mode p-type Ge Tri-gate FETs via GNSLC of 4 W at a counter dose of around 5×10^{13} cm^{-3} with fewer scattering centers would be appropriate for future applications.

IV. CONCLUSION

The high-performance p-type Ge Tri-gate FETs had been successfully fabricated via GNSLC and CD process. The crystallinity of poly-Ge films via different laser power was verified by material analysis, including SEM, AFM, RAMAN spectra, and Hall measurement. From these results, poly-Ge via 4 W laser power showed better grain size (> 1 μm) and a lower hole concentration of 2.01×10^{17} cm^{-3}. The rough poly-Ge surface was also eliminated by the CMP process, and it possessed a slighter surface roughness of 0.59 nm in R_{rms} and 7.2 nm in R_{Max}. Furthermore, the CD process was utilized to suppress the hole concentration of the recrystallized poly-Ge films. The p-type poly-Ge Tri-gate FETs with a counter dose of 5×10^{13} cm^{-3} displayed a V_{th} of −0.41 V, I_{ON}/I_{OFF} of $7.10\times10^{-6}/1.28\times10^{-9}$, and normally-off characteristic, which would be appropriate for the p-type Ge Tri-gate FETs in the monolithic 3D ICs.

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