Received 11 February 2023; revised 22 March 2023 and 7 April 2023; accepted 22 April 2023. Date of publication 25 April 2023;
date of current version 3 May 2023. The review of this article was arranged by Editor C.-M. Zetterling.

*Digital Object Identifier 10.1109/JEDS.2023.3270273*

# Investigations on Wide-Gap $Al_{0.21}Ga_{0.79}N$ Channel MOS-HFETs With $In_{0.12}Al_{0.76}Ga_{0.12}N$ Barrier/Buffer and Drain Field-Plate

**CHING-SUNG LEE [1], CHIH-TSUNG CHENG [1], JIAN-HONG KE [2], AND WEI-CHOU HSU [2]**

1 Department of Electronic Engineering, Feng Chia University, Taichung 40857, Taiwan
2 Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan 70101, Taiwan

CORRESPONDING AUTHOR: C.-S. LEE (e-mail: cslee@fcu.edu.tw)

This work was supported by the Ministry of Science and Technology under Contract MOST 111-2221-E-035-071-MY3 and Contract 108-2221-E-035-038-MY3.

**ABSTRACT** This work investigates, for the first time, wide-gap $Al_{0.21}Ga_{0.79}N$ channel metal-oxide-semiconductor heterostructure field-effect transistors (MOS-HFETs) with $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier/buffer and drain field-plate (DFP) designs. High-k and wide-gap $Al_2O_3$ was grown as the gate oxide and surface passivation by using non-vacuum ultrasonic spray pyrolysis deposition (USPD) technique. A control device having the same epitaxial layers, except with $In_{0.12}Al_{0.88}N$ barrier/buffer was studied in comparison. Enhanced spontaneous polarization effect, improved interfacial quality, and enhanced carrier confinement have been achieved by using the $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier/buffer design, which has successfully resulted in improved carrier transport, increased electron concentration, and high current densities. The present $In_{0.12}Al_{0.76}Ga_{0.12}N/AlN/Al_{0.21}Ga_{0.79}N$ MOS-HFET design with (without) DFP design has demonstrated superior maximum drain-source current density ($I_{DS,max}$) of >1 (>1) A/mm at $V_{DS}$ = 20 V, high saturated drain-source current density at $V_{GS}$ = 0 V ($I_{DSS0}$) of 791.1 (755) mA/mm, and low specific on-resistance ($R_{on,sp}$) of 2.83 (2.81) mΩ/cm$^2$. High device figure-of-merit (FOM) on $BV_{DS}^2/R_{on,sp}$ of 93.7 (75.4) MW/cm$^2$ was also obtained with the three-terminal on-state drain-source breakdown voltage ($BV_{DS}$) of 515 (460) V. The present design is promisingly advantageous to high-current and high-voltage power-switching circuit applications.

**INDEX TERMS** Wide-gap AlGaN channel, InAlGaN barrier, MOS-HFET, $Al_2O_3$, non-vacuum ultrasonic spray pyrolysis deposition, drain field-plate.

## I. INTRODUCTION

With the increasing demands of high-voltage power- switching devices for applications of DC-DC converters [1], [2], data centers [3], vehicle electronics [4], and renewable energy [5], heterostructure field-effect transistors (HFETs) with wide-gap channel have been explored [6], [7], [8], [9]. As compared to GaN-based devices, the wide-gap AlGaN compounds possessing high Johnson's figure-of-merit (JFOM) [10] and high Baliga's figure-of-merit (BFOM) [11] are suitable channel recipes to enhance the high-voltage operation. In order to improve battery charging efficiency for electric vehicles [12] and enhance power performance for wireless communication [13], [14] applications, devices with high current drive capability are needed. Our previous works have studied Si-doped AlGaN channel MOS-HFETs [15], [16] showing depletion-mode operation and $F^-$-implanted AlGaN barrier MOS-HFET [17] exhibiting enhancement-mode characteristics. This work presents, for the first time, wide-gap $Al_{0.21}Ga_{0.79}N$ channel MOS-HFETs with designs of $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier/buffer and drain field-plate (DFP). A control $In_{0.12}Al_{0.88}N/AlN/ Al_{0.21}Ga_{0.79}N$ device was fabricated and characterized in comparison. It is known that InAlN/GaN heterostructure possesses lattice match and enhanced spontaneous polarization effects [18], [19] as compared to AlGaN/GaN heterostructure. Yet, the carrier

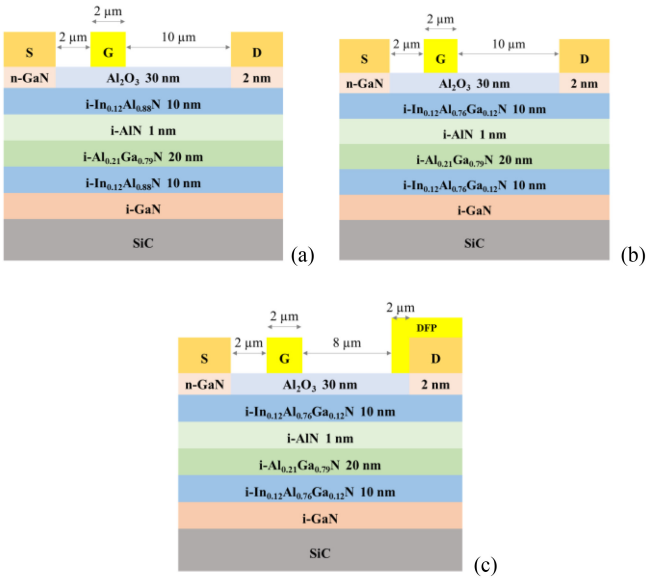


**FIGURE 1. Schematic device structures of (a) the control sample A1 and (b)-(c) the present MOS-HFET designs of samples B1-B2.**

transport would be degraded by the heterointerface defects and alloy scattering caused by different growth temperatures between InN and AlN during epitaxy. This work explores a novel $In_{0.12}Al_{0.76}Ga_{0.12}N$/AlN/ $Al_{0.21}Ga_{0.79}N$ heterostructural design to improve the carrier transport with preserved good polarization effect. Besides, a wide-gap $In_{0.12}Al_{0.76}Ga_{0.12}N$ ($In_{0.12}Al_{0.88}N$) buffer below the conduction channel was devised in the present (control) devices to enhance the carrier confinement, which would further increase both the electron concentration and current density. In addition, designs of MOS-gate, high-k gate dielectric, oxide passivation, and DFP [20], [21] were integrated to improve the gate modulation capability, reduce gate leakages, alleviate gate-drain electric field, and improve breakdown performance. $Al_2O_3$ was grown as gate dielectric and surface passivation layer at the same time by using a cost-effective non-vacuum ultrasonic spray pyrolysis deposition (USPD) [22], [23] technique.

## II. MATERIAL GROWTH AND DEVICE FABRICATION

Figs. 1(a)-(c) show the schematic device structures of (a) the control $In_{0.12}Al_{0.88}N$/AlN/$Al_{0.21}Ga_{0.79}N$ MOS-HFET (sample A1) and (b)/(c) the present $In_{0.12}Al_{0.76}Ga_{0.12}N$/AlN/ $Al_{0.21}Ga_{0.79}N$ MOS-HFET designs with/without DFP (samples B1/B2), respectively. The epitaxial structures were grown on a SiC substrate by using a low-pressure metal-organic chemical vapor deposition (LP-MOCVD) system. Both samples B1 and B2 have the same layer structures, including the GaN nucleation layer, an intrinsic 10-nm $In_{0.12}Al_{0.76}Ga_{0.12}N$ buffer, an intrinsic 20-nm $Al_{0.21}Ga_{0.79}N$ channel, an intrinsic 1-nm AlN layer, an intrinsic 10-nm $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier, and a 2-nm Si-doped ($\sim 3 \times 10^{18}$ $cm^{-3}$) GaN capping layer, as shown in Figs. 1(b) and (c). The control sample A1 has the identical epitaxial structures with respect to the present samples B1-B2, except replacing with the $In_{0.12}Al_{0.88}N$ barrier and buffer, as shown in Fig. 1(a).

All the three devices were fabricated at the same time. Standard photo-lithography and lift-off techniques were used for device fabrication [24]. For sample B2, mesa etching was first performed to provide electrical isolation for neighboring devices by using an inductively coupled-plasma reactive ion etcher (ICP-RIE). The etching gas is $BCl_3$ with a flow rate of 40 sccm. The ICP/RF power settings are both 110/110 W. The chamber pressure is 1 pa and the etching time is 500 seconds. Dry etching was conducted after photolithography to remove the GaN capper between source and drain electrodes. The flow rates of the $BCl_3/Cl_2$ mixture gases are 10/5 sccm, with the ICP/RF power settings of 100/12 W. The etching time is 80 seconds under chamber pressure of 1 pa. Metal stacks of Ti (20 nm)/Al (100 nm)/ Ni (20 nm)/Au (70 nm) were then evaporated as the source/drain electrodes. The source/drain ohmic contacts were formed by annealing the sample at 950°C for 60 seconds by using a ULVAC MILA-5000 rapid thermal annealing (RTA) system. Then, a 30-nm $Al_2O_3$ was grown on the exposed barrier surface between source and drain electrodes by using the USPD technique. Finally, after the photolithography to expose the gate/DFP windows, metal stacks of Ni (150 nm)/Au (40 nm) were evaporated on the $Al_2O_3$ surface to form both the gate and DFP structures, as shown in Fig. 1(c). The same fabrication procedures were applied to samples A1 and B1, except without the formation of DFP, as shown in Fig. 1(a) and 1(b). Besides, all three samples were gate recessed to the same depth by performing the dry etching simultaneously. The studied devices have the same gate length ($L_G$) of 2 $\mu$m, gate-to-source spacing of 2 $\mu$m, and gate-to-drain spacing of 10 $\mu$m. For sample B2, the DFP length ($L_{DFP}$) is 2 $\mu$m, which has resulted in an effective gate-to-drain separation of 8 $\mu$m.

The secondary ion-mass spectroscopy (SIMS) profiles of (a) the epitaxial structure (sample A) for the control device and (b) the present epitaxial design (sample B) for samples B1-B2, as shown in Figs. 2(a)-(b), respectively. Under the n-GaN capping layer, apparent decreases in the Ga-composition distribution were observed in sample A, as compared to sample B. The composition variations of the epitaxial structures were verified with the sample designs. The cross-sectional transmission electron microscopy (TEM) photo of the MOS-gate of sample B2 is also shown in Fig. 2(c). The layer thickness of the USPD-grown $Al_2O_3$ was verified to be 30 nm. Figs. 3(a) and 3(b) show the atomic force microscopy (AFM) photos of surface morphologies for the $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier of sample B2 after the gate-recess etching and further after the deposition of $Al_2O_3$ by using USPD, respectively. The average root-mean-square surface roughness after (before) the USPD-deposited $Al_2O_3$ was determined to be 0.6 (0.77) nm. The surface flatness was apparently degraded by using ICP-RIE and, then, was effectively improved by using USPD.

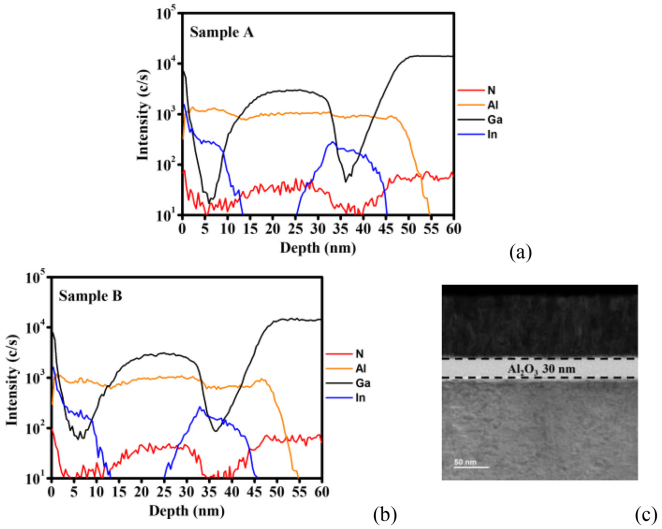


**FIGURE 2.** SIMS profiles of the epitaxial structures of samples (a) A and (b) B; (c) the TEM photo of MOS-gate for the present sample B2.

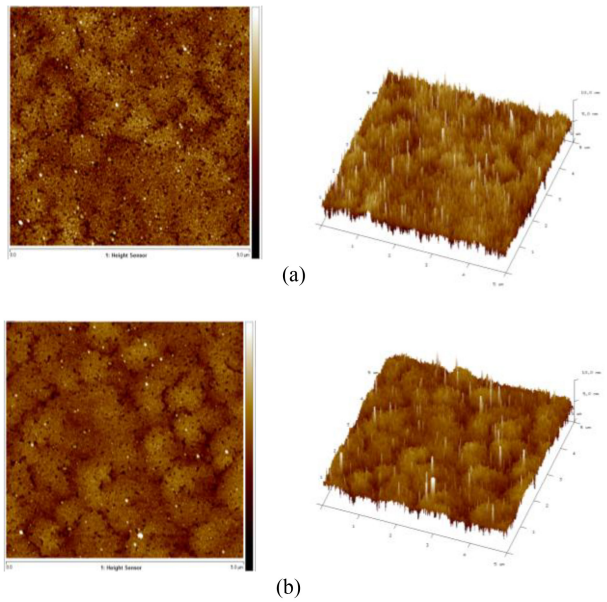


**FIGURE 3.** AFM photos of surface morphologies for the $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier of sample B2 (a) after the gate-recess etching and (b) further after deposition of $Al_2O_3$ by using USPD.

## III. EXPERIMENTAL RESULTS AND DISCUSSION

Hall measurements were conducted for both samples A and B at 300 K under a magnetic field of 5000 G. The electron mobility ($\mu_n$), two-dimensional electron gas concentration ($n_{2DEG}$), and he $\mu_n$-$n_{2DEG}$ product were found to be 417 (282) $cm^2$/V-sec, 3.6 (3.5) $\times$ $10^{13}$ $cm^{-2}$, and 1.5 (0.99) $\times$ $10^{16}$ $(V\text{-sec})^{-1}$ for sample B (A). Samples A-B have similar $n_{2DEG}$ concentrations since the same In-ratio of 0.12 was devised for the $In_{0.12}Al_{0.88}N$ and $In_{0.12}Al_{0.76}Ga_{0.12}N$ barriers. Similar polarization effects were maintained to provide appropriate comparison for the studied devices. Due to enhanced carrier confinement by the devised

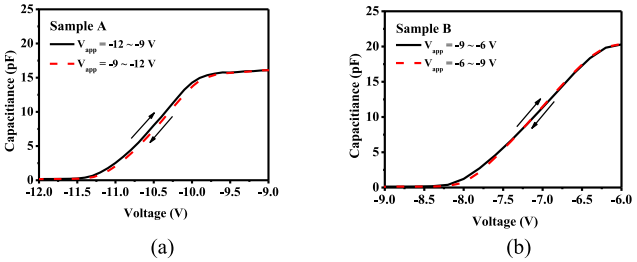


**FIGURE 4.** The measured C-V hysteresis characteristics for samples (a) A and (b) B at 300 K.

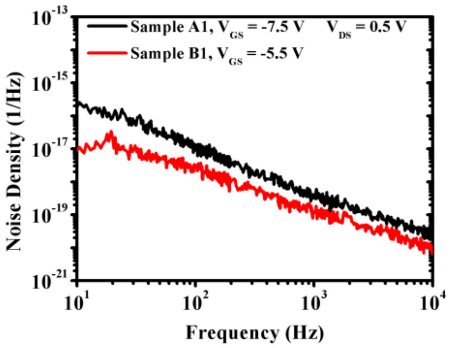


**FIGURE 5.** 1/*f* noise spectra of samples A1 and B1.

wide-gap $In_{0.12}Al_{0.76}Ga_{0.12}N$ or $In_{0.12}Al_{0.88}N$ barrier/buffer, the obtained $n_{2DEG}$ values are higher than our previous works [15], [16] and other InAlN/AlGaN device [25]. Moreover, the $\mu_n$ and $\mu_n$-$n_{2DEG}$ product of sample B have been significantly enhanced due to the improved interfacial property in the $In_{0.12}Al_{0.76}Ga_{0.12}N/AlN/Al_{0.21}Ga_{0.79}N$ heterostructure. High current densities are expected for the present $In_{0.12}Al_{0.88}N/AlN/Al_{0.21}Ga_{0.79}N$ MOS-HFET designs.

The measured C-V hysteresis characteristics for the fabricated MOS diodes for samples A and B are shown in Figs. 4(a)-(b), respectively. The diode areas are the same of 31400 $\mu m^2$. The applied voltage was increased from $-9$ V to 6 V and swept back immediately to the starting voltage. The hysteresis voltage ($\Delta V$) was defined to be the bias difference between mid-points of the C-V curves. The $\Delta V$ was determined to be about 1 (37) mV for sample B (A). Significant decrease in $\Delta V$ for sample B, as compared to sample A, has been obtained, indicating the interface property was effectively improved by using the $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier. Fig. 5 shows the 1/*f* noise spectra of samples A1 and B1 biased at $V_{GS} = -7.5$ V and $-5.5$ V with $V_{DS} = -0.5$ V, measured by using an Agilent 35670A amplifier and a BTA 9812B spectrum analyzer. The Hooge coefficients ($\alpha_H$) at $f = 100$ Hz were determined [26] to be $1.4 \times 10^{-5}$ and $2.3 \times 10^{-6}$ for samples A1 and B1 with the corresponding noise densities of $1.2 \times 10^{-17}$ and $2.9 \times 10^{-18}$ $Hz^{-1}$. Lower 1/*f* noise floor and lower $\alpha_H$ of sample B1 than those of sample A1 also indicate its improved interfacial quality. The surface electron trapping phenomenon [27]

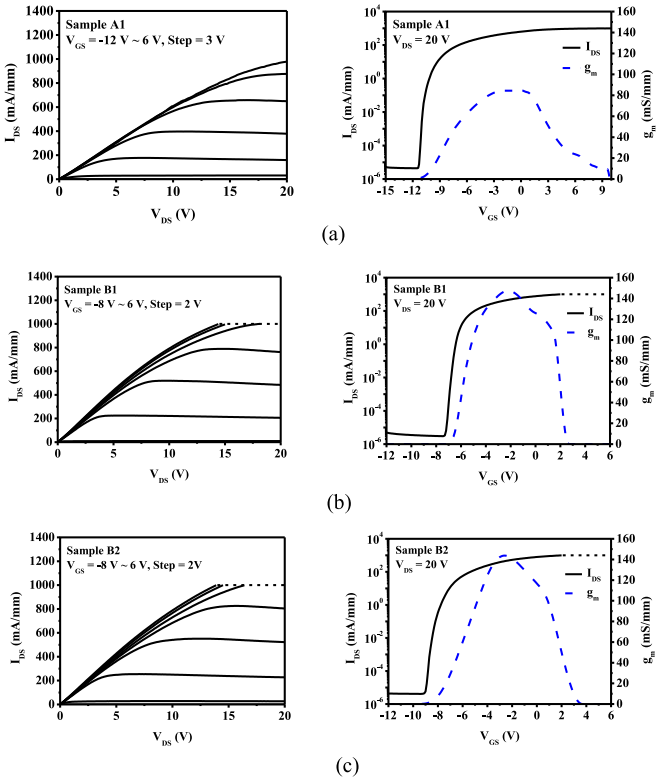


**FIGURE 6. Common-source $I_{DS}$-$V_{DS}$ characteristics (left) at 300 K and the transfer $g_m$ and $I_{DS}$ as functions of $V_{GS}$ (right) for samples (a) A1, (b) B1, and (c) B2, respectively.**

was effectively reduced by the oxide passivation by using USPD. The comparisons of both $\Delta V$ and $\alpha_H$ are consistent with the observed enhanced $\mu_n$ behavior in the devised $In_{0.12}Al_{0.76}Ga_{0.12}N/AlN/Al_{0.21}Ga_{0.79}N$ heterostructure. Besides, the transfer length method (TLM) [28] was employed to measure the specific contact resistivity ($\rho_c$) and contact resistances ($R_C$). $\rho_c$ and $R_C$ were characterized to be $8.7 \times 10^{-6}$ ($1.8 \times 10^{-5}$) $\Omega$-cm$^2$ and 0.18 (0.26) $\Omega$-mm for samples B1-B2 (A1), which are much lower than those wide-gap channel devices of our previous works [15], [16]. It is mainly contributed by the devised n-GaN capping layer to greatly improve the source/drain ohmic contacts. The improved interfacial quality by using the $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier has further improved the ohmic contact characteristics.

The common-source current-voltage ($I_{DS}$-$V_{DS}$) characteristics source/drain ohmic contacts. The improved interfacial quality (left) at 300 K and the transfer extrinsic transconductance ($g_m$) and saturated drain-source current ($I_{DS}$) density vs. the applied $V_{GS}$ for samples A1, B1, and B2 are shown in Figs. 6(a)-(c), respectively. The applied $V_{GS}$ bias was increased from $-8$ ($-12$) V to 6 (6) V at 2 (3) V/step for samples B1-B2 (A1) by using a KEITHLEY 4200 analyzer. All the studied devices have shown good pinch-off phenomena, indicating the good gate modulation capability by the high-k MOS-gate structure. As expected by the Hall data, the enhanced current densities in samples B1-B2 have exceeded the instrumentation limit of the KEITHLEY 4200 analyzer, as observed in Figs. 6(b)-(c). The measured $I_{DS}$ at $V_{GS} =$ 0 V ($I_{DSS0}$) and maximum $I_{DS}$ ($I_{DS,max}$) densities at $V_{DS} =$ 20 V were found to be 628 mA/mm and 978.5 mA/mm, 755 mA/mm and >1 A/mm, and 791.1 mA/mm and >1 A/mm for samples A1, B1, and B2, respectively. The corresponding maximum extrinsic transconductance ($g_{m,max}$) values are 89.7 mS/mm, 148.3 mS/mm, and 150.8 mS/mm. Both samples B1 and B2 have demonstrated superior current drive capability. It was contributed by the improved channel conductivity by the devised $In_{0.12}Al_{0.76}Ga_{0.12}N/AlN/Al_{0.21}Ga_{0.79}N$ heterostructure. Sample B2 (B1) has shown about 26% (20%) and 68% (65%) improvements in $I_{DSS0}$ and $g_{m,max}$ performances as compared to sample A1. Higher $I_{DSS0}$ density of sample B2 than B1 is due to the increased electric field resulted from the decreased gate-to-drain spacing by the inserted 2-$\mu$m DFP structure, as shown in Fig. 1(c). Consequently, enhanced $g_{m,max}$ performances have been achieved by the improved current densities in the present samples B1 and B2. The devised MOS-HFETs are superior to our previous woks [15], [16] and other wide-gap-channel devices of $g_{m,max} = 16$ mS/mm and $I_{DS,max} = 90$ mA/mm [25], $g_{m,max} = 9$ mS/mm and $I_{DS,max} =$ 350 mA/mm [29], $I_{DS,max} = 114$ mA/mm [30], $g_{m,max} =$ 38 mS/mm and $I_{DS,max} = 635$ mA/mm [31], $I_{DS,max} =$ 420 mA/mm [32], $g_{m,max} = 2.4$ mS/mm and $I_{DS,max} =$ 13 mA/mm [33], and $g_{m,max} = 97.9$ mS/mm and $I_{DS,max} =$ 473 mA/mm [34].

The gate-voltage swing (GVS) was defined to be the available $V_{GS}$ range where the $g_m$ value was within 90% of $g_{m,max}$. Sample A has wider GVS of 4.9 V than 2.9 (2.3) V of sample B1 (B2), indicating its good linearity. The threshold voltage ($V_{th}$) was defined as the $V_{GS}$ intercept by the extrapolated line of $(I_{DS})^{1/2}$. Sample A1 has the lowest $V_{th}$ of about $-11$ V as compared to $-6.8$ ($-8.6$) V of sample B1 (B2). The observed small $V_{th}$ deviations from the C-V curves in Fig. 4 was due the different anode/cathode separation as compared to the MOS-HFETs. Higher GVS and lower $V_{th}$ of sample A1 than sample B1 were due to its wider bandgap and higher conduction-band discontinuity ($\Delta E_C$) of the $In_{0.12}Al_{0.88}N$ barrier/buffer than those of $In_{0.12}Al_{0.76}Ga_{0.12}N$. Moreover, higher $I_{DS}$ density of sample B2 has resulted in its lower $V_{th}$ value than sample B1, since more negative $V_{GS}$ was needed to deplete the channel. The specific on-resistances ($R_{on,sp}$) of samples A1, B1, and B2 were determined to be 5.14 m$\Omega$/cm$^2$, 2.81 m$\Omega$/cm$^2$, and 2.83 m$\Omega$/cm$^2$. The present samples B2/B1 with/without DFP have shown comparable $R_{on,sp}$ values. They have also exhibited lower $R_{on,sp}$ than sample A1. Since $R_{on,sp}$ was extracted at low electric fields, reduced $R_{on,sp}$ was resulted from the improved channel conductivity by the devised $In_{0.12}Al_{0.76}Ga_{0.12}N/AlN/Al_{0.21}Ga_{0.79}N$ heterostructure. It is consistent with the characterized Hall data. The present devices has shown lower $R_{on,sp}$ than other AlGaN channel devices [25], [35]. Besides, the subthreshold swing (SS)

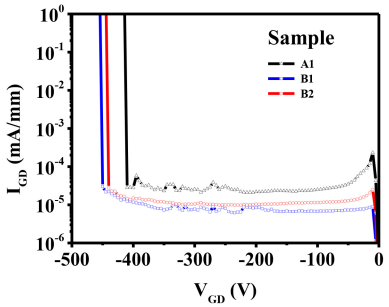


**FIGURE 7.** Two-terminal off-state $BV_{GD}$ characteristics at 300 K for samples A1, B, and B2.

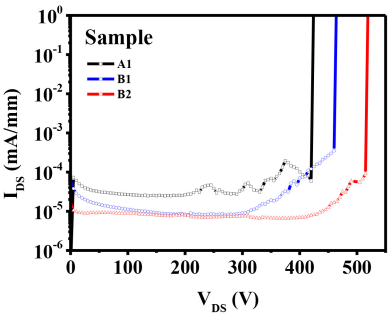


**FIGURE 8.** Three-terminal on-state BVDS characteristics at 300 K for samples A1, B, and B2.

and on/off-current ratios ($I_{on}/I_{off}$) for the studied samples A1, B1, and B2 were found to be 112.2 mV/dec and $2.2 \times 10^8$, 104 mV/dec and $> 10^9$, and 124.3 mV/dec and $> 10^9$, respectively. The studied devices have shown higher $I_{on}/I_{off}$ ratios than other works [25], [29], [35]. It was due to the devised $In_{0.12}Al_{0.88}N$ or $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier/buffer, since $I_{on}$ was increased by the improved self-polarization effect, whereas the $I_{off}$ densities were reduced by the wide-gap barrier/buffer. Besides, improved gate insulation, $g_{m,max}$ gain, and $I_{DS}$ density resulted from the MOS-gate design with high-k dielectric, wide-gap $Al_2O_3$, and good surface passivation have also contributed to the enhanced switching performance. Moreover, the $I_{off}$ leakage in sample B2 was further suppressed by the DFP design. High $I_{on}/I_{off}$ and superior SS performances with decreased $R_{on,sp}$ of the present design are advantageous to the power-switching circuit applications.

The two-terminal off-state gate-drain breakdown voltage ($BV_{GD}$) and three-terminal on-state drain-source breakdown voltage ($BV_{DS}$) characteristics of samples A1, B1, and B2 at 300 K are shown in Figs. 7 and 8, respectively. $BV_{GD}$ and $BV_{DS}$ were determined to be the corresponding $V_{GD}$ and $V_{DS}$ biases where the $I_{GD}$ and $I_{DS}$ densities were equal to 1 $\mu$A/mm. The source terminal remained float while characterizing $BV_{GD}$, and the $V_{GS}$ was biased at $-12$ V for measuring $BV_{DS}$ for all devices. $BV_{GD}$ and $BV_{DS}$ were found to be $-410$ V and 425 V, $-465$ V and 460 V, and $-455$ V and 515 V for samples A1, B1, and B2. Good breakdown characteristics have been

**TABLE 1.** Device characteristics of the studied samples.

| Sample | A1 | B1 | B2 |
|---|---|---|---|
| $I_{DSS0}$ (mA/mm) | 628 | 755 | 791.1 |
| $I_{DS,\,max}$ (mA/mm) | 978.5 | > 1000 | > 1000 |
| $g_{m,\,max}$ (mS/mm) | 89.7 | 148.3 | 150.8 |
| $V_{th}$ (V) | -11 | -6.8 | -8.6 |
| $GVS$ (V) | 4.9 | 2.9 | 2.3 |
| $I_{on}/I_{off}$ | $2.2 \times 10^8$ | $> 10^9$ | $> 10^9$ |
| $SS$ (mV/dec) | 112.2 | 104 | 124.3 |
| $R_{on,\,sp}$ (m$\Omega$/cm$^2$) | 5.14 | 2.81 | 2.83 |
| $BV_{GD}$ (V) | -410 | -465 | -455 |
| $BV_{DS}$ (V) | 425 | 460 | 515 |
| $BV_{DS}^2/R_{on,\,sp}$ (mW/cm$^2$) | 35.1 | 75.4 | 93.7 |

obtained in the studied devices. It is attributed by the reduced gate/substrate leakage currents by the devised MOS-gate structure with the USPD-grown $Al_2O_3$ surface passivation, wide-gap $Al_{0.21}Ga_{0.79}N$ channel, and wide-gap barrier/buffer using $In_{0.12}Al_{0.76}Ga_{0.12}N$ or $In_{0.12}Al_{0.88}N$ compounds. About 13% improvement in $BV_{GD}$ was obtained in sample B1 with respect to sample A1. It is possibly due to the decreased gate leakage by improved interfacial quality of the devised $In_{0.12}Al_{0.76}Ga_{0.12}N$/AlN/ $Al_{0.21}Ga_{0.79}N$ heterostructure, as discussed before. Though $BV_{GD}$ was slightly degraded in sample B2 due to reduced gate-to-drain separation, it has shown about 21% (12) improvement in $BV_{DS}$ as compared to sample A1 (B1). It is because that the electric field distribution has been effectively smoothed out [21] by the DFP design. $BV_{DS}^2/R_{on,sp}$ is known as an important device figure-of-merit (FOM) for power switching applications. The present $In_{0.12}Al_{0.76}Ga_{0.12}N$/AlN/$Al_{0.21}Ga_{0.79}N$ MOS-HFET with (without) DFP design has shown superior device FOM of 93.7 (75.4) MW/cm$^2$ as compared to other AlGaN channel devices [25], [34], [35]. Table 1 summarizes the device characteristics of the studied devices. Superior current densities, high breakdown voltages, and improved switching characteristics have been successfully achieved in the present design.

## IV. CONCLUSION

Wide-gap-channel $In_{0.12}Al_{0.76}Ga_{0.12}N$/AlN/$Al_{0.21}Ga_{0.79}N$ MOS-HFETs grown on a SiC substrate with/without DFP have been reported for the first time. Superior $I_{DS,max}$ in excess of 1 A/mm with low $R_{on,sp}$ has been achieved due to improved polarization effect, interfacial property, and carrier confinement by the $In_{0.12}Al_{0.76}Ga_{0.12}N$ barrier/buffer design. The DFP was further integrated to improve the breakdown

performance. A reference $In_{0.12}Al_{0.88}N/AlN/Al_{0.21}Ga_{0.79}N$ MOS-HFET was fabricated in comparison. The present $In_{0.12}Al_{0.76}Ga_{0.12}N/AlN/$ $Al_{0.21}Ga_{0.79}N$ MOS-HFET design with (without) DFP has demonstrated superior $I_{DSS0}$ of 791.1 (755) mA/mm, $I_{DS,max}$ of >1 (>1) A/mm, $g_{m,max}$ of 150.8 (148.3) mS/mm, GVS of 2.3 (2.9) V, $I_{on}/I_{off}$ of $>10^9$ ($>10^9$), SS of 124.3 (104) mV/dec, $R_{on,sp}$ of 2.83 (2.81) $m\Omega/cm^2$, $BV_{GD}$ of −455 (−465) V, $BV_{DS}$ of 515 (400) V, and $BV_{DS}^2/R_{on,sp}$ of 93.7 (75.4) $MW/cm^2$. The present MOS-HFET design possessing high current drive capability, low $R_{on}$, and high device FOM is especially advantageous to shorten the battery charging time and improve the battery charging efficiency for the electric vehicle applications.

## REFERENCES

[1] Y. Guan, Y. Wang, D. Xu, and W. Wang, "A 1 MHz half-bridge resonant DC/DC converter based on GaN FETs and planar magnetics," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2876–2891, Apr. 2017.

[2] A. Martinez-Perez, A. K. Solomon, A. Castellazzi, and B. Lu, "GaN-based consumer application DC-DC converter for PCB embedment technology integration," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Nov. 2015, pp. 2100–2105.

[3] M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48-V VRM with intermediate bus voltage optimization for data centers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 702–715, Feb. 2021.

[4] H. V. Nguyen, D.-C. Lee, and F. Blaabjerg, "A novel SiC-based multifunctional onboard battery charger for plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5635–5646, May 2021.

[5] M. Abbasi, R. Emamalipour, M. A. M. Cheema, and J. Lam, "A new fully magnetically coupled SiC-based DC/DC step-up LLC resonant converter with inherent balanced voltage sharing for renewable energy systems with a medium voltage DC grid," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 5542–5547.

[6] T. Nanjo et al., "First operation of AlGaN channel high electron mobility transistors," *Appl. Phys. Exp.*, vol. 1, no. 1, pp. 1–3, Jan. 2008.

[7] T. Nanjo et al., "AlGaN channel HEMT with extremely high breakdown voltage," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1046–1053, Mar. 2013.

[8] M. Xiao et al., "High performance $Al_{0.10}Ga_{0.90}N$ channel HEMTs," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1149–1151, Aug. 2018.

[9] I. Abid et al., "AlGaN channel high electron mobility transistors with regrown ohmic contacts," *Electronics*, vol. 10, no. 6, p. 635, Mar. 2021.

[10] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, vol. 26, pp. 163–177, Jun. 1965.

[11] B. J. Baliga, "Semiconductors for high-voltage, vertical channel field-effect transistors," *J. Appl. Phys.*, vol. 53, no. 3, pp. 1759–1764, Mar. 1982.

[12] M. M. Morcos, N. G. Dillman, and C. R. Mersman, "Battery chargers for electric vehicles," *IEEE Power Engr. Rev.*, vol. 20, no. 11, pp. 8–10, Nov. 2000.

[13] T. Kachi, "Recent progress of GaN power devices for automotive applications," *Jap. J. Appl. Phys.*, vol. 53, no. 10, Sep. 2014, Art. no. 100210.

[14] R. Ma, K. H. Teo, S. Shinjo, K. Yamanaka, and P. M. Asbeck, "A GaN PA for 4G LTE-advanced and 5G: Meeting the telecommunication needs of various vertical sectors including automobiles, robotics, health care, factory automation, agriculture, education, and more," *IEEE Microw. Mag.*, vol. 18, no. 7, pp. 77–85, Nov./Dec. 2017.

[15] C. S. Lee, K. T. Lee, W. C. Hsu, H. Y. Liu, W. L. Yang, and C. H. Ko, "Investigations on $Al_2O_3$-dielectric wide-gap $Al_{0.3}Ga_{0.7}N$ channel MOS-HFETs with composite $Al_2O_3$/In Situ SiN passivation," *ECS J. Solid State Sci. Technol.*, vol. 11, Aug. 2022, Art. no. 85002.

[16] C. S. Lee, Y. T. Shen, W. C. Hsu, Y. P. Huang, and C. Y. You, "$Al_{0.75}Ga_{0.25}N/Al_xGa_{1-x}N/Al_{0.75}Ga_{0.25}N/AlN/SiC$ metal–oxide–semiconductor heterostructure field-effect transistors with symmetrically-graded widegap channel," *IEEE J. Electron Devices Soc.*, vol. 8, no. 1, pp. 9–14, Dec. 2019.

[17] C. S. Lee, C. L. Li, W. C. Hsu, C. Y. You, and H. Y. Liu, "Enhancement-mode characteristics of $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N/AlN/$ SiC MOS-HFETs," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 1003–1008, 2021.

[18] O. Ambacher, M. Yassine, B. Christian, M. Baeumler, S. Leone, and R. Quay, "Polarization induced interface and electron sheet charges of pseudomorphic ScAlN/GaN, GaAlN/GaN, InAlN/GaN, and InAlN/InN heterostructures," *J. Appl. Phys.*, vol. 129, no. 20, May 2021, Art. no. 204501.

[19] S. Ganguly, A. Konar, Z. Hu, H. Xing, and D. Jena, "Polarization effects on gate leakage in InAlN/AlN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 101, no. 25, Dec. 2012, Art. no. 253519.

[20] A. Minetto et al., "Drain field plate impact on the hard-switching performance of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5003–5008, Oct. 2021.

[21] B. Liao, Q. Zhou, J. Qin, and H. Wang, "Simulation of AlGaN/GaN HEMT's breakdown voltage enhancement using gate field-plate, source field-plate, and drain field-plate," *Electronics*, vol. 8, no. 4, p. 406, Apr. 2019.

[22] B. Y. Chou et al., "$Al_2O_3$-passivated AlGaN/GaN HEMTs by using nonvacuum ultrasonic spray pyrolysis deposition technique," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 903–905, Sep. 2014.

[23] C. S. Lee, W. C. Hsu, H. Y. Liu, and Y. C. Chen, "$Al_2O_3$-Dielectric $In_{0.18}Al_{0.82}N/AlN/GaN/Si$ metal-oxide-semiconductor heterostructure field-effect transistors with backside substrate metal-trench structure," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 68–73, 2017.

[24] C. C. Cheng, "Investigations on wide-gap AlGaN channel MOS-HFETs with InAlGaN barrier layer." M.S. thesis, Dept. Electron. Eng., Feng Chia Univ., Taichung, Taiwan, Jul. 2022.

[25] J. J. Freedsman, T. Hamada, M. Miyoshi, and T. Egawa, "$Al_2O_3$/AlGaN channel normally-off MOSFET on silicon with high breakdown voltage," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 497–500, Feb. 2017.

[26] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, "Experimental studies on 1/*f* noise," *Rep. Progr. Phys.*, vol. 44, no. 5, pp. 479–532, 1981.

[27] K. Omika et al., "Dynamics of surface electron trapping of a GaN-based transistors revealed by spatiotemporally resolved X-ray spectroscopy," *Appl. Phys. Lett.*, vol. 117, Oct. 2020, Art. no. 171605.

[28] D. K. Schroder, *Semiconductor Materials and Device Characterization*. Hoboken, NJ, USA: Wiley, 2003.

[29] S. Bajaj et al., "High Al-content AlGaN transistor with 0.5 A/mm current density and lateral breakdown field exceeding 3.6 MV/cm," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 256–259, Feb. 2018.

[30] T. Nanjo et al., "Remarkable breakdown voltage enhancement in AlGaN channel high electron mobility transistors," *Appl. Phys. Lett.*, vol. 92, Jun. 2008, Art. no. 263502.

[31] T. Razzak et al., "Design of compositionally graded contact layers for MOCVD grown high Al-content AlGaN transistors," *Appl. Phys. Lett.*, vol. 115, Jul. 2019, Art. no. 43502.

[32] H. Xue et al., "All MOCVD grown $Al_{0.7}Ga_{0.3}N/Al_{0.5}Ga_{0.5}N$ HFET: An approach to make ohmic contacts to Al-rich AlGaN channel transistors," *Solid State Electron.*, vol. 164, Feb. 2020, Art. no. 107696.

[33] H. Tokuda et al., "High Al composition AlGaN-channel high-electron-mobility transistor on AlN substrate," *Appl. Phys. Exp.*, vol. 3, Dec. 2010, Art. no. 121003.

[34] Y. Zhang et al., "High-performance AlGaN double channel HEMTs with improved drain current density and high breakdown voltage," *Nanoscale Res. Lett.*, vol. 15, p. 114, May 2020.

[35] J. Lemettinen, N. Chowdhury, H. Okumura, I. Kim, S. Suihkonen, and T. Palacios, "Nitrogen-polar polarization-doped field-effect transistor based on $Al_{0.8}Ga_{0.2}N/AlN$ on SiC with drain current over 100 mA/mm," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1245–1248, Aug. 2019.