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Depletion- and Enhancement-Mode p-Channel MISHFET Based on GaN/AlGaN Single Heterostructures on Sapphire Substrates

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ABSTRACT We report on p-channel metal-insulator-semiconductor heterostructure field-effect transistors (MISHFET) based on p-GaN/uid-GaN/$Al_{0.29}Ga_{0.71}N$ single heterostructures on sapphire substrates, grown by metalorganic vapor phase epitaxy (MOVPE). The impact of p-GaN layer removal and channel layer thickness adjustment by dry-etching on the characteristics of the MISHFET are investigated. Depending on the remaining GaN thickness (t_{GaN}), the fabricated MISHFET show either depletion-mode (d-mode) operation with a threshold voltage V_{th} of 3.8 V and an on-current $|I_{D,on}|$ of 9.5 mA/mm ($t_{GaN} = 21$ nm) or enhancement-mode (e-mode) operation with V_{th} of -2.3 V and $|I_{D,on}|$ of 1.5 mA/mm ($t_{GaN} = 12$ nm). Independent of the etching depth, all devices exhibit a very low off-state drain current $|I_{D,off}| \sim 10^{-8}$ mA/mm and a steep subthreshold swing (SS) between 80 and 89 mV/dec. Similar to n-channel devices, a V_{th} instability caused by charge trapping at the dielectric/semiconductor interface is found, emphasizing that careful interface engineering is required for good device performance.

INDEX TERMS 2DHG, p-channel, e-mode, MISHFET.

I. INTRODUCTION

In order to exploit the full potential of wide-bandgap III-nitrides for high-performance electronics, p-channel transistors of e-mode type and with properties comparable to their n-channel counterparts are required [1]. High electron mobility transistors (HEMT) are generally based on metal-polar Al(Ga,In)N/GaN heterostructures, which induce a high-density, high-mobility two-dimensional electron gas (2DEG) that constitutes the transistor channel. Coupled with the ability to handle high voltages, GaN HEMT are very attractive for switching large voltages or generating high powers at RF frequencies [1].

p-Channel field-effect transistors (FET) on the other hand, which are typically based on a GaN/Al(Ga,In)N heterostructure, lag far behind their n-channel counterparts, due to challenging growth and processing issues. Nevertheless, p-channel FET are of interest for several applications requiring high-temperature operation or for complementary logic in analogy with CMOS [2]. Reported p-channel transistors realized by metalorganic vapor phase epitaxy (MOVPE) are typically based on an Al(In)GaN barrier with an unintentionally doped (uid) GaN channel layer on top, both grown pseudomorphically on a relaxed GaN buffer [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. Furthermore, p-GaN-gated HEMT structures, originally developed for high-power switches, have been most recently utilized to investigate p-channel devices [15], [16], [17], [18], [19], [20]. The double-heterostructure design typically results in the formation of a 2DEG below and a 2DHG above the Al(In)GaN barrier [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [40]. This can be advantageous for monolithic integration of n- and p-channel devices [6], [7], [8], [20] on the same wafer, but it could also be an issue due to parasitic coupling of n- and p-channels, leakage at elevated temperature etc. [4], [40]. Single GaN/AlN

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heterostructures, which contain only a 2DHG, are usually realized by molecular beam epitaxy (MBE) on single-crystal AlN substrates or templates [21], [22], [23], [24], [25]. Based on these binary heterostructures, p-channel transistors with the highest reported carrier ($\sim 5\times10^{13}$cm^{-2}) and current densities (~400 mA/mm) were shown. However, these devices often suffer from a low on/off current ratio ($\leq 10^4$) [23], [24], [25]. The high cost associated with AlN substrates may also be considered as a severe drawback. The challenges of heteroepitaxial growth of high-quality AlGaN buffer layers on foreign substrates like Si or sapphire have limited reports on such structures to just a few [45], [46], [47].

This work presents p-channel metal-insulator-semiconductor heterostructure field-effect transistors (MISHFET) based on a p-GaN/uid-GaN/$Al_{0.29}Ga_{0.71}N$ single heterostructure grown by MOVPE on an AlN buffer layer on sapphire. In contrast to the common double-heterostructure approach using a relaxed GaN buffer, a partially relaxed (85 %) AlGaN buffer layer is employed here. A nominally undoped GaN channel is grown strained on the AlGaN buffer, and only a 2DHG channel is induced by the polarization difference between these two layers (Fig. 1 (a)). This structure allows the adjustment of the threshold voltage from d-mode to e-mode by appropriate choice of the channel thickness. By inserting Al_2O_3 as a leakage reducing gate dielectric, MISHFET operation with large on/off ratios can be targeted.

A common challenge for p-channel devices is to enable low-resistive ohmic contacts [26]. Contact properties can be improved by growing a highly doped p-GaN contact layer [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26] on top of the uid-GaN channel, in which the 2DHG is formed. In the past, due to the relatively large n-type uid concentration in GaN, the channel had to be either intentionally p-doped [27] instead or the p-GaN contact layer above was also explicitly utilized as a carrier supply layer for the channel (similar to conventional III-V HEMT) in earlier publications [3], [4], [5], [6]. The high quality of today's state-of-the-art GaN no longer requires such uid-GaN channel background compensation [22].

The p-GaN ohmic contact layer makes it however challenging to realize FET with good gate control. Therefore, p-GaN needs to be removed or at least recessed in the active area. Another aspect is the known diffusivity of Mg in GaN [42] at MOVPE growth temperatures which can result in parasitic p-type doping of the GaN channel below the p-GaN contact layer. In the following, we investigate the effect of etching the p-GaN contact layer and thinning down the GaN channel on the characteristics of the fabricated transistors. Extensive Hall and DC characterization of test structures and FET is performed. Additionally, C-V (capacitance-voltage) measurements are employed to analyze the impact of implementing the gate dielectric Al_2O_3.

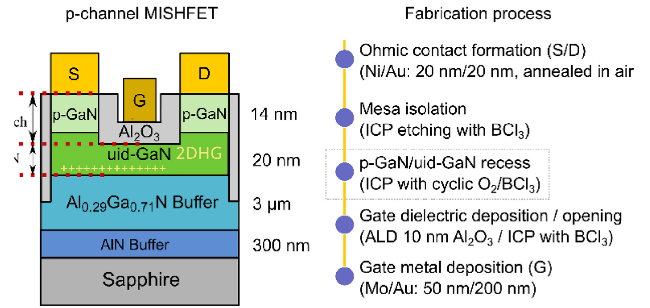

FIGURE 1. (a) Schematic device structure of the p-channel MISHFET with etching depth D_{etch} of the (p-)GaN recess and the corresponding remaining GaN layer thickness t_{GaN}. (b) Simplified process flow. The ohmic source (S) and drain (D) contacts consist of Ni/Au (20/20 nm) and the gate (G) contact of Mo/Au (50/200 nm).

II. EXPERIMENTAL

The p-GaN/uid-GaN/AlGaN/AlN stack was grown on a 2-inch sapphire substrate in an AIXTRON 200/4 RF-S MOVPE system. The epitaxial structure (Fig. 1 (a)) consists of a 300 nm AlN buffer layer (low-temperature AlN nucleation and high-temperature AlN), a ~3 μm AlGaN buffer layer, a 20 nm uid-GaN channel layer and a 14 nm p-GaN cap (Mg: $\sim 3\cdot10^{19}$ cm^{-3}). From high-resolution X-ray diffraction analysis, we have determined the Al content and relaxation of the buffer layer to be x = 0.29 and ~85 % respectively. The FWHM of the asymmetric (105) AlGaN reflex determined from a reciprocal space map is equal to 324 arcsec at a distance of 20 mm off-center. The GaN layer (consisting of p-GaN contact and uid-GaN channel layer) is found to be pseudomorphically grown on the AlGaN buffer layer with ~ 4 % relaxation. More details on the growth as well as the dependence of the structural and electrical properties on the Al content in the barrier and on the GaN channel thickness are discussed in [45].

After growth, Mg activation was performed in an RTA (rapid thermal annealing) system in N_2 atmosphere at 700 °C for 15 minutes. Subsequently, test structures for characterization by Hall and transmission line measurements (TLM) as well as MISHFET devices were fabricated. The process flow is sketched in Fig. 1 (b). On the whole 2-inch wafer, ohmic source and drain contacts, consisting of Ni/Au (20/20 nm), were deposited by e-beam evaporation and thermally annealed in air at 535 °C for 10 minutes. The devices were isolated using an ICP-RIE (inductively coupled plasma - reactive-ion etching) mesa etch process with BCl_3 (~100 nm etching depth). After characterization by Hall measurements and TLM, the wafer (sample ED0) was diced into four samples. For each piece, a (p-)GaN recess with different etch depths D_{etch} was performed by cyclic O_2/BCl_3 ICP-RIE digital etching [18]. The ohmic contacts served as etch masks in this process. The etching depth per cycle was previously determined by AFM (atomic force microscopy) to 3.2 nm using calibration samples. The number of cycles used for each sample piece determines its name: ED4, ED5, ED6 and ED7. With the initial total GaN layer

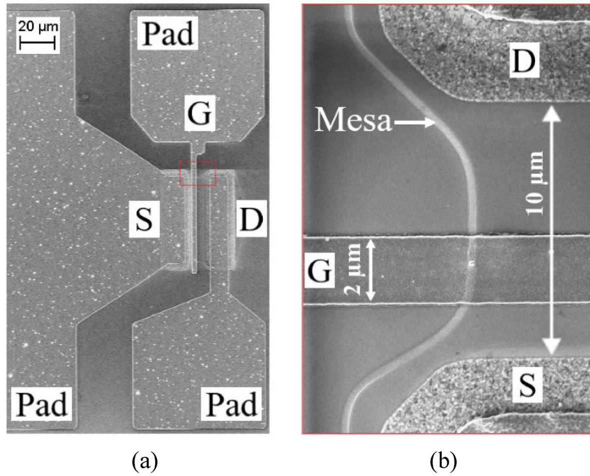

FIGURE 2. (a) Top-view SEM images of the fabricated p-channel MISHFET, with G: gate, S: source and D: drain. (b) Zoomed-in image of the active device region.

thickness of 34 nm of the unetched ED0 (20 nm uid-GaN +14 nm p-GaN), the remaining GaN thicknesses t_{GaN} of ED4 – ED7 can be calculated from the number of cycles (see Tab. 1). Taking the nominal etch rate and thicknesses into account, we expect sample ED4 to have been etched such that an ultra-thin p-GaN layer is left on top of the GaN, whereas sample ED5 is expected to be recessed slightly into the uid-GaN channel

To form the MISHFET gate dielectric, 10 nm Al_2O_3 were grown by plasma-enhanced atomic layer deposition (PEALD). Al_2O_3 also serves as a surface passivation in the access regions [38]. The PEALD process was performed at a substrate temperature of 300 °C, and oxygen and trimethylaluminum were used as precursors. Finally, after exposing the ohmic contacts by dry etching (BCl_3-based ICP-RIE), metallic gates and contact pads consisting of 50 nm Mo and 200 nm Au are evaporated in one process step (cf. Fig. 1 (b)). In Fig. 2, top-view SEM images of the fabricated p-channel MISHFET with a gate-length $L_G = 2\ \mu$m, drain-source distance $L_{DS} = 10\ \mu$m and gate width $W_G = 50$ are shown. Hall measurements were repeated after Al_2O_3 deposition. The results are discussed further below, but it should be mentioned already here that the carrier concentration and mobility values for samples ED4 - ED6 were found to be almost identical within the margin of error *before and after* Al_2O_3 deposition. Sample ED7 yielded measurable values only when covered with Al_2O_3 (s. Tab. 1).

III. RESULTS AND DISCUSSION

A. OHMIC CONTACTS AND 2DHG PROPERTIES

The unetched sample ED0 was characterized by TLM measurements (Fig. 3 (a)). Extracted values for specific contact resistivity (r_c) and normalized contact resistance (R_C) are in the range of 2.0×10^{-4} Ωcm^2 and 21.0 Ωmm. A specific ohmic contact resistivity r_c of $\sim1\times10^{-4}$ Ωcm^2 for ohmic contacts on p-GaN is within the range of published values

TABLE 1. Overview of the samples with varying etching depth D_{etch} and corresponding remaining total GaN thickness t_{GaN}. The 2DHG density p_S and mobility μ_p determined by Hall measurements before and after Al_2O_3 deposition.

Sample	D_{etch} (nm)	t_{GaN} (nm)	p_S (x10^{12} cm^{-2})	μ_p (cm²/Vs)
ED0	0	34	16.5/-	14.1/-
ED4	12.8	21.2	13.1/13.2	9.2/8.9
ED5	16.0	18.0	11.4/11.3	7.7/7.7
ED6	19.2	14.8	9.3/9.5	5.9/4.5
ED7	22.4	11.6	-/5.1	-/4.5

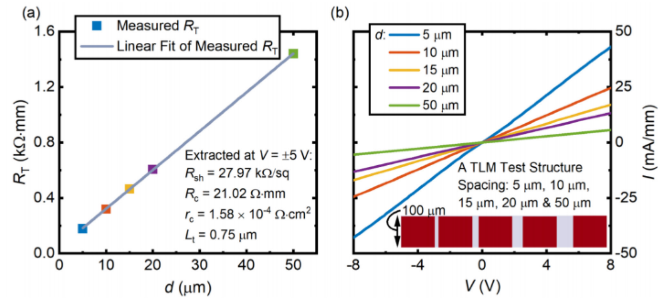

FIGURE 3. TLM measurement results of the annealed Ni/Au p-type ohmic contacts (sample ED0): a) a linear fit of normalized total resistance (R_T) against contact spacing (d) along with extracted characteristics: sheet resistance (R_{sh}), specific contact resistivity (r_c), normalized contact resistance (R_C) and transfer length (L_t) and b) corresponding I-V characteristics for varying *d*. A schematic TLM test structure is shown as inset.

for annealed Ni/Au metal stacks [7]. Fig. 3 (b) shows the I-V curves of the ohmic contacts measured at different spacing d which demonstrate linear ohmic characteristics.

After removal of the p-GaN and recess of the GaN channel, ohmic behavior is maintained (not shown here), however the contact resistance increases steadily with reduced GaN channel thickness between the TLM contacts. This is most likely caused by a modified potential distribution and current crowding at the contact edges with increasing sheet resistance of the channel layer. A growing specific contact resistance extracted by TLM up to the $\sim1\times10^{-3}$ Ωcm^2 range is observed, which is still sufficiently low for good device operation.

The impact of the (remaining) total GaN thickness t_{GaN} including the p-doped contact layer, on the electrical properties of the 2DHG is investigated in detail using Hall measurements (Fig. 4) and is compared to theoretical expectations. The measured hole concentration decreases almost linearly with reciprocal thickness $1/t_{GaN}$. This is in good agreement with theory, which – assuming a uid-GaN channel on the AlGaN buffer layer – to a first approximation predicts that the hole concentration in the 2DHG p_{2DHG} depends on the GaN thickness t_{GaN} according to [41]:

$$p_{\mathrm{2DHG}} \approx \frac{\sigma_{\mathrm{int}}}{q} - \frac{\varphi_s \cdot \varepsilon_0 \varepsilon_{GaN}}{q \cdot t_{\mathrm{GaN}}} \quad (1)$$

Here σ_{int} is given by the polarization difference between GaN and the AlGaN buffer, ε_{GaN} is the relative permittivity of GaN [41] and φ_s represents the surface potential as

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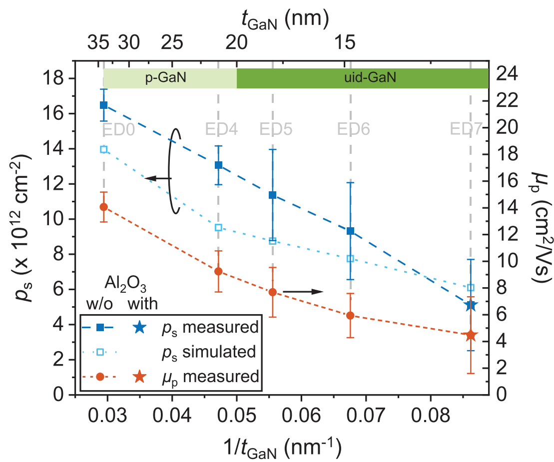

FIGURE 4. Average 2DHG densities p_S and mobility μ_p determined by Hall measurements for ED0 – ED7 with varying etching depth D_{etch}, i.e., GaN thickness t_{GaN}, measured before the Al_2O_3 dielectric deposition. Sample ED7 (star symbols) was measured after Al_2O_3 deposition. Note: Nominally, p-GaN is completely removed for $t_{GaN} \leq 20$ nm. The average values and error bars are based on at least 4 measurements per sample.

the difference between valence band and Fermi level at the GaN surface. In addition, we have calculated the expected carrier concentration using Sentaurus TCAD [15] and the structure shown in Fig. 1(a). We have employed the given material parameters, and only modified the valence band offset according to [21] by adjusting the electron affinity of AlGaN. The surface potential was set to $\varphi_s = 1.6$ eV [17], and the relaxation of the GaN channel was also taken into account.

The measured carrier concentration values are quite close to the theoretical prediction. However, in the region of the uid-GaN, the slope with thickness is distinctly different from theoretically expected, and the values of p_s are systematically higher than the calculated ones (with exception of the thinnest sample). We believe that this is indicative of Mg that has diffused from p-GaN into the uid-GaN channel and results in a systematic increase of carrier concentration. Our previous growth and characterization study [45], which discussed similar heterostructures as the ones presented here, also yielded systematically larger carrier concentrations than expected for a uid-GaN channel. The measured 2DHG Hall mobility decreases steadily from 14.1 cm^2/Vs for the non-recessed sample ED0 (t_{GaN} = 34 nm) to 4.5 cm^2/Vs for sample ED7 (t_{GaN} = 11.6 nm). The trend of lower mobility with lower carrier concentration is opposite to the behavior observed in the past [5]. Therefore, in the present case, accumulated etch damage with extended etch time appears to be a likely origin of the mobility reduction observed here. On the other hand, reduction of mobility with lower carrier concentration due to less screening of ionized impurities and delocalization of the 2DHG might also play a role.

B. DC DEVICE CHARACTERISTICS

The transfer and output characteristics of transistors fabricated on samples ED4 to ED7 are shown in Fig. 5 and

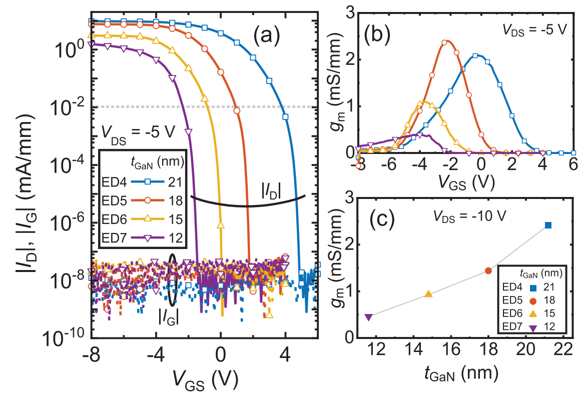

FIGURE 5. DC performance of p-channel MISHFET with varying t_{GaN}: (a) Transfer characteristics in semi-log scale at $V_{DS} = -5$ V, the dotted line indicates the current at which V_{th} was determined. (b) Transconductance profile at $V_{DS} = -5$ V and (c) maximum transconductance extracted from the output characteristics in Fig. 6.

Fig. 6, respectively, demonstrating transistor operation with excellent DC performance. The transfer characteristics of MISHFET processed on samples ED4 to ED7 were recorded at $V_{DS} = -5$ V by sweeping V_{GS} from positive to negative values ("to"-sweep). The output characteristics were measured starting in the off-state and stepwise turning the transistors into accumulation. The current levels correlate with the carrier concentrations determined by Hall (s. Fig. 4), reaching maximum levels of ~10 mA/mm for sample ED4 with largest value of t_{GaN} (21 nm). In general, the maximum current is limited for all samples by the low hole mobility which dominates the operation of our long gate-length devices. For comparison, a 100× higher mobility value (comparable to a typical electron mobility) would result in current levels in the same range as found for n-channel devices of similar dimensions. This and the additionally high access resistance values are also affecting the extrinsic transconductance values, which are drastically reduced with lower GaN thickness (Fig. 5 (b)). The g_m profiles are also skewed by the fact that the devices have not reached full saturation at $V_{DS} = -5$ V. Nevertheless, maximum g_m values estimated in saturation from the output characteristics (cf. Fig. 6) clearly confirm this trend (Fig. 5 (c)).

The threshold voltages V_{th}, extracted from pristine devices at a drain current of $|I_D| = 10^{-2}$ mA/mm, shift with decreasing t_{GaN} in negative V_{GS} direction (Fig. 5 and 7). For shallow etching, samples ED4 and ED5 with t_{GaN} of 21 and 18 nm show d-mode operation with V_{th} of +3.8 V and +0.9 V. As the etching depth increases, we observe e-mode behavior for samples ED6 and ED7, with V_{th} of −0.8 V and −2.3 V, respectively. Note: When correlating the threshold voltage of the fabricated devices with the 2DHG density determined by Hall measurements, we have to consider that these measurements were performed on ungated structures. In the case of the transistors, Mo used as low-work function gate metal most likely enhances the barrier height resulting in an additional depletion of the 2DHG and rendering the thin-channel devices normally-off. On the other hand, one also may want

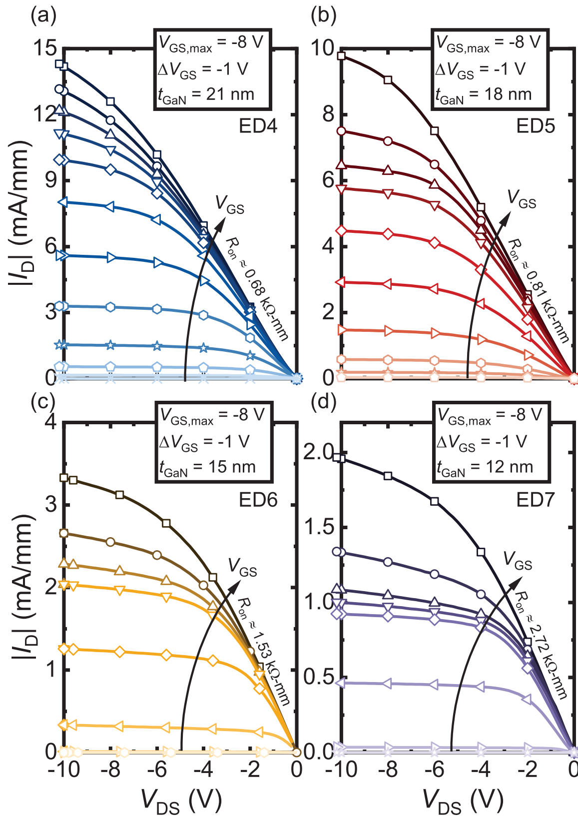

FIGURE 6. **DC output characteristics of p-channel MISHFET based on GaN/$Al_{0.29}Ga_{0.71}N$ with varying t_{GaN}.**

to consider the impact of the (unintended) Mg doping on the threshold voltage. An exact calculation requires knowing the precise Mg doping concentration and profile. A simple estimate can be performed though, considering an additional sheet charge density of $p_{s_extra} = 2 \cdot 10^{12} cm^{-2}$ in agreement with the extra charge seen in Figure 4 and also consistent with the data from [45]. This estimate predicts a shift of V_{th} in *positive* direction by 0.4 - 0.6 V, depending on the thickness of the channel in the range between 12ñm and 20ñm.

Due to the effective insulation provided by the Al_2O_3 gate dielectric, all devices (ED4 – ED7) reach low off-state current values $|I_{D,off}|$ in the range of $\sim 10^{-8}$ mA/mm, independent of the etching depth. Therefore, an excellent current on/off ratio of $\sim 10^8$ is achieved and a steep subthreshold swing (SS) is obtained for all devices, which is between 80 mV/dec (ED4) and 89 mV/dec (ED7). These values, which are close to the theoretical limit of SS at room temperature, are attributed to the good quality of the highly resistive AlGaN buffer layer and the GaN/AlGaN interface. However, hysteresis and other trap-related effects are observed, as will be discussed further below. In contrast to many other publications on p-channel devices [3], [5], [10], [12], [13], [14], [16], [21], [23], [25], [48], [49], no non-linear turn-on behavior is observed in the output characteristics of all fabricated p-channel MISHFET in Fig. 6 as a result of the linear and low-resistive ohmic contacts.

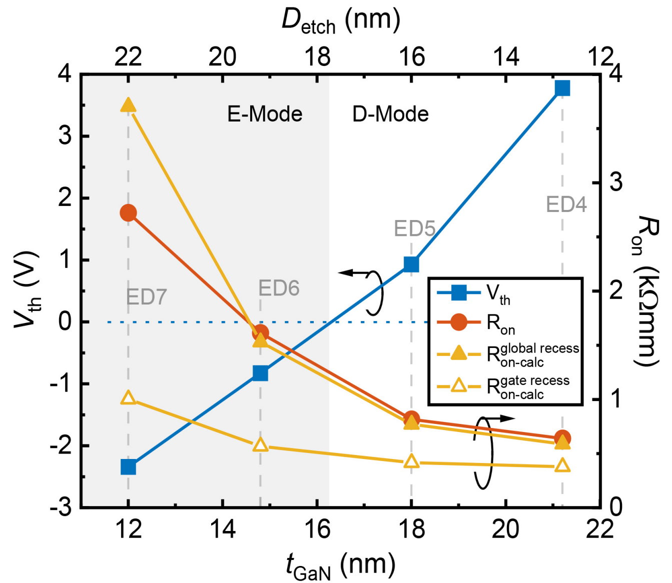

FIGURE 7. **Comparison of extracted V_{th} (squares) and R_{on} (circles) of p-channel MISHFETs in dependence of t_{GaN}. $R_{on-calc}^{global\ recess}$ (filled triangles) and $R_{on-calc}^{gate\ recess}$ (open triangles) represent the on-resistance estimated from the measured contact and sheet resistances for the recess of the complete source-drain region and assuming a gate recess only.**

Fig. 7 shows the on-resistance R_{on} extracted at $V_{DS} = -5$ V plotted as a function of the GaN layer thickness t_{GaN}. Included is also the calculated on-resistance for each sample, derived from $R_{on-calc} = 2 \cdot R_c + L_{DS} \cdot R_{Sh}$, the contact resistance R_c measured by TLM and sheet resistance R_{Sh} obtained by Hall measurements.

Etching the complete source-drain region not only shifts the threshold voltage from positive to negative values, but increases the on-resistance as a result of decreasing 2DHG density in the access regions as well. The clear trade-off between R_{on} and V_{th} visible in Fig. 7 might only be avoided if the (p-)GaN recess is limited to the gate region. This can be visualized when we estimate the on-resistance by utilizing the measured contact and sheet resistances determined by TLM. For comparison, the total resistance $R_{on-calc}^{global\ recess}$ for the complete gate-drain region is also shown, which is in excellent agreement with R_{on} extracted from the output characteristics. We conclude that an on-resistance ($R_{on-calc}^{gate\ recess}$ in Fig. 7) *below* 1 $k\Omega \cdot mm$ could be achieved even for normally-off devices. On the downside, such an approach may lead to higher off-state leakage currents and degraded three-terminal breakdown characteristics.

C. INVESTIGATION OF DIELECTRIC/SEMICONDUCTOR TRAPS

Charge trapping at a dielectric/semiconductor interface is known to cause hysteresis in I-V and C-V characteristics, often summarized as V_{th} *instability* in GaN-based n-channel and p-channel transistors [19], [30], [31]. A gate dielectric such as Al_2O_3 between the gate metal and the AlGaN barrier or GaN channel layer can result in a high density of

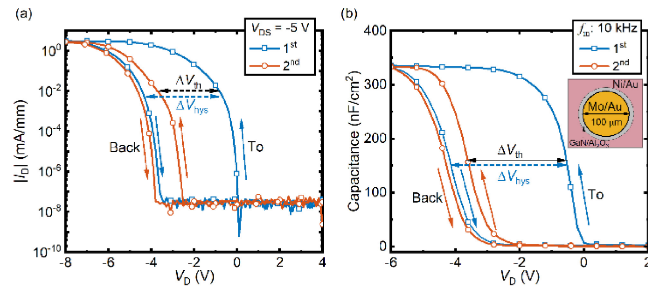

FIGURE 8. a) Dual-sweep transfer curves of fabricated e-mode p-channel MISHFET ED6 and b) dual-sweep C-V profiles of a MIS diode on sample ED6 at the first and second measurement, measurement frequency (f_m) of 10 kHz. A schematic top-view of a large-area diode with a diameter of 100 μm is shown in the inset.

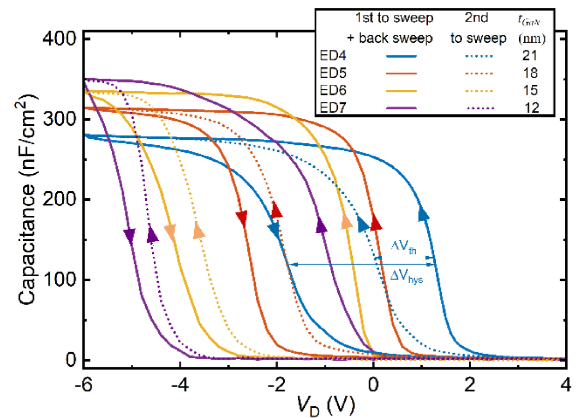

FIGURE 9. C-V measurements of large-area MIS diodes at $f = 10$ kHz recorded with a sweep rate of $\sim$ 1 V/s. Hysteresis width and threshold voltage shift are indicated in the figure.

states at the Al_2O_3/semiconductor interface. Depending on their energetic location, these states can either be charged or discharged over the course of a measurement cycle or are "frozen" in a state depending on the biasing history.

The p-channel devices presented here are also revealing several instabilities which may be directly related to dielectric/semiconductor charges. First, a close investigation of the output characteristics already discussed in Fig. 6, show an anomalous "bunching" of the I-V curves recorded in the gate voltage range of $V_{GS} = -4 \ \ldots -6\ V$. This behaviour is most predominant for ED7 and ED6, the devices with smallest channel charge, but visible for the other samples as well. The reduction of the transconductance for large accumulating gate biases is a known effect for compound semiconductor transistors, usually associated to, i.e., reduced modulation efficiency [32], velocity saturation [33] or parasitic MESFET formation [34]. However, as is clearly seen in Fig. 6, for gate biases more negative than $V_{GS} =\sim -6\ V$, the curves are increasingly separated, hence a larger transconductance is apparent. One would expect a transconductance profile measured at sufficiently large drain bias to yield two distinct maxima. However, we found *no stable biasing sequence* to reliably record this behavior while measuring the transfer curves. On the other hand, the "bunching" of the IV curves in output characteristics was quite well observable across all devices and samples. It appears that for a limited range of intermediate gate biases, some channel charge is "lost", possibly by capture in interface states.

To investigate the interface trapping effects, we have analyzed transistor dual-sweep transfer curves and dual-sweep C-V curves of large-area metal-insulator-semiconductor (MIS) diodes fabricated on the same samples.

In Fig. 8 (a), transfer characteristic measurements of sample ED6 are shown, with V_{GS} swept from +4 V to −8 V (to-sweep) and then from −8 V back to +4 V (back-sweep). The first transfer curve measurement (blue in Fig. 8 (a)) exhibits a large hysteresis width ΔV_{hys} of around 3.7 V. The second dual-sweep transfer curve recorded approx. 1 minute after the first one (red) shows a significantly reduced hysteresis ΔV_{hys} of 0.8 V, resulting in a threshold voltage shift between the two measurements of $\Delta V_{th} = 2.9$ V (extracted from the to-sweeps). It is notable that the back-sweeps of the two consecutive measurements are almost identical. Such behavior is similar to what has been reported in [19] for p-channel transistors and in [21] for n-channel devices. In accumulation (here at negative biases), interface states can capture free holes from the 2DHG channel. The threshold voltage shift between two consecutive sweeps is caused by deep traps which apparently do not have sufficient time to discharge before the second measurement is started. Shallow levels can release their trapped holes already during the back-sweep, resulting in the smaller hysteresis for the subsequent measurements.

This described behavior is not only visible in the MISHFET transfer characteristics, but can also be detected in C-V measurements performed on MIS diodes with a diameter of 100 μm, shown in Fig. 8 (b). V_{th} of our MIS diodes as well as hysteresis width ΔV_{hys} have been determined at those bias values V_D for which the measured capacitance equals $C_{max}/2$ (found at $V_D = -6$ V). The hysteresis width and the threshold voltage determined by C-V measurements are quite comparable to the values found for the transfer curves.

C-V measurement results for the samples with different GaN channel thickness are displayed in Fig. 9, displaying for each the first and second measurement recorded with a sweep rate of $\sim$ 1 V/s. For clarity, only *the first* back-sweep is shown for each sample, as the back-sweeps are almost identical for successive measurements (see Fig. 8 for comparison). The maximum bias in accumulation was limited to $V_D = -6$ V, larger values lead to destructive breakdown of the Al_2O_3 dielectric.

The *total density* of charge trapped at the interface $N_{trap,tot}$ correlates directly with the hysteresis width ΔV_{hys} between to- and back-sweeps. The threshold voltage shift ΔV_{th} between two consecutive to-sweeps on the other hand is related to the *deep traps* $N_{trap,d}$ at the dielectric/semiconductor interface, which *do not discharge* between the two consecutive measurements (the second measurement was repeated within 1 minute after the first). As a result, the

TABLE 2. Summary of values extracted from C-V measurements. Remaining GaN thickness t_{GaN} calculated from C-V measurements. Calculated ΔV_{th} and ΔV_{hys} as well as associated trap densities $N_{trap,d}$ and $N_{trap,tot}$.

Sample	t_{GaN} (nm)	ΔV_{th} (V)	$N_{trap,d}$ (x10^{12} cm^{-2})	ΔV_{hys} (V)	$N_{trap,tot}$ (x10^{13} cm^{-2})
ED4	21.0	1.3	5.6	3.1	1.53
ED5	17.5	2.0	8.8	2.7	1.33
ED6	15.8	3.1	13.6	3.7	1.82
ED7	14.6	3.5	15.6	4.0	1.97

difference between $N_{trap,tot}$ and $N_{trap,d}$ represents an estimate of the concentration of shallow traps, which are discharged between two consecutive measurements under our specific conditions.

From ΔV_{th} and ΔV_{hys}, we can estimate the corresponding density of deep traps $N_{trap,d}$ and the total trap density $N_{trap,tot}$ (assuming that all trapped charges are located at the Al_2O_3/GaN interface) by using the following expression [21]:

$$N_{trap} = \frac{C_{ins}\Delta V}{q} = \frac{\varepsilon_{ins}\Delta V}{q \cdot t_{ins}} \tag{2}$$

where ε_{ins} represents the dielectric constant of the dielectric layer and t_{ins} its thickness. The results are summarized in Table 2. It is remarkable that the values for the hysteresis width ΔV_{hys} are very similar, and consequently the estimated total trap density $N_{trap,tot}$ lies in a very narrow range from $1.3 - 2.0 \times 10^{13}\text{cm}^{-2}$ for all the investigated samples. Given that the interfaces of the samples have been exposed to the same process (dry etch and Al_2O_3 deposition), this conclusion appears plausible. On the other hand, we see that the threshold voltage shift ΔV_{th} and the corresponding deep trap density $N_{trap,d}$ are increasing quite systematically with reduced GaN thickness. A plausible explanation for this behavior could be accumulated etch damage with extended etch depth, resulting in an increased density of deep-level defects. This hypothesis is also consistent with the previously mentioned mobility degradation observed with rising recess etch depth.

From the capacitance in accumulation (at $V_{GS} = -6$ V), we can also estimate the effective thickness of the GaN channel by calculating the channel capacitance $C_{ch} = (C_{ox} \cdot C_{meas})/(C_{ox} - C_{meas})$, with measured total capacitance C_{meas} and the oxide capacitance C_{ox}. The GaN channel thicknesses were calculated using the dielectric constants of GaN ($\varepsilon_{GaN} = 10.3$ [25]) and Al_2O_3 ($\varepsilon_{Al_2O_3} = 8.9$ [26]) and the nominal thickness of the dielectric layer ($t_{Al_2O_3} = 10$ nm) and are summarized in Table 2. The values are in reasonable agreement with our estimate from the etch rate mentioned before (s. Tab. 1).

Finally, it is worth recalling that the accumulation-bias C-V curve of n-channel AlGaN/GaN MISHFET usually shows a second plateau associated with the capacitance of the dielectric layer [21]. This is due to the large number of carriers which overcome the AlGaN barrier. In our devices, such a second plateau could not be found and the fairly constant capacitance in accumulation also indicates that there is no flooding of the interface with free carriers at negative gate bias. As mentioned, accumulation bias was limited by the breakdown of the Al_2O_3 dielectric. Nevertheless, the missing barrier between 2DHG and interface enables charge transfer to and from the interface, potentially leading to severe transient effects.

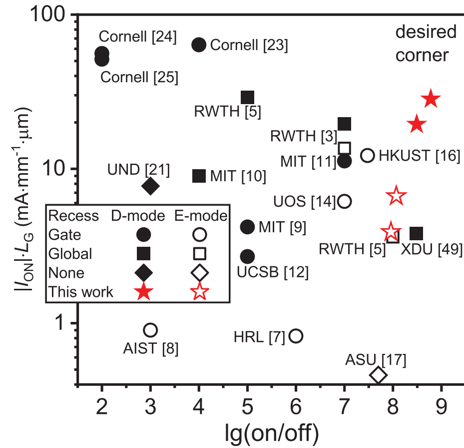

FIGURE 10. Benchmark of III-nitride p-channel HFET highlighting on-current·gate-length product vs. on/off ratio.

IV. CONCLUSION

In conclusion, we have examined the DC characteristics of p-channel MISHFET using strained p-GaN/uid-GaN on (almost) relaxed $Al_{0.29}Ga_{0.71}N$ buffers. By adjusting the channel thickness, we can shift the device characteristics from depletion- to enhancement-mode. The devices yield excellent on/off ratios and subthreshold swings SS for all channel thicknesses investigated here, demonstrating the good quality of the epitaxial material. Both e-mode and d-mode devices exhibit state-of-the-art on-current·gate-length products, placing them among the best performing transistors as shown in Fig. 10.

Nevertheless, severe hysteresis and V_{th} instability have been observed, as revealed by dual sweep I-V and C-V measurements. More detailed analyses and further process developments are necessary to elucidate how these effects can be minimized. Selective-area growth of p-GaN contact layers may help to avoid surface damage related to dry etching and to avoid Mg diffusion into the uid-GaN channel. Still, the unhindered charge transfer from 2DHG channel to the dielectric/GaN interface may prove to be a serious challenge.

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