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Monolithic Dual-Gate E-Mode Device-Based NAND Logic Block for GaN MIS-HEMTs IC Platform

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ABSTRACT In this work, dual-gate enhancement-mode (E-mode) device based NAND circuit (DG-NAND) and the NAND block with double E-mode devices (DD-NAND) are developed and fabricated based on the GaN MIS-HEMTs (metal-insulator-semiconductor-high-electron-mobility-transistors) platform. The DG-NAND circuit has an area of 0.118 mm^2 with the probe pad, which is 24% lower than the area of the DD-NAND circuit. Both static and dynamic experimental results validate the advantages of performance improvement of NAND circuits designed by dual-gate technology at an input voltage of 9 V. This paper demonstrates the design potential of dual-gate NAND in an all-GaN MIS-HEMTs platform through compact design.

INDEX TERMS Logic circuits, GaN, MIS-HEMTs, dual-gate E-mode device, monolithic integration.

I. INTRODUCTION

AlGaN/GaN HEMTs become a promising candidate for power converter switches in recent years due to high switching frequency, power density, and conversion efficiency [1], [2], [3], [4]. Stray inductances and commutation loops are the main factors that limit the switching speed of GaN-based power electronics with discrete driver chips [5]. The lateral structure of the GaN-on-Si technology allows the monolithic integration of several devices for a compact design to restrain parasitic effects [6].

For GaN devices, the dual-gate technology could be applied to realize the unique function and reduce requirements on the extra component [7], [8], [9], [10]. With the back gate technology, Hazra et al. [8] proposed a dual-gate structure to control the threshold voltage. A cascade dual-gate structure is proposed by Lin et al. to suppress current collapse [11]. Gong et al. [12] reported a normally-on dual-gate AlGaN/GaN MIS (metal-insulator-semiconductor) HEMTs (high-electron-mobility-transistors) with Al_2O_3 gate oxide layer, which showed a lower reverse gate leakage current than its normally-on dual-gate Schottky HFET, while the gate insulators are also used to enhance the gate swing [13], [14], [15]. However, all the above applications are examined with depletion-mode (D-mode) devices. Since D-mode HEMT technology requires a negative voltage control, its counterpart, the enhancement-mode (E-mode) HEMT, is more suitable for the power conversion application [16], [17]. Wolf et al. [18] fabricated a monolithically integrated bidirectional switch based on E-mode p-GaN HFETs using dual-gate technology.

For a high-level integrated power system, dual-gate technology is a feasible solution for monolithic design [19]. Chvála et al. demonstrated a monolithic NAND cell that is based on InAlN/GaN MIS-HEMTs with a maximum gate voltage of 3 V, and confirming the validity of the proposed models [20]. As an essential building block for

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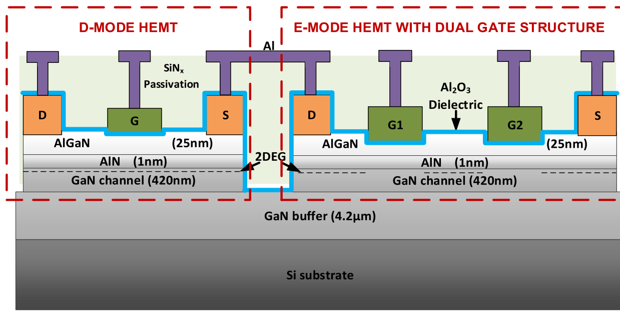

FIGURE 1. Schematic cross-section of the AlGaN/GaN MIS-HEMT DG-NAND logic circuit.

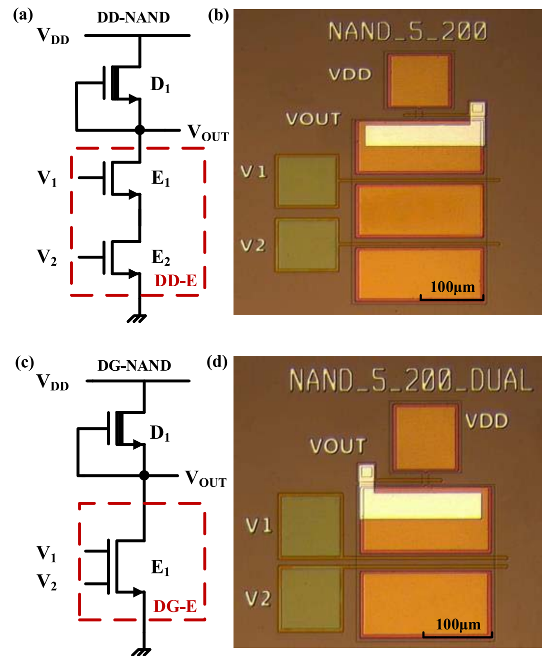

FIGURE 2. DD-NAND logic circuit: (a) schematic of the logic circuit, (b) microscope photo (E-mode device dimension: $L_{GS}/L_G/L_{GD}/W_G$ = 5/3/10/200 μm). DG-NAND logic circuit: (c) circuit diagram, (d) microscope view.

digital circuits, implementing dual-gate E-mode NAND (DG-NAND) by p-GaN HEMTs with a smaller area provides an optimization method [21]. However, as a result of the limitations of p-GaN technology with low gate breakdown voltage, the gate driver voltage is limited to 5 V, which requires extra protection circuits for an all-GaN integrated circuit (IC) development. Moreover, the dynamic test is necessary to analyze the superior characteristics of the dual-gate design.

In this work, we demonstrate double E-mode devices NAND (DD-NAND) and dual-gate E-mode device NAND logic gate circuits by monolithic integrated E/D mode MIS-HEMTs. The static and dynamic measurements are conducted to evaluate the performance of the logic gate. The experimental investigation is reported about the compact solution to logic blocks for power IC applications.

II. EXPERIMENTS AND DISCUSSION

Fig. 1 depicts a schematic cross-section of the proposed DG-NAND circuit by utilizing the AlGaN/GaN MIS-HEMTs technology. All devices are fabricated on a Si substrate consisting of a 4.2 μm GaN buffer layer, a 420 nm layer GaN channel layer, a 1 nm AlN spacer and a 25 nm AlGaN layer. GaN devices with D-mode and E-mode are capable of forming logic circuits by Direct Coupled FET Logic (DCFL) structure [22], [23]. For E-mode devices, recessed-gate technology has been utilized [24], and MIS gates have been implemented to extend the swing voltage of the gate and thus improve performance [25]. An interconnect layer of Al is deposited to allow the integration of monolithic integrated circuits. An in-depth description of the fabrication process is provided in [26]. The D-mode device features a 5 μm source to gate distance (L_{GS}), a 3 μm gate length (L_G), a 5 μm gate width (W_G), and a 10 μm drain to gate distance (L_{GD}). For dual-gate E-mode device dimension, $L_{GS}/L_G/L_{GD}/W_G$ = 5/3/5/200 μm, and the separation between the two gates is set to 10 μm.

The schematic diagram of the GaN-based double device E-mode (DD-E) structure is illustrated in the red border, as shown in Fig. 2 (a) and reported in [19]. Unlike traditional NAND design uses two E-mode devices connected in series [27], the two E-mode devices share the common pad for the connection part to optimize the chip layout. The D-mode device functions as an active load resistor and two E-mode gates serve as logic input. In this work, the presented GaN-based dual-gate E-mode (DG-E) structure is used to replace the counterpart DD-E structure. Thus the DG-NAND logic circuit is formed, as shown in Fig. 2 (c). The employment of dual-gate devices aims to replace two E-mode HEMTs in the logic circuit design and eliminates redundant ohmic contacts [28], which could reduce on-state resistance and parasitic capacitance. The corresponding microscope views of the DD-NAND and DG-NAND circuits are shown in Fig. 2 (b) and Fig. 2 (d), respectively. The size of the layout with the probe pad reduces from 0.155 mm^2 to 0.118 mm^2 owing to the advantages of a dual-gate structure.

A. EXPERIMENTAL SETUP

The static test platform is illustrated in Fig. 3 (a), and the experimental setup is represented by the blue and black connection. A fixed DC bias voltage is provided to V_2. It is worth pointing out that DD-E structure measurements use V_1 and V_2 to regulate the switching states of the two E-mode devices. For DG-E device, V_1 and V_2 are utilized to control the G_1 and G_2 gates of the dual-gate E-mode device, as shown in Fig. 3 (a) left part. Meanwhile, the static performance of the NAND circuits is monitored by the same analyzer, the supply voltage V_{DD} is provided. The dynamic experimental setup is represented by the red and black arrows in Fig. 3 (a). Two input signals V_1 and V_2 are supplied by

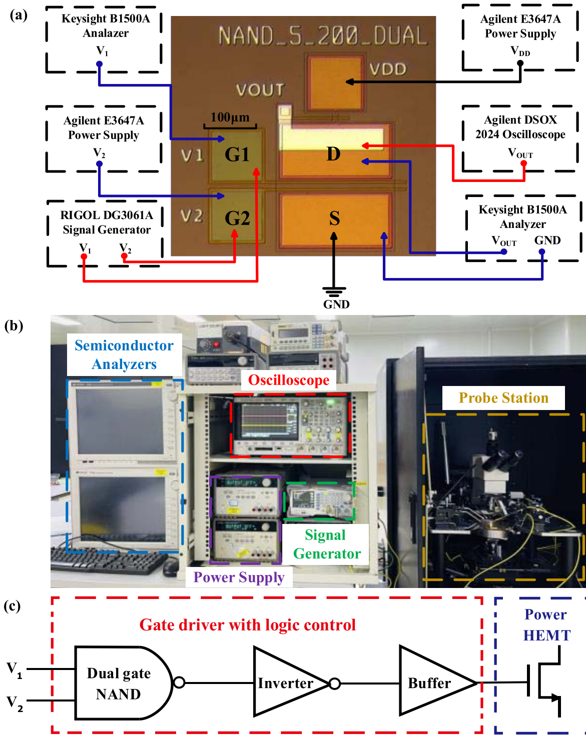

FIGURE 3. (a) The experimental setup diagram of the DG-NAND logic circuit for static (blue and black line) and dynamic measurement (red and black line), (b) test setup, (c) monolithic integrated GaN driver with DG-NAND circuit.

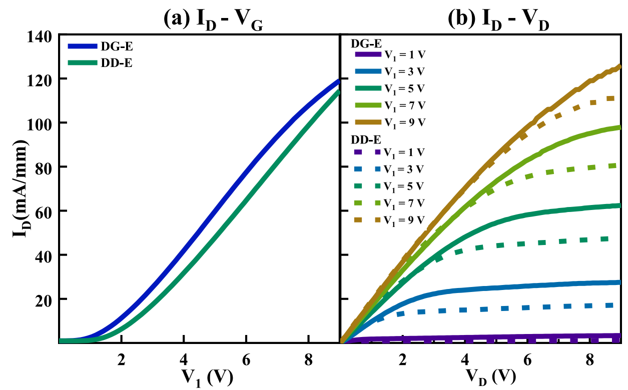

FIGURE 4. Comparison of DD-E structure and DG- E device at V_2 is biased at constant 9 V: (a) Transfer characteristics, (b) output characteristics.

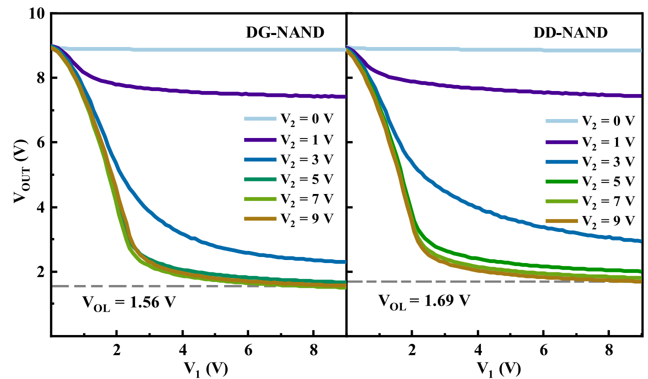

FIGURE 5. Comparison between measured voltage transfer characteristics of the DG-NAND and DD-NAND logic circuits.

a signal generator, and they are set to output different logic levels. The dynamic performance of the NAND logic circuit is monitored and recorded by an oscilloscope. The test setup is demonstrated in Fig. 3 (b). Fig. 3 (c) shows an integration of the logic unit into the pre-drive module [13], in which the dual-gate NAND circuit could be utilized to replace the first-level DCFL inverter in the driver stage. This method would contribute to the high integration level all-GaN power conversion system.

B. STATIC CHARACTERISTICS MEASUREMENT FOR DD-E STRUCTURE AND DG-E DEVICE

The characteristics of the devices and the NAND circuits were measured by an Agilent B1505A power device analyzer. As illustrated in Fig. 4 (a), the threshold voltage (V_{th}) of the DD-E structure is 1.9 V, and the V_{th} of the DG-E device is 1.7 V. Fig. 4 (b) shows the I_D-V_D curve, the current density ($I_{D,\,max}$) is approaching 124.8 mA/mm when two gates are biased at 9 V for DD-E structure. As could be observed in Fig. 4 (b), the current density of the DG-E structure reaches a peak value of 133.9 mA/mm.

C. STATIC AND DYNAMIC CHARACTERISTICS MEASUREMENT FOR GAN-BASED TWO-INPUT NAND LOGIC CIRCUIT

In all-GaN monolithic IC design, the logic circuit serves as the drive control module applied to modify the drive voltage based on the feedback signal [29]. The voltage transfer characteristics (VTC) of the investigated DG-NAND circuit are demonstrated in Fig. 5, and it is compared with the VTC of the DD-NAND circuit. A supply voltage V_{DD} of 9 V is applied. The minimum output voltage (V_{OL}) of the DD-NAND circuit is about 1.69 V, and V_{OL} of the DG-NAND circuit is nearly 1.56 V. Meanwhile, the output voltage of 9 V are obtained in Fig. 5 at $V_1 = 0$ V.

The NAND dynamic test is used to emulate different operating conditions on an all-GaN integrated power chip. Logic circuits are designed to generate a drive signal based on the input operating signal (V_1) and enable signal (V_2) as shown in Fig. 3 (c). Different output states could be observed in the output waveforms by adjusting the phase between the input operating signal and enable signal. In Fig. 6, the voltage output waveforms of the DG-NAND and DD-NAND logic circuits working at 100 kHz are monitored by the oscilloscope. The black and red curves represent the gate voltages applied on the first gate and the second gate, respectively, from signal generators. When the DD-NAND circuit and DG-NAND circuit work at a switching frequency of 100 kHz, the falling time of the DG-NAND circuit is 15 percent shorter than the DD-NAND circuit.

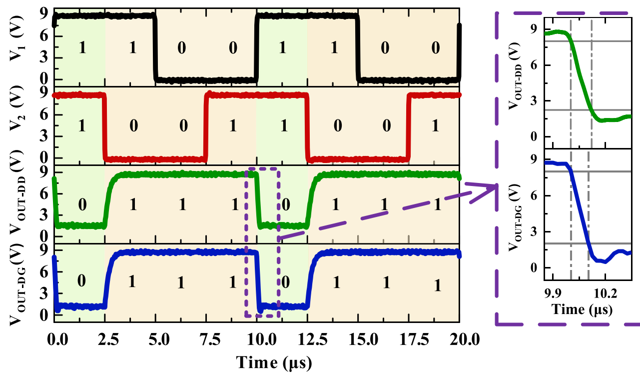

FIGURE 6. Measured output voltage waveforms of the DD-NAND (green line) and DG-NAND (blue line) logic circuits.

TABLE 1. Comparison for GaN-based dual-gate device.

Ref	Method	TYPE	V_g（V）	Application
[8]	HEMT	D-mode	-5 to 5	Back gate for boosting the threshold voltage
[10]	HEMT	D-mode	-8 to 2	Study of current collapse behaviors
[12]	MIS-HEMT	D-mode	-5 to 0	Power device
[18]	p-GaN HFET	E-mode	0 to 5	Normally off Bidirectional switches
[30]	p-GaN GIT	E-mode	0 to 5	GaN-based monolithic bidirectional switch
[20]	InAlN/GaN MIS-HEMT	E-mode	0 to 3	Monolithic NAND logic cell
[21]	p-GaN HEMT	E-mode	0 to 5	Monolithic NAND logic cell
This work	**MIS-HEMT**	**E-mode**	**0 to 9**	**Monolithic NAND logic block**

Table 1 compares the dual gate technology for different applications. References [8], [10], and [12] apply a second gate in the D-mode to improve device performance. Papers [18] and [30] uses a second gate to complete the design of a bidirectional device. Both papers [20] and [21] utilize a dual-gate structure for the functional block of the monolithic integrated GaN platform. Verifying the dynamic performance and comparing it with the conventional design is necessary. In this paper, a logic circuit module for the GaN MIS-HEMTs platform is designed based on DG-E device and compared with the conventional design of the DD-E structure through dynamic and static tests. Furthermore, this design also exploits the advantages of the MIS-HEMTs platform. The large gate swing lowers the demand for gate voltage protection, resulting in a compact design.

III. CONCLUSION

In this work, two types of AlGaN/GaN -based NAND logic circuits are demonstrated. Static and dynamic measurements experimentally validate the NAND logic circuit of both structures. The dual-gate E-mode device NAND logic cell utilizes fewer devices and the die area drops by 24%. Indicated parasitic parameters are also reduced due to the elimination of redundant ohmic contacts. The static characterization of the dual-gate E-mode device NAND circuit indicates a lower V_{OL} about 1.46 V. From the dynamic measurement results, the DG-NAND logic circuit observed less falling time, which decreased by 15%. Furthermore, the dual-gate NAND will be applied as a subunit of the drive unit development for compact design and functional integration of the all-GaN MIS-HEMTs IC platform.

REFERENCES

[1] D. Kinzer and S. Oliver, "Monolithic HV GaN power ICs: Performance and application," *IEEE Power Electron. Mag.*, vol. 3, no. 3, pp. 14–21, Sep. 2016, doi: 10.1109/MPEL.2016.2585474.
[2] R. Sun, Y. C. Liang, Y.-C. Yeo, C. Zhao, W. Chen, and B. Zhang, "All-GaN power integration: Devices to functional subcircuits and converter ICs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 31–41, Mar. 2020, doi: 10.1109/JESTPE.2019.2946418.
[3] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.
[4] C.-L. Tsai et al., "Smart GaN platform: Performance & challenges," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2017, pp. 1–4, doi: 10.1109/IEDM.2017.8268488.
[5] S. Moench et al., "Monolithic integrated quasi-normally-off gate driver and 600 V GaN-on-Si HEMT," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2015, pp. 92–97, doi: 10.1109/WiPDA.2015.7369264.
[6] D. Kinzer, "GaN power IC technology: Past, present, and future," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, 2017, pp. 19–24, doi: 10.23919/ISPSD.2017.7988981.
[7] J. S. Moon et al., "<70% power-added-efficiency dual-gate, cascode GaN HEMTs without harmonic tuning," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 272–275, Mar. 2016, doi: 10.1109/LED.2016.2520488.
[8] S. Hazra, A. A. Shuvo, and A. G. Bhuiyan, "Electrical characteristics of dual gate algan/gan high-electron mobility transistors," in *Proc. 5th Int. Conf. Electr. Inf. Commun. Technol. (EICT)*, 2021, pp. 1–4, doi: 10.1109/EICT54103.2021.9733454.
[9] B. Kim, H. Q. Tserng, and P. Saunier, "A GaAs dual gate power FET for operation up to K band," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1983, pp. 200–201, doi: 10.1109/ISSCC.1983.1156508.
[10] L. Shi, M. Liu, N. Dong, and X. Lin, "Dual-metal-gate AlGaN/GaN HEMTs for power application," in *Proc. 14th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, 2018, pp. 1–3, doi: 10.1109/ICSICT.2018.8565730.
[11] D.-J. Lin, J.-Y. Yang, C.-K. Chang, and J.-J. Huang, "Study of current collapse behaviors of dual-gate AlGaN/GaN HEMTs on Si," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 59–64, 2022, doi: 10.1109/JEDS.2021.3132429.
[12] R. Gong et al., "AlGaN/GaN dual gate MOS HFET for power device applications," in *Proc. 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, 2010, pp. 1353–1355, doi: 10.1109/ICSICT.2010.5667654.
[13] M. Cui et al., "Monolithic integration design of GaN-based power chip including gate driver for high-temperature DC–DC converters," *Jpn. J. Appl. Phys.*, vol. 58, no. 5, 2019, Art. no. 56505, doi: 10.7567/1347-4065/ab1313.
[14] A. Li et al., "A monolithically integrated 2-transistor voltage reference with a wide temperature range based on AlGaN/GaN technology," *IEEE Electron Device Lett.*, vol. 43, no. 3, pp. 362–365, Mar. 2022, doi: 10.1109/LED.2022.3146263.
[15] Y. Cai et al., "Low ON-state resistance normally-OFF AlGaN/GaN MIS-HEMTs with partially recessed gate and ZrO_x charge trapping layer," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4310–4316, Sep. 2021, doi: 10.1109/TED.2021.3100002.

[16] H. Amano et al., "The 2018 GaN power electronics roadmap," *J. Phys. D, Appl. Phys.*, vol. 51, no. 16, Mar. 2018, Art. no. 163001, doi: 10.1088/1361-6463/aaaf9d.

[17] M. Giandalia, J. Zhang, and T. Ribarich, "650 V AllGaN^{TM} power IC for power supply applications," in *Proc. IEEE 4th Workshop Wide Bandgap Power Device Appl. (WiPDA)*, 2016, pp. 220–222, doi: 10.1109/WiPDA.2016.7799941.

[18] M. Wolf, O. Hilt, and J. Würfl, "Gate control scheme of monolithically integrated normally OFF bidirectional 600-V GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3878–3883, Sep. 2018, doi: 10.1109/TED.2018.2857848.

[19] Y. Zhu, M. Cui, A. Li, F. Li, H. Wen, and W. Liu, "Monolithic DFF-NAND and DFF-NOR logic circuits based on GaN MIS-HEMT," in *Proc. Int. Conf. IC Des. Technol. (ICICDT)*, 2021, pp. 1–4, doi: 10.1109/ICICDT51558.2021.9626401.

[20] A. Chvála et al., "Device and circuit models of InAlN/GaN D- and dual-gate E-mode HEMTs for design and characterisation of monolithic NAND logic cell," in *Proc. 13th Int. Conf. Des. Technol. Integr. Syst. Nanoscale Era (DTIS)*, 2018, pp. 1–6, doi: 10.1109/DTIS.2018.8368565.

[21] M. Basler et al., "Building blocks for GaN power integration," *IEEE Access*, vol. 9, pp. 163122–163137, 2021, doi: 10.1109/ACCESS.2021.3132667.

[22] M. D. Feuer et al., "Direct-coupled FET logic circuits on InP," *IEEE Electron Device Lett.*, vol. 12, no. 3, pp. 98–100, Mar. 1991, doi: 10.1109/55.75724.

[23] G. Tang et al., "Digital integrated circuits on an E-mode GaN power HEMT platform," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1282–1285, Sep. 2017, doi: 10.1109/LED.2017.2725908.

[24] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-Voltage AlGaN/GaN HEMT for power electronics applications," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 356–362, Feb. 2006, doi: 10.1109/TED.2005.862708.

[25] R. Sun, Y. C. Liang, Y.-C. Yeo, and C. Zhao, "Au-free AlGaN/GaN MIS-HEMTs with embedded current sensing structure for power switching applications," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3515–3518, Aug. 2017, doi: 10.1109/TED.2017.2717934.

[26] M. Cui et al., "Monolithic GaN half-bridge stages with integrated gate drivers for high temperature DC–DC buck converters," *IEEE Access*, vol. 7, pp. 184375–184384, 2019, doi: 10.1109/ACCESS.2019.2958059.

[27] X. Li et al., "GaN-on-SOI: Monolithically integrated all-GaN ICs for power conversion," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2019, pp. 1–4, doi: 10.1109/IEDM19573.2019.8993572.

[28] Z. Hu, S. Zhou, R. He, and Q. Zhang, "A broadband voltage variable attenuator with high-power tolerance and compact size based on dual-gate GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6108–6115, May 2023, doi: 10.1109/TPEL.2023.3242474.

[29] H. Xu, G. Tang, J. Wei, and K. J. Chen, "Integrated high-speed over-current protection circuit for GaN power transistors," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2019, pp. 275–278, doi: 10.1109/ISPSD.2019.8757685.

[30] T. Morita et al., "650 V 3.1 mΩcm2 GaN-based monolithic bidirectional switch using normally-off gate injection transistor," in *Proc. IEEE Int. Electron Devices Meeting*, 2007, pp. 865–868, doi: 10.1109/IEDM.2007.4419086.