Received 13 January 2023; accepted 25 March 2023. Date of publication 10 April 2023; date of current version 6 December 2023.
The review of this article was arranged by Editor F. J. Guarin.

Digital Object Identifier 10.1109/JEDS.2023.3265663

n-MOS Transistor Impact Ionization Boosted by Cumulative Stress Degradation in a 250-nm SiGe BiCMOS Technology

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This work was supported in part by the Mexico National Council for Science and Technology (Conacyt).

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ABSTRACT We introduce experimental observations of impact ionization in an n-type MOSFET of a 250 nm SiGe BiCMOS technology when operated under an aging test setup at room temperature. As expected, the electrical basic parameters of the transistor, such as drain current drivability, transconductance, and threshold voltage degrades following a power law. However, impact ionization measured as bulk current enhances as degradation evolves with stress time. Through numerical simulations we prove that impaction ionization gets boosted because an enhancement of the longitudinal electric field peak at the drain side, where most of the hot carriers are generated.

INDEX TERMS nMOSFET, reliability, impact ionization, hot carriers.

I. INTRODUCTION

Today SiGe BiCMOS technologies are in general used for high-speed digital data communications systems, automotive radar, radio systems, and some analog circuits, where they share market with CMOS technologies [1]. On the other hand, CMOS-based transceivers, operating in the mm-wave band, are a low-cost available approach [2], but they are limited by the output power, which reduces the radio system range. Despite the unceasing advancement of CMOS technologies, there is still a chance for SiGe-based technologies in the field of mm and sub-mm wave circuits and drivers, for power amplifier stages in the sub-mm and THz range [3], [4].

Getting the best of both SiGe- and Si-based technologies, implies looking not only at the electrical performance in terms of speed, power driving capability, and integration density, but also in terms of reliability. In that direction work on SiGe HBT reliability has been already introduced in [5] for a 130 nm technology, and most recently in [6] for a 55 nm technology. In this work we experimentally test the reliability of the n-type MOSFET transistors of a 250 nm SiGe BiCMOS technology.

II. EXPERIMENTAL RESULTS, ANALYSIS, AND SIMULATIONS

In this work we introduce experimental reliability data of a n-type Metal-Oxide-Field-Effect Transistor (nMOSFET) of a 250 nm BiCMOS technology. A transistor with a gate width W=1 μm, a gate length L=240 nm, a gate oxide Tox=5 nm, a retro grade P and N wells [7], and with a maximum operation voltage of 2.5 V +/− 8%, is used as a test device. We particularly focus on the nMOSFET device as a critical piece for high-density digital processing and high-voltage analog devices within a BiCMOS system. An average result of three devices, measured on-wafer, is reported here. All the devices were tested using a Semiconductor Device Analyzer B1500A.

The concurrence of a high electric field with the flow of large number of electrical charges, either electrons or holes, gives rises to charge acceleration, which in turns results in hot carriers (HC) [8], which either get trapped in the gate oxide or generate interface states. Because of HC ionization, charges impacted by accelerated charges are dislodged, resulting in the case of n-type MOSFET, in hot electrons

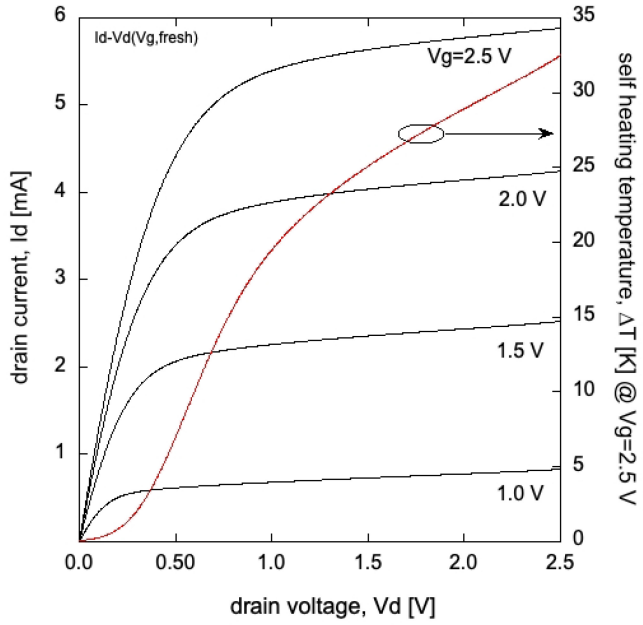

FIGURE 1. Measured Id-Vd characteristics for Vg swept from 1.0 to 2.5 V in steps of 0.5 V. The extracted selfheating temperature is shown at the right axis.

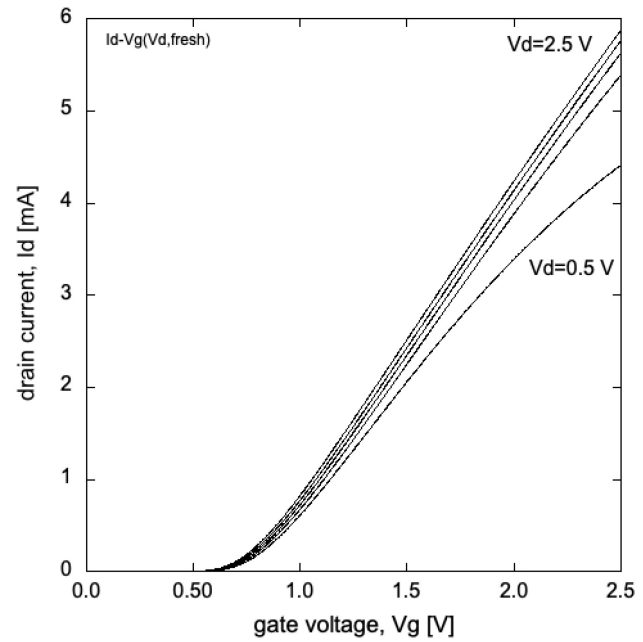

FIGURE 2. Measured Id-Vg characteristics with Vd swept from 0.5 to 2.5 V in steps of 0.5 V.

traveling to the drain side or being trapped in the gate oxide, while hot holes are swept towards the bulk. The hole current collected at the bulk contact becomes the bulk current Ib. The Ib current is considered as a sort of monitor of HC and its associated device degradation.

To start with the analysis, we show, in Fig. 1 and Fig. 2, the experimental results of the drain current versus drain voltage (Id-Vd) and drain current versus gate voltage (Id-Vg) characteristics.

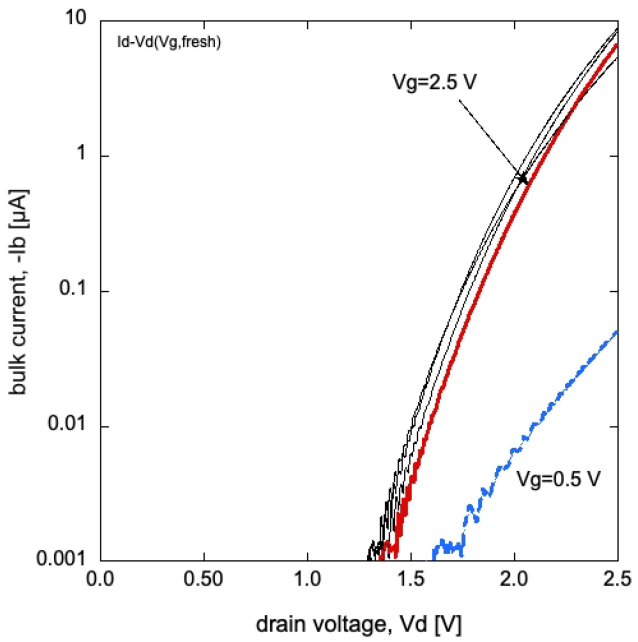

FIGURE 3. Measured bulk current Ib versus drain voltage Vg, for Vg swept from 0.5 V to 2.5 V.

The maximum dissipated power, within the maximum operating voltage, is about 15 mW. And because of the selfheating effect [9], the internal temperature ΔT increases above that of room temperature by about 32 K (see right axis of Fig. 1). The internal temperature was calibrated against the measured Id-Vd versus temperature in the 300 K-350 K range.

The Id-Vd value was measured using a pulsed voltage technique to avoid self-heating [10]. Because of the exponential dependence of the impact ionization on the longitudinal electric field E_l, the Ib-Vd characteristics are expected to follow an exponential behavior as shown in Fig. 3. The light deviation from a pure exponential behavior of the Ib-Vd curve ca be attributed to self-heating as we monitored an average reduction of 49 nA per Kelvin degree, in the 300 K-350 K temperature range, for Vg=Vd=2.5 V. The Ib-Vg, with Vd as a parameter, characteristics in Fig. 4 show a typical bell-shaped curve.

The Ib-Vd shows a typical exponential behavior that obeys the exponential dependence of impact ionization on the longitudinal electric field E_l, which in turns depends on Vd. This behavior can be modeled by Eq. (1).

$$I_b = I_d \int_0^{L_{sat}} \alpha \ \partial x \tag{1}$$

where L_{sat} refers to the length of the pinch off region at the drain side where impact ionization takes place. α refers to the impact ionization coefficient given by Eq. (2) [11].

$$\alpha = \alpha_0 exp\left[-\left(\frac{E_{crit} \cdot \left| \overrightarrow{J_n} \right|}{\overrightarrow{E} \cdot \overrightarrow{J_n}} \right)^{\beta} \right] \tag{2}$$

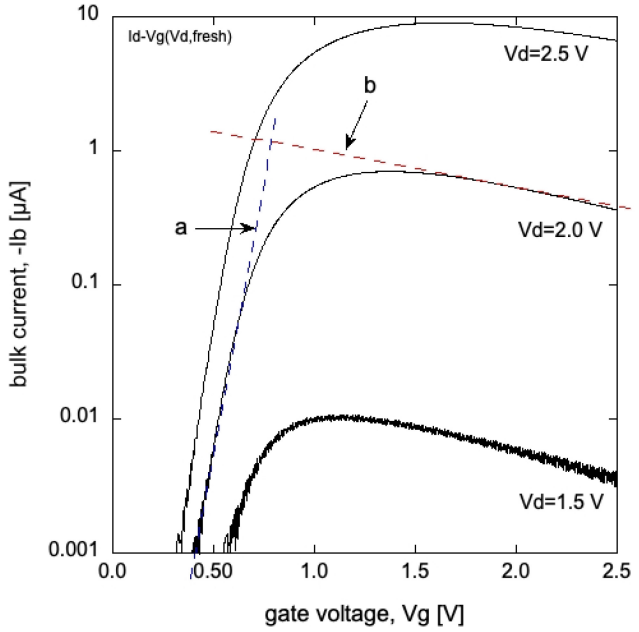

FIGURE 4. Measured bulk current Ib versus gate voltage Vg for Vd swept from 0.5 V to 2.5 V.

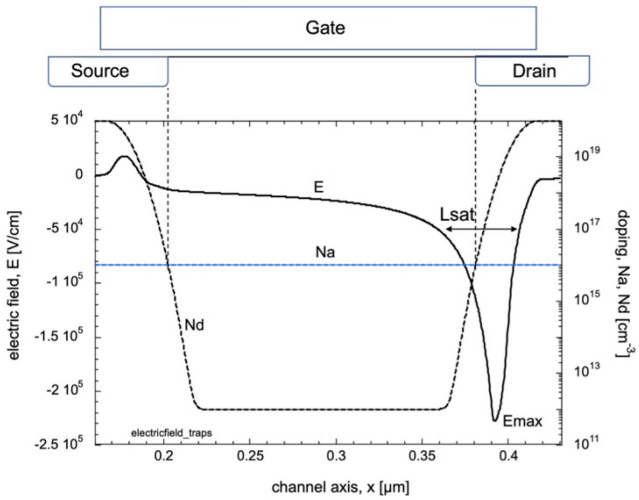

FIGURE 5. Longitudinal electric field E_l distribution along the channel axis x. The doping profile (Nd and Na) is also shown.

where α_0, β, and E_{crit}, are fitting parameters, $\vec{J}_n$ is the electron current density for electrons, and $\vec{E}$ is the electric field.

Impact ionization happens when electrons enter the high field region (see Fig. 5) gaining energy and dislodging holes when impacting the drain side. Most of the hot electrons flow to the drain contact and some other might tunnel through the gate oxide. In the case of a nMOSFET, the hot holes flow to the bulk to become the bulk current Ib.

For having impact ionization, two conditions are required; the existence of a high enough longitudinal electric field E_l for carriers to be accelerated to gain additional energy, and enough carriers flowing through the high field region. This

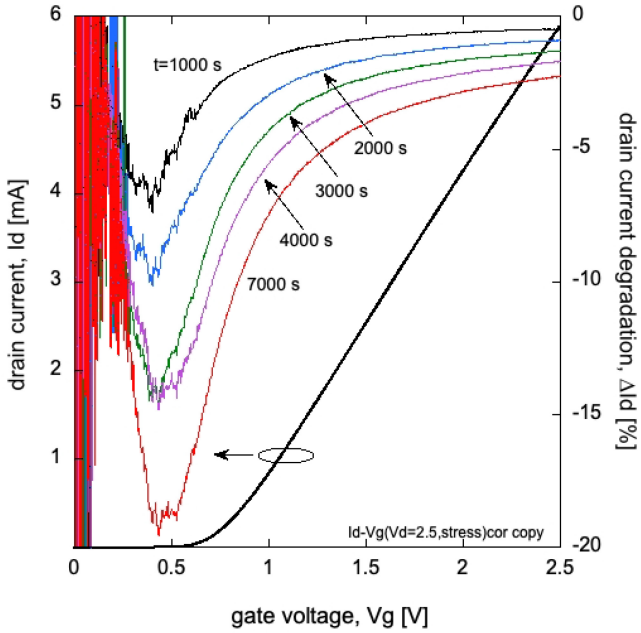

FIGURE 6. Measured Id current and drain current degradation ΔId versus Vg for 5 different stressing times.

condition is shown by the dashed lines in Fig. 4. The line with positive slope marked with the letter "a" describes the linear dependence of Ib with respect to Id (see Eq. (1)). In this low Vg regime, the electric field E_l has a large value through which the electrons supplied by the Id current flow and ignite impact ionization. As Vg increases E_l reduces resulting in an exponential decrease of the impact ionization α, with the transistor entering the region "b" with the line with negative slope. The longitudinal electric field E_l is controlled by both, the gate and drain voltages.

Now an aging procedure is applied on the transistor to investigate the reliability performance and its correlation to the impact ionization mechanism.

An overvoltage Vd=3.0 V is applied on the drain terminal, while Vg is set to 1.6 V corresponding with the bias condition at maximum bulk current Ib, with 5 different stress times of 1000, 2000, 3000, 4000, and 7000 seconds. We chose Vg=1.6 V because is the voltage at which the impact ionization is maximized and thus the damage caused to the channel-oxide interface. The results of the aging procedure are shown in Fig. 6 and Fig. 7.

From Fig. 6 we observe a larger channel current degradation ΔId in the subthreshold to linear region, which is originated by the increase of the threshold voltage V_T with the stress time as shown in Fig. 8.

The increase of the absolute value of the threshold voltage V_T is understood as a transistor degradation as a much higher voltage is required to turn on the device, and thus an increase of the energy consumption is required. As expected, the transconductance degrades because of the creation of interface defects, which degrades the carrier mobility μ and thus lowers the transconductance gm. The measured

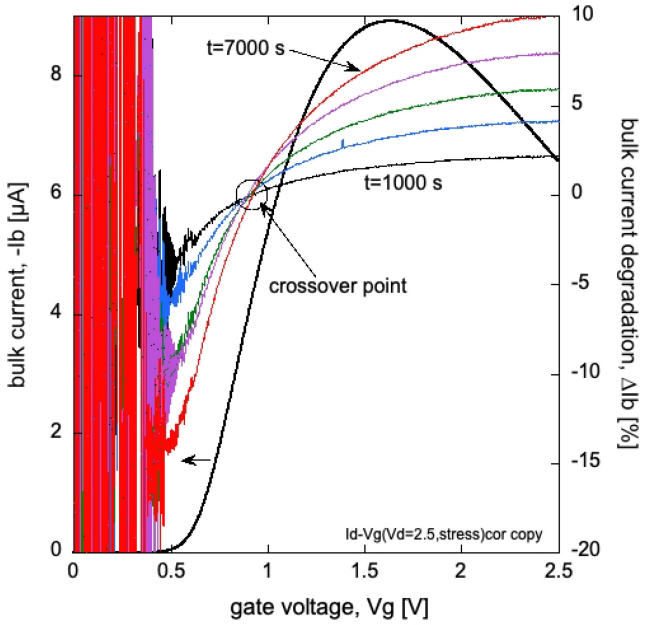

FIGURE 7. Measured Ib and bulk current degradation ΔIb versus Vg at 5 different stress times, with Vd=2.5 V.

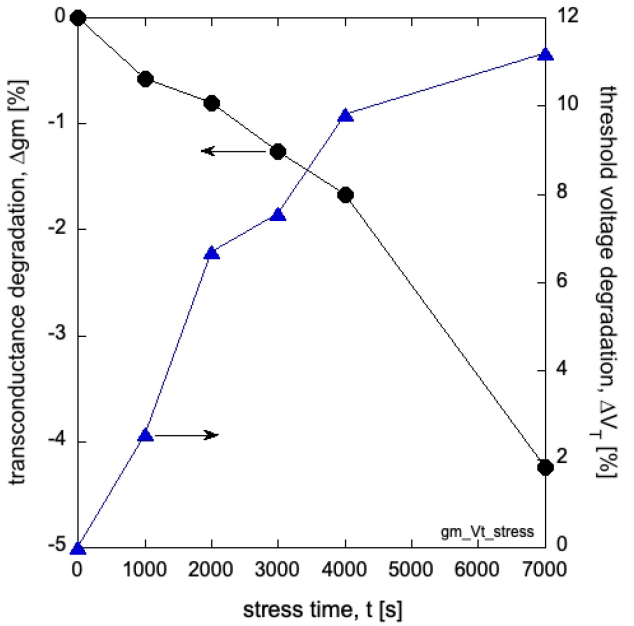

FIGURE 8. Measured transconductance Δgm and threshold voltage ΔVT degradation.

bulk current Ib in Fig. 7, shows a peculiar behavior with a crossover gate voltage point around 0.9 V. Below that voltage value the Ib current reduces with the stress time, but at higher Vg values it increases. As an example, for a Vg=2.5 V and a stress time of 7000 s, the Ib current enhances by a factor of 10% compared to the fresh condition. This effect is interpreted as a boosting of the impact ionization mechanism. Therefore, to understand this boosting, measured as an increase of Ib, we perform numerical simulations with the support of the Minimos-NT 2.1 tool [12].

To simulate the device degradation, a density of defects per unit are D_{it} versus stress time, based on a power law (see Eq. (3)), is used to reproduce the effect of stress time on the degradation or reliability of the transistor.

$$D_{it} = a \cdot t^{b} \tag{3}$$

The simulation results, setting a=6x10^6 cm^{-2} and b=0.5, are shown Fig. 9.

The simulated ΔId-Vg characteristics shown in Fig. 9 resembles those of the experimental results in Fig. 6, with a larger current degradation ΔId at low Vg values compared to those obtained at high Vg values.

The simulated Ib and corresponding degradation ΔIb, are shown in Fig. 10. The shape of these Ib- and ΔIb-Vg simulated characteristics, are alike the experimental ones, except for the magnitude that does not matches.

The magnitude mismatch is attributed to the fact that we did not calibrate the impact ionization model used for the numerical simulations. Despite that fact, the match is good from the qualitative point of view as the crossover point of the ΔIb-Vg and the Ib boosting, are reproduced.

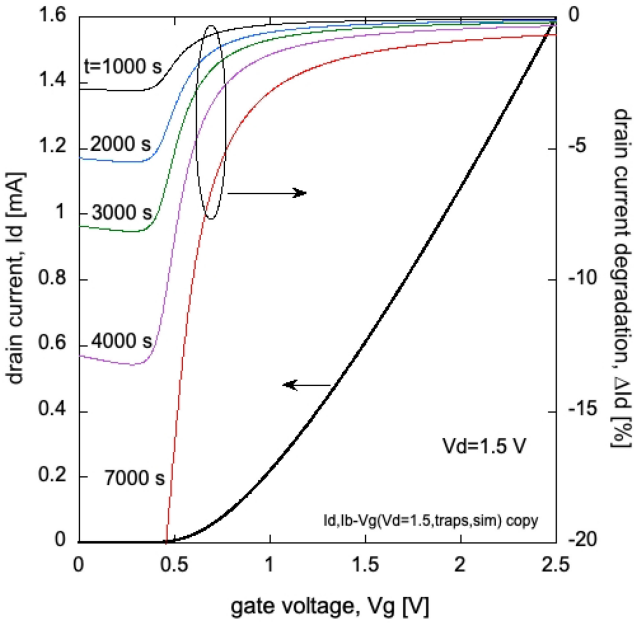

FIGURE 9. Simulated Id and ΔId versus Vg voltage for 5 different stress times, for Vd=1.5 V.

To back up the physical reasoning behind the simulations, the boosting of impact ionization ΔIb and drain current degradation ΔId is simulated and plotted versus Dit in Fig. 11. As the stress time increases, the density of interface states D_{it} increases as predicted by Eq. (3). This is reproduced in the x-axis of Fig. 11, where both ΔId and ΔIb are simulated as a function of D_{it}. The simulation reproduces the degradation of Id and the boosting of Ib as shown by

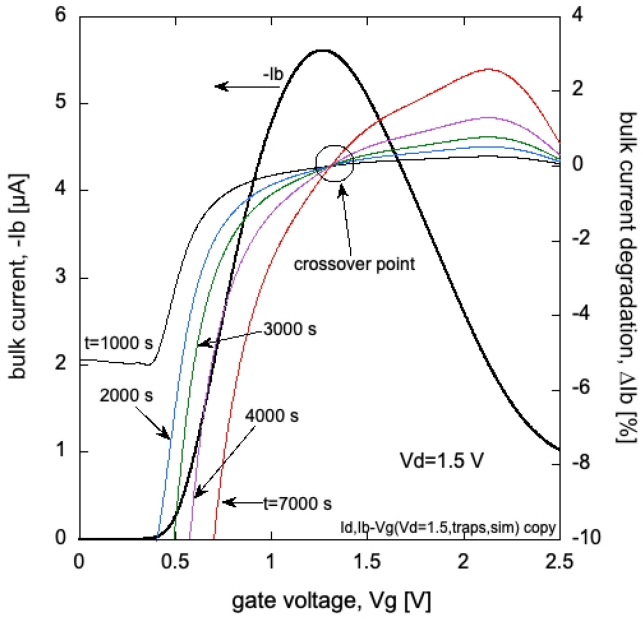

FIGURE 10. Simulated Ib and ΔIb versus Vg curves for 5 different stress times, Vd=1.5 V.

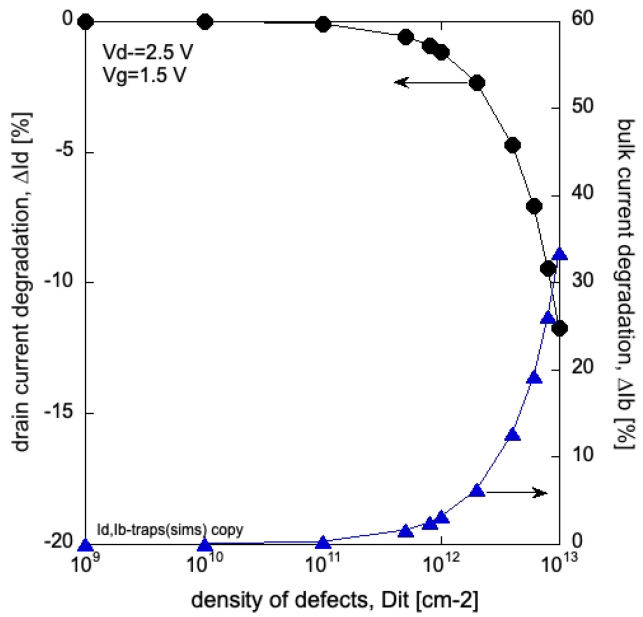

FIGURE 11. Simulation of the degradation values ΔId and ΔIb versus the density of interface defects, at Vd=2.5 V and Vg=1.5 V.

an increase ΔIb of about +33% for Dit=10^{13} cm^{-2} and a ΔId=12%.

As we mentioned before, the hot electrons which gain energy from the longitudinal electric field E_l, are responsible for the creation of interface defects generated by impact ionization. Then, we proceed to simulate the internal electric field, with both its longitudinal and transversal components, E_l and E_t, respectively. Both simulated electric field components as a function of Dit, are plotted in Fig. 12. As D_{it}

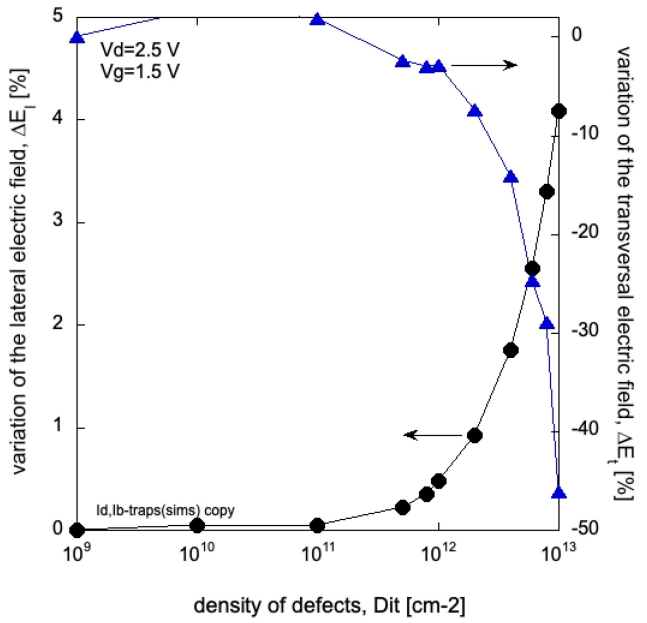

FIGURE 12. Simulation of the value of the magnitude of the lateral E_l and transversal E_t electric field, captured at the maximum value of the electric field in the pinch-off region (see Emax at figure 3). For Vd=2.5 V and Vg=1.5 V.

increases the E_t component gets shielded by the generation of defects, which reduces its magnitude with a corresponding degradation of the transconductance gm and drain current Id. On the other hand, the shielding of E_t results in an increase of the longitudinal electric field E_l, with the consequent increase of the energy source for electron impact ionization.

III. CONCLUSION

The experimental evidence of impact ionization boosting, measured by the increase of the bulk current Ib when the Id current degrades, is qualitatively reproduced with numerical simulations. The numerical simulation, based on a Dit-stress calibration model, shows the boosting of impact ionization is correlated to the increase of the longitudinal electric field E_l at the pinch-off region. And that the increase of E_l is a result of the reduction of the transversal electric field E_t shielded by the interface trap generated by the electrical stress applied on the transistor. We also were able to reproduce the crossover point at the Vg voltage where Ib goes from degradation to boosting.

ACKNOWLEDGMENT

First author would like to thank GlobalFoundries for providing the devices for the experimental work, and INAOE-Conacyt for providing the laboratory iunfrastructure. Second and third authors thank Conacyt for providing PhD scholarships.

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