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High Temperature and Width Influence on the GIDL of Nanowire and Nanosheet SOI nMOSFETs

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ABSTRACT In this work, an experimental evaluation of Gate-Induce Drain Leakage (GIDL) current is presented for nanowire and nanosheet-based SOI transistors. The effects of fin width and temperature increase are studied. Obtained results indicate that the increase in device width makes the GIDL current more sensitive to temperature increase. Three-dimensional numerical simulations have shown that despite the reverse junction leakage increase with temperature, leakage current in nanosheet and nanowire transistors is composed predominantly of GIDL current. The change in valence and conduction bands caused by temperature increase favors the band-to-band tunneling, which is responsible for the worsening of GIDL at high temperatures.

INDEX TERMS GIDL, high temperature, nanosheet MOSFET, nanowire MOSFET, SOI.

I. INTRODUCTION

Multiple gate FETs are the most promising devices to succeed planar MOSFETs in advanced technological nodes, allowing for the continuation of scaling [1]. Multiple-gate devices have achieved enough maturity for mass production and can already be found in commercial applications [2], [3], [4]. The reduction of fin height gave origin to nanowire and nanosheet transistors, whose fin height (H_{FIN}) is in the order of 10 nm. The nanowire MOSFET is a triple gate (or tri-gate) transistor with fin width (W_{FIN}) in the same order of fin height [1], [5]. On the other hand, a nanosheet transistor is a tri-gate with W_{FIN} higher than H_{FIN}, with H_{FIN} being equal to or smaller than 10 nm [6]. When fabricated in Silicon-On-Insulator (SOI) substrates, these devices take advantage of the improved electrostatic coupling, further contributing to reducing short-channel effects occurrence [6].

The improvement of electrostatic control provided by fully depleted devices associated with the high-k dielectrics has substantially reduced the gate leakage in planar MOSFETs, increasing the relevance of another leakage mechanism, the so-called Gate-Induced Drain Leakage (GIDL), as the primary source of off-state current in MOSFETs [7], [8], [9], with an important impact on static power. The GIDL consists of a drain current caused by trap-assisted tunneling (TAT) and band-to-band tunneling (BTBT) effects occurring in the overlap between the highly doped drain region and the gate stack, due to lateral diffusion in the PN junction [8]. This effect becomes more significant as the gate voltage is reduced, moving the device toward the accumulation of the channel.

Multiple-gate transistors such as FinFETs are believed to have smaller GIDL than planar MOSFETs due to the reduction of the electric field provided by the fully depleted

body [10], [11]. Although nanowire and nanosheet transistors are usually expected to have negligible GIDL, the strong gate coupling generated by the reduced dimensions is responsible for the increase of the longitudinal band-to-band tunneling (L-BTBT) of electrons from the body to the drain [12], [13], additionally to the transverse BTBT.

Several industrial applications expose MOSFETs to high-temperature environments, such as automotive, aerospace, and oil extraction. In integrated circuits for these applications, it is relevant that the transistors preserve their electrical characteristics with slight variation or degradation compared to room temperature operation. However, it is well known that the electrical characteristics of semiconductors, such as mobility [14], carrier velocity saturation [15], threshold voltage and subthreshold slope [16], and leakage current [17] are strongly dependent on the temperature, which might result in a change of circuits performance as a function of the operating temperature.

The GIDL effect in nanowire transistors has been modeled and investigated through simulations and some experimental data, as in [12], [18], [19], at room temperature. To the best of the authors' knowledge, experimental measurements of GIDL at high temperatures were reported only at [9], [20].

This paper investigates the effect of temperature increase on the GIDL current of SOI nanowire and nanosheet transistors with different widths. The characteristics of the measured devices are presented in Section II. Section III presents the experimental data extracted from fabricated transistors operating in temperatures ranging between 300 K and 580 K. To have a physical insight into the experimental results, three-dimensional numerical TCAD simulations were performed to investigate the change in the internal characteristics of nanowire and nanosheet transistors with temperature variation, and the results are shown in Section IV. The conclusions are summarized in Section V.

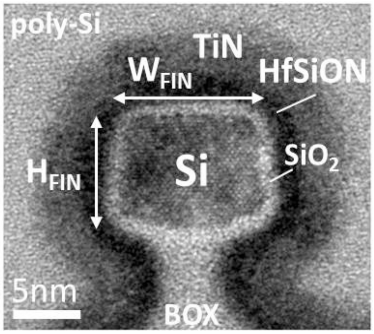

FIGURE 1. TEM cross-section image of an SOI nanowire [21].

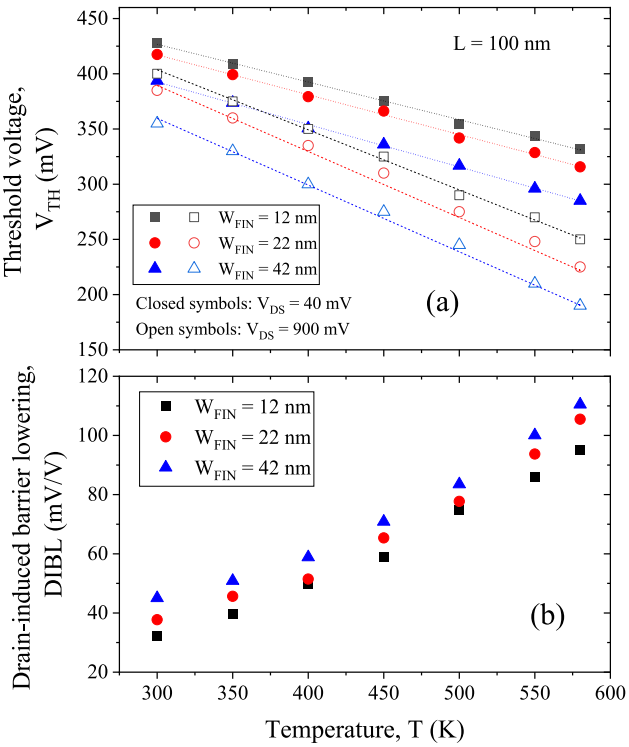

FIGURE 2. Extracted (a) threshold voltage, measured at drain bias V_{DS} = 40 mV and 900 mV, and (b) drain-induced barrier lowering as a function of temperature for nanowire and nanosheet transistors.

II. DEVICE CHARACTERISTICS

The n-type triple gate MOSFETs measured in this work were fabricated at CEA-Leti, using Silicon-on-Insulator (SOI) wafers with a buried oxide thickness of 145 nm [21]. The fin height is 10 nm, and the fin width is 12 nm, 22 nm, and 42 nm, with a channel length (L) of 100 nm and ten parallel fingers. The total channel width of each device has been calculated as $W_T = 10\times(2H_{FIN}+W_{FIN})$. The channel region is not intentionally doped. The gate stack is formed by a thin interfacial SiO_2 layer, followed by 2.3 nm HfSiON, 5 nm TiN, and 50 nm polysilicon. The effective oxide thickness (EOT) is 1.4 nm. Fig. 1 presents a TEM image of the cross-section of a silicon nanowire, showing its height and width.

Drain current curves were obtained from measurements performed directly on the wafer using a B1500A Semiconductor Analyzer. The temperature has been varied between 300 K and 580 K with 50 K-steps, using a Low-Temperature Micro Prober (LTMP) system from MMR Technologies, which ensures temperature accuracy better than 100 mK [22].

From the drain current (I_D) as a function of the gate voltage (V_G) measured at drain-to-source voltage bias, V_{DS} = 40 mV, the threshold voltage (V_{TH}) has been extracted for all devices and temperatures using the double derivative technique [23]. The threshold voltage at V_{DS} = 900 mV has been obtained considering the same current level measured at V_{TH} with low drain bias. The results of V_{TH} *versus* temperature are presented in Fig. 2(a). The temperature increase promoted a linear V_{TH} decrease. The threshold voltage reduction is caused by the rise of intrinsic carrier concentration (n_i) at higher temperatures, reducing the Fermi potential (ϕ_F) and the flatband voltage [24]. The width reduction increases the threshold voltage due to strong potential coupling between

TABLE 1. Rate of variation of the threshold voltage with temperature (dV_{TH}/dT) for the measured devices.

W_{FIN} (nm)	dV_{TH}/dT (mV/K)	
	V_{DS} = 40 mV	V_{DS} = 900 mV
12	0.341	0.539
22	0.361	0.569
42	0.385	0.588

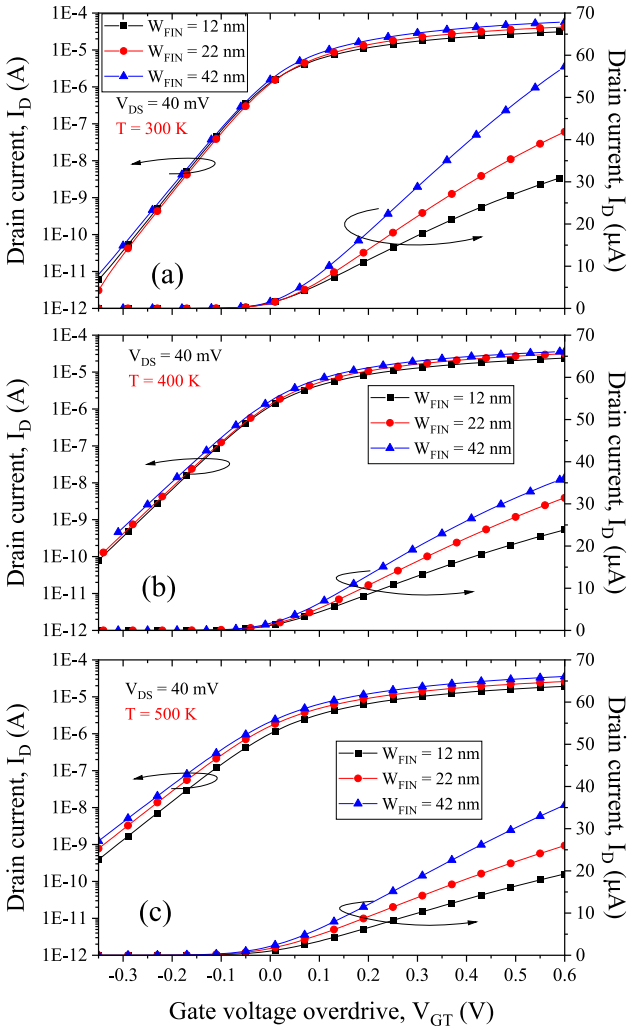

FIGURE 3. Drain current as a function of gate voltage measured at V_{DS} = 40 mV for nanowire and nanosheet transistors at 300 K (a), 400 K (b), and 500 K (c) in log and linear scales.

the top and sidewall gates. The rate of variation of the threshold voltage with temperature (dV_{TH}/dT) is shown in Table 1 for both V_{DS} values. The improved potential coupling caused by fin width reduction is also responsible for the slight decrease in the $|dV_{TH}/dT|$ rate [25]. For all devices, the increase of drain bias leads to the reduction of V_{TH} due to drain-induced barrier lowering, which becomes more pronounced as the temperature is raised, as presented in Fig. 2(b). Even though the DIBL becomes slightly larger with the W_{FIN} increase, its degradation with temperature rise is similar for all measured devices.

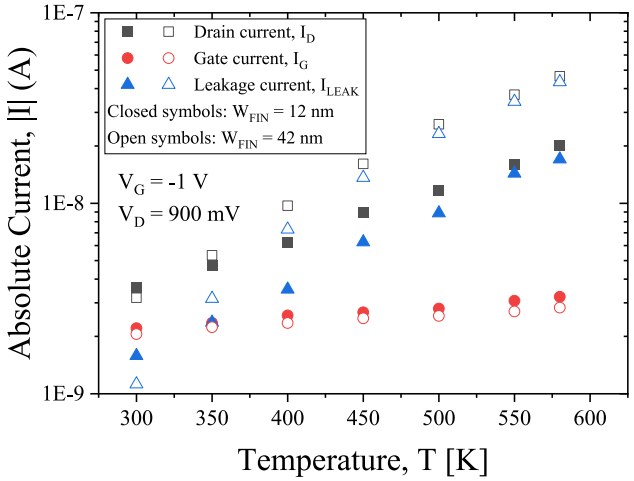

FIGURE 4. Drain current, gate current, and leakage current as a function of the temperature measured at V_{DS} = 900 mV and V_G = −1V for nanowire and nanosheet transistors with W_{FIN} = 12 nm and 42 nm.

Fig. 3 presents the drain current (I_D) as a function of the gate voltage overdrive, $V_{GT} = V_{GS} - V_{TH}$, measured at drain-to-source voltage bias, V_{DS} = 40 mV, in linear and logarithmic scales, at 300 K (A), 400 K (B), and 500 K (C). The increase in temperature reduces the drain current level for all devices due to mobility (μ_n) reduction [14]. The larger the W_T, the higher the current level for any given temperature. This increase is not only associated with the width but also with the fact that as the width is augmented, a more significant portion of the drain current flows in the (100) direction, which is favorable for electrons [26]. From the logarithmic scale curves, one can note that the subthreshold slope (SS) is weakly affected by the W_{FIN} increase. At 300 K, the SS is close to 61.5 ± 0.8 mV/dec for all devices.

III. EXPERIMENTAL GIDL RESULTS

For the GIDL analysis, the applied drain bias has been increased to V_{DS} = 900 mV, and the gate voltage swept down to −1 V, which is well below the threshold voltage. In this region, the device is turned off, and the measured drain current is composed of leakage components: junction leakage ($I_{JUNCTION\ LEAK}$), gate-induced drain leakage current (I_{GIDL}), and gate current (I_G). Fig. 4 presents the measured drain and gate current and the resulting leakage current ($I_{LEAK} = I_{JUNCTION\ LEAK} + I_{GIDL}$), measured at V_G = −1V, for the devices with W_{FIN} = 12 nm and 42 nm. At room temperature, the gate current corresponds to approximately 60% of the total drain current for both devices. As the temperature is raised from 300 K to 580 K, the gate current linearly increases, with a rate of 3.5 pA/K and 2.6 pA/K for the devices with W_{FIN} = 12 nm and W_{FIN} = 42 nm, respectively. On the other hand, the leakage current presents an exponential increase with temperature.

The obtained leakage current is composed of the GIDL component due to the band-to-band tunneling and the junction leakage ($I_{JUNCTION\ LEAK}$), expressed by equation (1),

where q is the electron charge, A is the junction area, D_n is the diffusion coefficient for electrons, τ_n is the electron lifetime, n_i is the intrinsic carrier concentration, W_{depl} is the depletion width, τ_e is the effective lifetime related to thermal generation in the depletion region [27]. This equation shows that the junction leakage is proportional to the junction area and the intrinsic electron concentration, which is exponentially dependent on the temperature. The first term of equation (1), related to the diffusion component, is proportional to n_i^2, and the second term (generation component), is proportional to n_i. Experimental results show that the junction leakage in SOI transistors varies as n_i for temperatures up to 400 K – 450 K and as n_i^2 above those temperatures [28].

$$I_{JUNCTION\ LEAK} = qA\left(\frac{D_n}{\tau_n}\right)^{1/2}\frac{n_i^2}{N_A} + qA\frac{n_i W_{depl}}{\tau_e} \quad (1)$$

Fig. 5 presents the measured I_D-V_G curves at V_{DS}=900 mV for the nanowire nanosheet devices for different temperatures, compensating for the gate current. The leakage current, $I_{LEAK} = I_{JUNCTION\ LEAK} + I_{GIDL}$, extracted at $V_G = -1$ V, is shown in Fig. 6. The results show that I_{GIDL} rises with width increase for a fixed gate voltage, especially for temperatures above 300 K.

At low absolute gate voltage, $|V_G|$, the gate-induced drain leakage is dominated by trap-assisted tunneling, whereas at high $|V_G|$, the band-to-band tunneling dominates [10]. Equation (2) presents the analytical model for the BTBT component of the GIDL current [9], being A and B are temperature-dependent parameters, and E_{max} is the maximum value of the electric field in the overlap region below the gate. As can be seen, the I_{GIDL} is directly proportional to W_T, which may be the cause for its larger leakage current values in the larger transistor.

$$I_{GIDL-BTBT} = W_T\frac{A}{B}E_{max}{}^2\exp\left(-\frac{B}{E_{max}}\right) \quad (2)$$

Therefore, to remove the effect of W_T, the I_{LEAK} has been normalized by W_T. The normalized experimental leakage current (I_{LEAK}/W_T) has been plotted as a function of the temperature and is presented in Fig. 7 for V_{DS}=900 mV and $V_G = -1$ V. The normalized I_{LEAK} has an exponential rise with the temperature for all devices. The slope of linear regression of the I_{LEAK}/W_T is $3.78\text{x}10^{-3}$ A/nm.K, 4.47 A/nm.K, and $5.50\text{x}10^{-3}$ A/nm.K for the devices with $W_{FIN} = 12$ nm, 22 nm, and 42 nm, respectively. Contrary to the results presented in Fig. 5, the normalized I_{LEAK} increases with W_{FIN} reduction for temperatures up to approximately 400 K. However, the larger rate of rise of I_{LEAK}/W_T with temperature presented by larger devices makes the normalized I_{LEAK} higher for T > 450 K. At room temperature, I_{GIDL}/W_T is 2.8 times larger for $W_{FIN} = 12$ nm in comparison to 42 nm. As the temperature increases, this ratio diminishes, and there is an inversion of the trend, leading to an I_{LEAK}/W_T 1.6 times larger for $W_{FIN} = 42$ nm in relation to 12 nm. Similar behavior has been observed for the

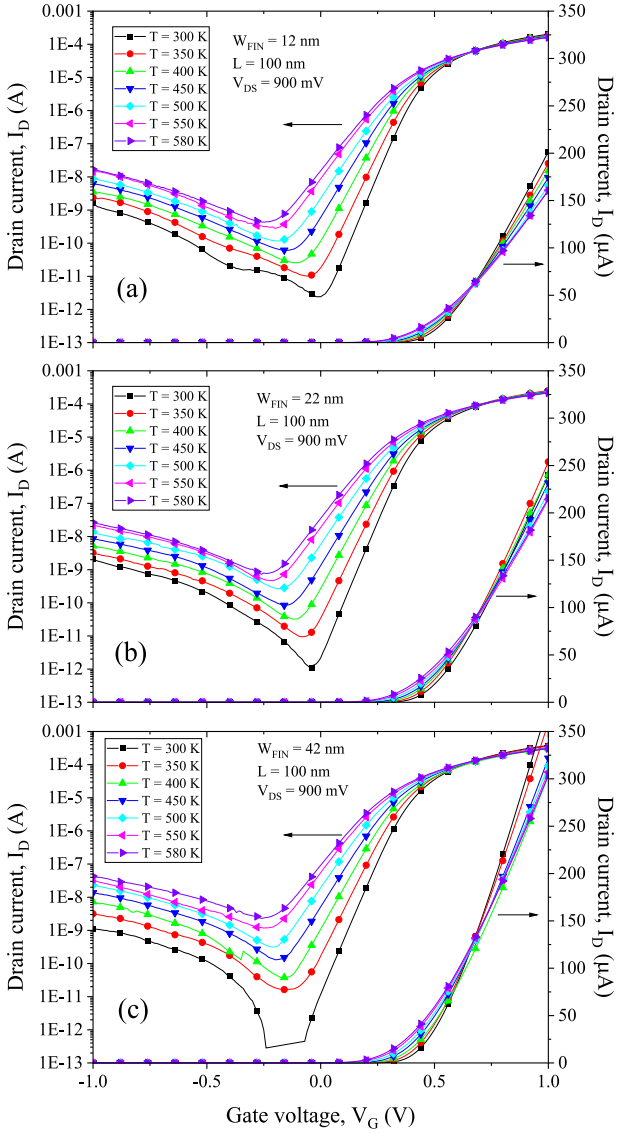

FIGURE 5. Drain current as a function of gate voltage measured at V_{DS} = 900 mV for nanowire and nanosheet transistors with W_{FIN} = 12 nm (a), 22 nm (b), and 42 nm (c) for temperatures ranging between 300 K and 580 K.

GIDL current in stacked nanowire transistors at low temperatures [29], where the junction leakage current is negligible, and the I_{LEAK} can be attributed to GIDL.

Aiming to account for V_{TH} differences and Drain-Induced Barrier Lowering (DIBL) with W_{FIN} and temperature exhibited in Fig. 2, the normalized leakage current has been plotted for the narrower and wider transistors as a function of the temperature for different values of gate voltage overdrive, $V_{GT} = V_{GS} - V_{TH}$. The results are presented in Fig. 8. The increase of $|V_{GT}|$ and consequent larger electric field, E_{max}, leads to the rise of GIDL and hence leakage current. Nevertheless, larger $|V_{GT}|$ reduces the leakage current variation with temperature. Independently of the V_{GT} value, the rate of I_{LEAK} variation with temperature is more prominent in the nanosheet transistor than in the

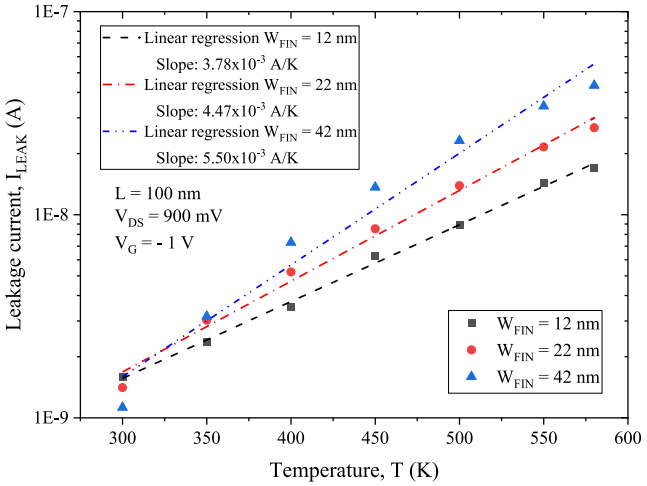

FIGURE 6. Leakage current as a function of the temperature measured for devices with different widths at V_{DS} = 900 mV and V_G = −1 V.

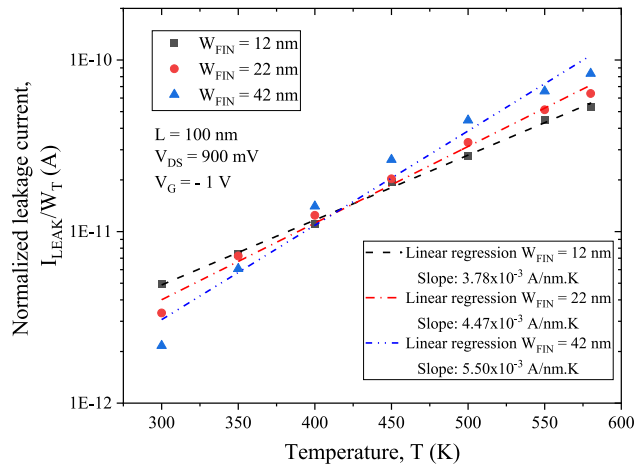

FIGURE 7. Normalized leakage current as a function of the temperature measured for devices with different widths at V_{DS} = 900 mV and V_G = −1 V.

nanowire one, confirming the trend obtained at constant gate voltage, V_G.

IV. THREE-DIMENSIONAL NUMERICAL SIMULATIONS

To make insight into the results presented by the experimental data and separate the effects of GIDL and junction leakage with temperature change, TCAD tridimensional simulations were performed [30]. The simulation structures were created with the same technological and geometrical parameters as the experimental devices. Uniform doping concentrations of $N_A = 1\times10^{15}$ cm^{-3}, $N_{D,ext} = 5\times10^{19}$ cm^{-3}, and $N_{D,SD} = 5\times10^{20}$ cm^{-3} were adopted at the channel, extensions, and source/drain regions, respectively. The simulated structures have a gate/drain overlap of 5 nm at the source and drain sides of the channel. Nanowire and nanosheet SOI MOSFETs with a channel length of 100 nm and fin width ranging between 10 nm and 50 nm were simulated for temperatures between 300 K and 600 K with steps of 100 K.

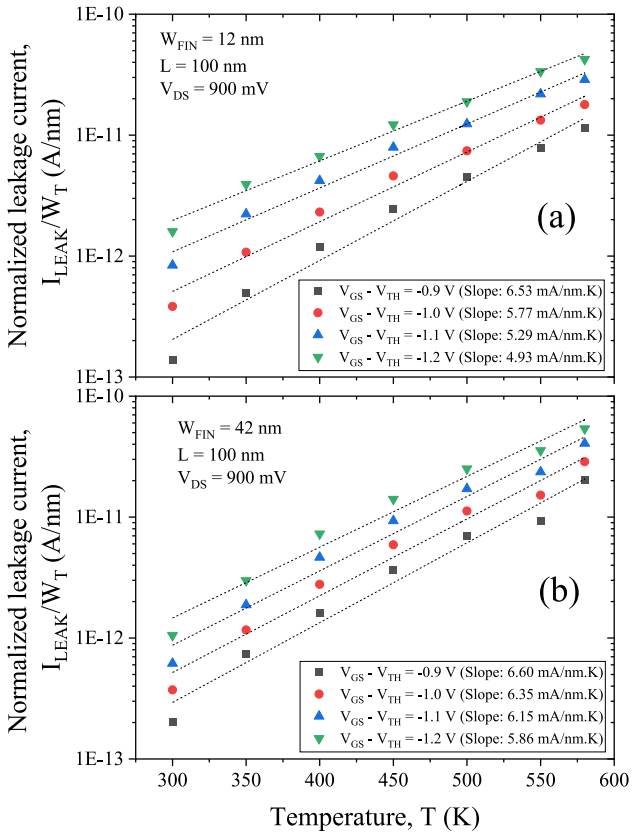

FIGURE 8. Leakage current normalized by the total width as a function of temperature measured at V_{DS} = 900 mV and different gate voltage overdrive for a nanowire (a) and a nanosheet (b) transistor.

The analytical models in the simulations account for the carrier mobility variation with the temperature, Bandgap Narrowing, mobility degradation due to the horizontal and vertical electric fields, and temperature-dependent velocity saturation. Also, Shockley-Read-Hall, Auger, and non-local path BTBT models were considered. Default simulation parameters were used except for the carrier mobility, which has been adjusted to fit experimental data. Simulations without the BTBT model were also performed to obtain the junction leakage current without the GIDL component. No gate current has been simulated for the studied devices to clarify the contributions of junction leakage and BTBT currents on the leakage current.

Fig. 9 presents the drain current as a function of the gate voltage simulated for the transistors with W_{FIN} = 10 nm and 50 nm, at 300K and 600K, obtained with and without the BTBT tunneling model. The simulated results show the increase of junction leakage with temperature and an additional increase when the band-to-band tunneling effect is included in the simulation file.

Fig. 10 presents the simulated I_{LEAK}, $I_{JUNCTION\ LEAK}$, and I_{GIDL} as a function of temperature for the nanowire and nanosheet transistors with W_{FIN} = 10 nm and 50 nm at V_G= −1 V. As can be seen, the junction leakage varies as n_i for temperatures up to ∼500K and approaches n_i^2

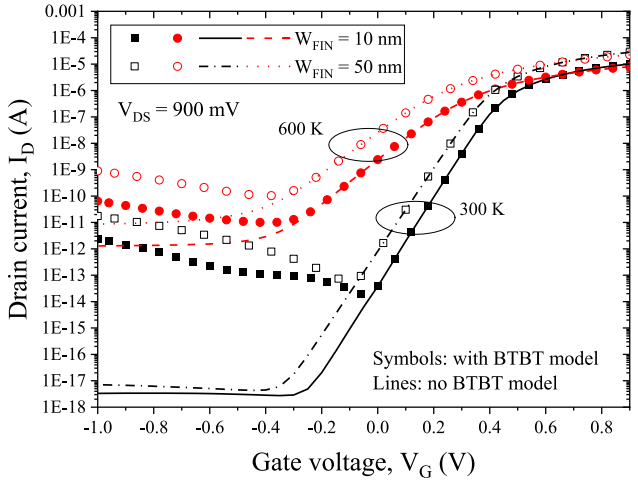

FIGURE 9. Drain current simulated with and without BTBT model, biased at V_{DS} = 900 mV at T = 300 K and 600 K.

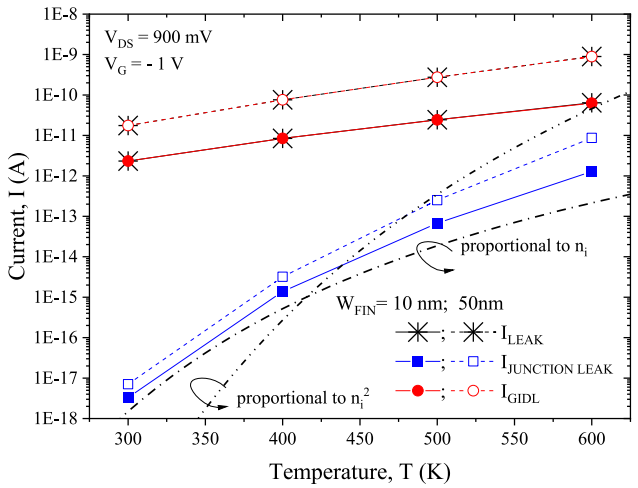

FIGURE 10. Total leakage current, junction leakage, and gate-induced drain leakage as a function of temperature measured at V_{DS} = 900 mV and V_G = −1V, simulated for devices with W_{FIN} = 10 nm and 50 nm.

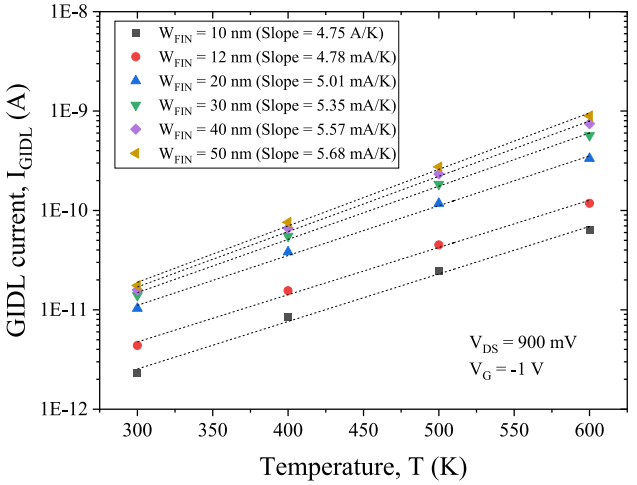

FIGURE 11. Simulated GIDL current, I_{GIDL}, as a function of temperature for nanowire and nanosheet transistors with different fin widths at V_{DS}=900 mV and V_{GS}=−1 V.

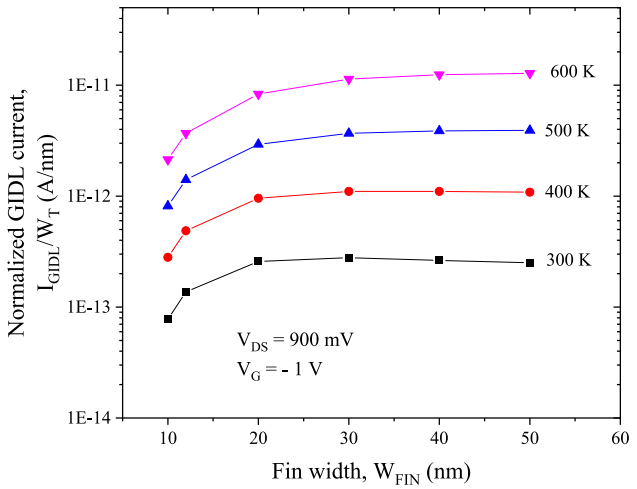

FIGURE 12. Simulated leakage current normalized by the total width as a function of the fin width extracted at V_{DS} = 900 mV and V_G = −1 V at different temperatures.

behavior for higher temperatures. Despite the increase of several orders of magnitude in the junction leakage with temperature rise, the total I_{LEAK} is dominated by the BTBT current component for both fin widths, indicating that the I_{LEAK} tendencies observed in experimental data are related to GIDL current rather than junction leakage.

The GIDL current for transistors with different fin widths is presented as a function of the temperature in Fig. 11. The experimental results tendencies with temperature and device width are reasonably reproduced by the simulations shown in Fig. 8, indicating that the physical phenomena associated with the set of models used in the simulations can reproduce observed GIDL behavior. One can see a slightly increased I_{GIDL} variation with the temperature in the simulations than for the experimental data for both narrow and large fin devices, which may be related to the use of default model parameters.

The normalized GIDL current, I_{GIDL}/W_T, as a function of fin width is presented for all simulated temperatures in Fig. 12. It can be observed that the normalized GIDL current is slightly dependent on the width above W_{FIN} = 30 nm.

To have a deeper insight into the origin of GIDL current, the band-to-band current generation has been extracted from the simulated structures. Fig. 13 confirms that band-to-band generation (BTBG) occurs mainly at the drain extension region, under the gate/drain overlap.

BTBG cuts were extracted at different positions along the longitudinal direction (x-axis indicated in Fig. 13) for three fin widths. The results at 300 K are presented in Fig. 14. As the fin width is reduced, the strong gate coupling moves the BTBG to the center of the nanowire in comparison to wider devices, as can be seen in Fig. 14(a)-(c). For the device with W_{FIN} = 10 nm, the peak of BTBG in the drain-body junction

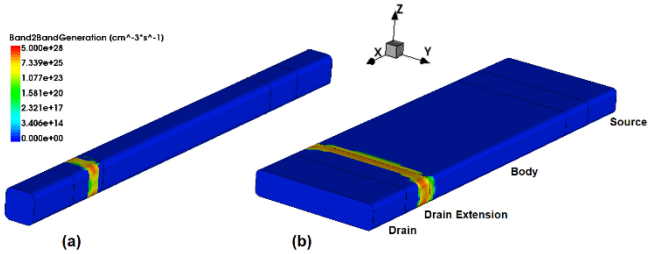

FIGURE 13. 3D-view of the band-to-band generation in the silicon region of devices with W_{FIN} = 10 nm (a) and 50 nm (b) extracted at V_{DS} = 900 mV and V_G = −1 V, at 300 K.

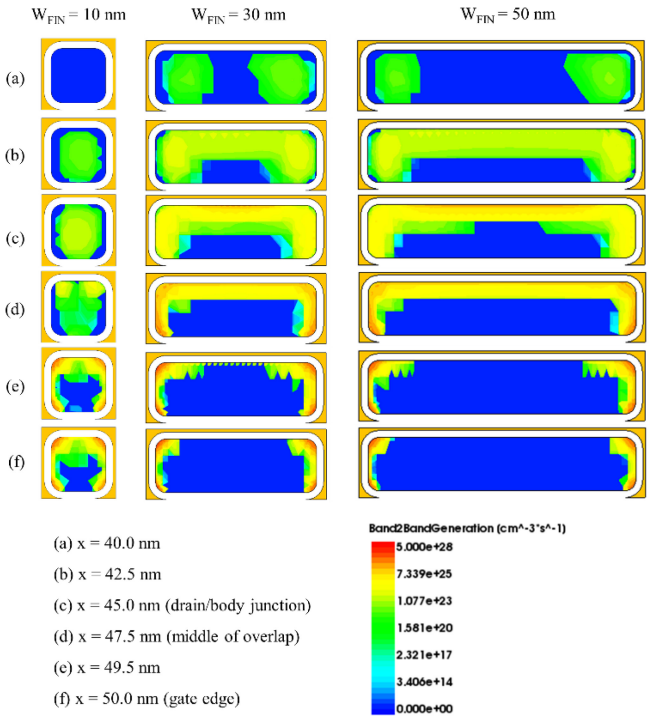

FIGURE 14. Simulated band-to-band generation profiles, at V_{DS} = 900 mV and V_G = −1 V, extracted from simulated devices with W_{FIN} = 10 nm, 30 nm, and 50 nm, at T = 300K and different positions.

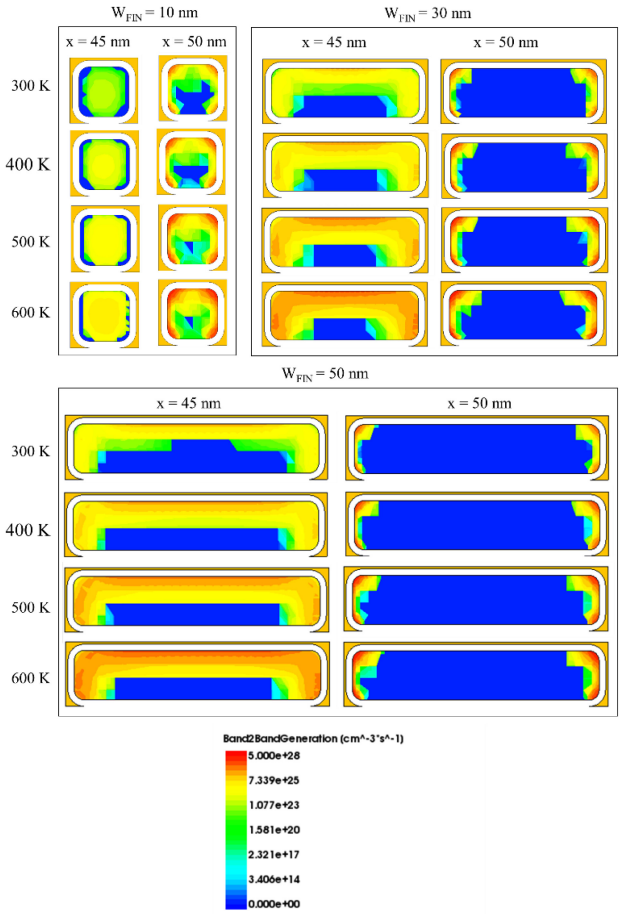

FIGURE 15. Simulated band-to-band generation profiles, at V_{DS} = 900 mV and V_G = −1 V, extracted from simulated devices with W_{FIN} = 10 nm, 30 nm, and 50 nm, at T = 300K and the junction and the gate edge at different temperatures.

is observed at the center of the silicon nanowire, indicating the longitudinal tunneling of electrons from the body to the drain extension under the overlap [12]. On the contrary, for the devices with W_{FIN} = 30 and 50 nm, the BTBG occurs closer to the Si-SiO_2 interface. Moving closer to the end of the overlap, at the gate edge (Fig. 14(e)-(f)), the BTBG becomes more pronounced at the corners due to the larger electric field in this region [31]. In all cases, the intensity of BTBG is higher for the wider devices than for the nanowire due to the improved gate coupling.

The effect of temperature increase in the BTBG is shown in Fig. 15. The presented results were extracted at the drain extension-body junction (x = 45 nm) and the gate edge (x = 50 nm) for the devices with W_{FIN} = 10 nm, 30 nm, and 50 nm and all simulated temperatures. The temperature rise promotes an increase in the band-to-band generation intensity and an increase in the area of the device cross-sections where tunneling occurs. In the case of the nanowire with 10 nm of width at 600 K, there is band-to-band tunneling in practically the entire silicon cross-section. However, the BTBG intensity remains lower and less temperature-dependent in the nanowire transistor with W_{FIN} = 10 nm.

The band diagram along the longitudinal direction has been extracted at the middle of fin height, 2 nm from the sidewall, for the devices with W_{FIN} = 10 nm and 50 nm. The results obtained at T = 300 K and 600 K are exhibited in Fig. 16. The increase of valence band energy (E_V) at the body side (p-type) with temperature is more pronounced than the increase of conduction band (E_C), reducing the lateral distance between E_C and E_V inside the overlap region, which favors the tunneling of electrons from the valence band of the body to the conduction band of the drain, increasing band-to-band generation. The results show larger BTBG in the wider device for both temperatures. In addition, it is possible to see that for the narrower transistor, tunneling is more pronounced within the overlap region and close to the extension/body junction. In contrast, the tunneling is

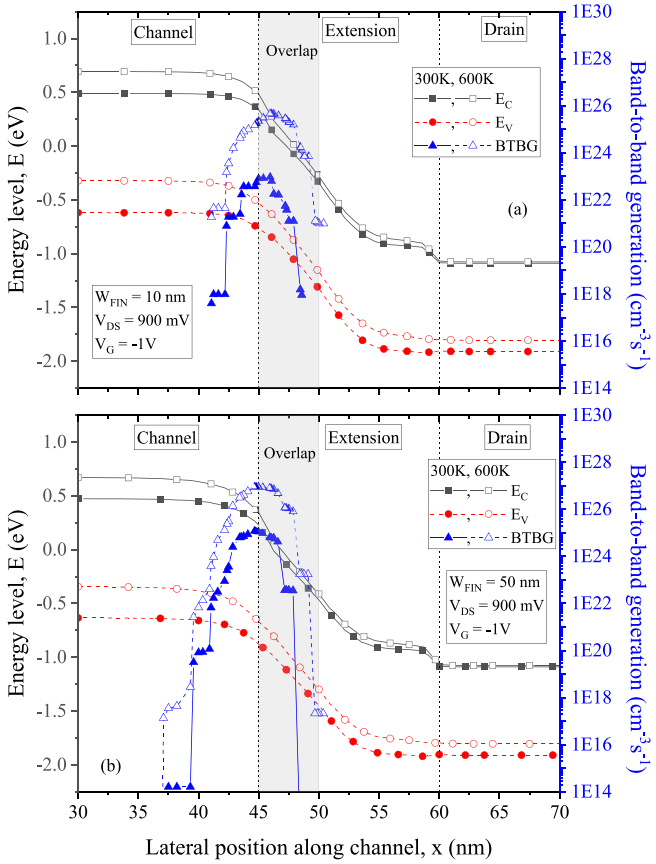

FIGURE 16. Longitudinal energy band and band-to-band generation extracted from 3D simulation of nanowire and nanosheet transistors with W_{FIN} = 10 nm and 50 nm, at T = 300K and 600 K, biased at V_{DS} = 900 mV and V_G = −1 V.

extended to the interior of the p-type body for the wider transistor (see also Fig. 14(a)) due to the weakening of coupling, contributing to the increase of I_{GIDL} with W_{FIN} increase.

V. CONCLUSION

An analysis of the GIDL effect in nanowire and nanosheet-based SOI transistors is presented. Experimental data shows that the GIDL current dependence on temperature becomes more pronounced as the width increases. Three-dimensional numerical simulation results indicate that, despite junction leakage increasing with temperature, the leakage current in nanowire and nanosheet SOI transistors is mainly composed of the GIDL component. Band-to-band generation intensity increases as fin width increases, and the temperature rise contributes to this effect due to the more pronounced increase of valence band energy about the conduction band, contributing to the rise of band-to-band tunneling in the overlap region.

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