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A Compact Amorphous In-Ga-Zn-Oxide Thin Film Transistor Pixel Circuit With Two Capacitors for Active Matrix Micro Light-Emitting Diode Displays

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ABSTRACT In this paper, we propose a novel amorphous In-Ga-Zn-oxide (a-IGZO) thin film transistor (TFT) pixel circuit for pulse width modulation (PWM) driving active matrix micro light-emitting diode (μLED) displays. The proposed pixel circuit compensates for wavelength shifts according to gray level and threshold voltage (V_{TH}) variation of TFTs with only two capacitors. This compact operation can be achieved by simultaneous compensation for V_{TH} along with data input in the constant current generation (CCG) circuit and the PWM circuit, which consist the pixel. Since the V_{TH} variation in TFTs is compensated, the proposed pixel circuit can supply a uniform and stable current to the μLED throughout all gray levels. The compensation accuracy was verified by HSPICE with an oxide TFT model based on the measurement data. In addition, we analyzed the optimization method to improve the PWM driving by controlling the electrical properties of TFT, and verified this approach by simulation.

INDEX TERMS Micro light-emitting diode, pixel circuit, amorphous In-Ga-Zn-oxide, thin film transistor, active matrix, pulse width modulation.

I. INTRODUCTION

Micro light-emitting diode (μLED) displays have been attracted attention as the most promising candidate for the next-generation display technologies. The μLEDs generally refer to ultra-small LEDs of less than 100 μm, and have outstanding advantages such as high efficiency, long lifetime, low power consumption, and short response time [1], [2], [3], [4]. In addition, μLED can solve various limitations of organic light-emitting diode (OLED). First of all, μLEDs are safe from burn-in, the most serious and unavoidable problem in OLEDs [5], [6], [7]. Also, μLEDs can maintain high brightness even at temperature below 253 K and above 373 K, whereas OLEDs are extremely degraded under these harsh temperature stress conditions [8], [9]. For deep-blue color expression, μLEDs also have more stable and long operating time compared to OLEDs [10], [11].

Despite this superior potential, the wavelength shift of μLED still remains a major challenge for achieving high-quality displays. The wavelength of the μLED shifts depending on the current density, and this instability causes a severe color distortion in the display [12], [13], [14]. For that reason, conventional OLED driving methods, which control luminance by modulating the current density, cannot be adopted for μLED driving. Instead, pulse width modulation (PWM) driving method, which controls luminance by adjusting the emission time with constant current density, is preferred [5], [15], [16].

In order to implement the PWM driving method, pixel circuit requires the constant current generation (CCG) circuit

and the PWM circuit to supply a constant high current and modulate μLED emission period, respectively [8], [9]. Then, spatial and temporal variation in the threshold voltage (V_{TH}) of thin film transistors (TFTs), which is caused by process fluctuation or unwanted degradation during operation, should be considered in each circuit to achieve luminance uniformity.

In this paper, we propose a novel amorphous In-Ga-Zn-oxide (a-IGZO) TFT pixel circuit for PWM driving μLED displays, which compensates for V_{TH} variation with only two capacitors. The proposed pixel circuit consists of 6 TFTs and 1 capacitor for CCG circuit, and 8 TFTs and 1 capacitor for PWM circuit. Each circuit requires only one capacitor, because the V_{TH} compensation and data input are performed in the same stage [17]. The small number of capacitors has a considerable advantage in increasing pixel density over other conventional circuits with three or four capacitors [5], [18], as capacitors generally occupy a large portion of the pixel layout area. Meanwhile, the constant μLED current of the proposed circuit is above 20 μA, as it is generally known that the current range of tens of μA can ensures the high EQE of the μLED [21]. The gray level is adjusted by modulating the width of the emission period. Also, the V_{TH} compensation accuracy is verified by HSPICE, and the simulation result shows that the proposed circuit can supply a uniform current despite the V_{TH} variation of TFTs throughout all gray levels.

II. PROPOSED PIXEL CIRCUIT

Fig. 1 shows the schematic, signal timing diagram, and layout design of the proposed μLED pixel circuit. As shown in Fig. 1(a), the proposed 14T2C pixel circuit is divided into the CCG circuit consisting of T_CCG, T1-T5, and C1, and the PWM circuit consisting of T_PWM, T6-T12, and C2. Here, T_CCG and T_PWM are driving TFTs of each circuit, and T1-T12 are switching TFTs. For the CCG circuit, T_CCG and T4 are 40 μm in width and 5 μm in length for the high current driving, and other switching TFTs are 5 μm in width and 5 μm in length. For the PWM circuit, T_PWM is 10 μm in width and 5 μm in length, and other switching TFTs are 5 μm in width and 5 μm in length. Two storage capacitors C1 and C2 are 400 fF and 200 fF, respectively. ELVDD and REF are the power and DC lines set to 13 V and 3 V, respectively. In Fig. 1(b), the switching voltage of SCCG, SPWM, and EM signals is ranged from −12 V (V_{GL}) to 15 V (V_{GH}), and SWEEP voltage is swept from 0 V to 9 V during emission period. The switching voltage range was carefully set in consideration of ELVDD, SWEEP, and DATA voltage to ensure that the proposed pixel circuit can operate properly. Meanwhile, the layout design in Fig. 1(c) has smaller size than latest works using metal oxide TFTs [19], [20], [21] due to the small number of capacitors as shown in Table 1. Hence, the proposed circuit can achieve very high pixel density.

The proposed μLED pixel circuit adopts the simultaneous emission method, and the circuit operation is divided into

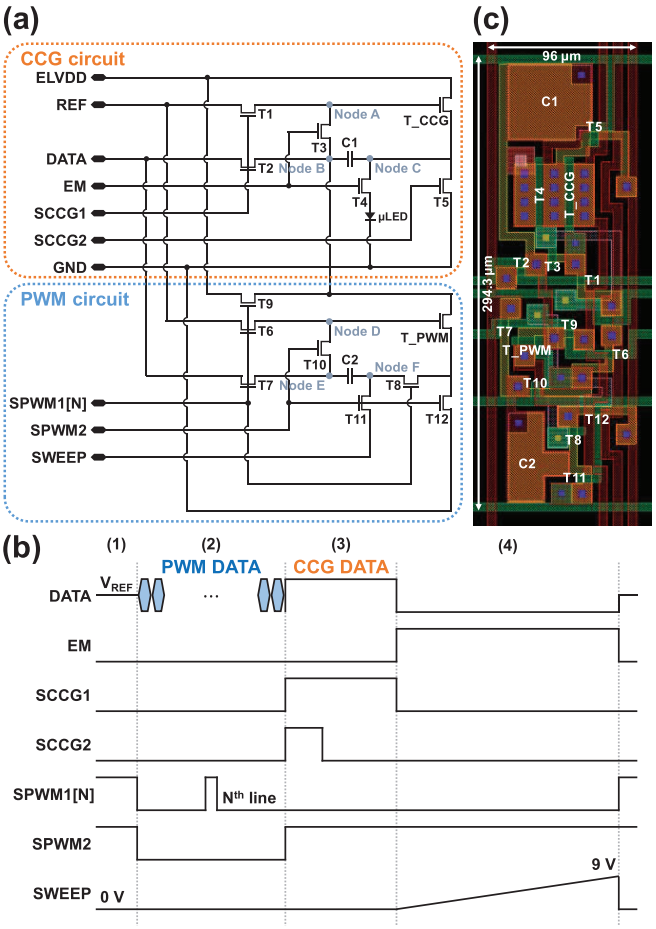

FIGURE 1. The proposed μLED pixel circuit (a) schematic, (b) signal timing diagram for 1 frame time (8.3 ms), and (c) layout design.

TABLE 1. Comparison of the proposed pixel circuit and other works.

Category	TED [19]	SID [20]	SID [21]	Proposed
TFTs	12	12	Sealed	14
Capacitors	3	3	Sealed	2
Signals	9	8	7	7
Sub pixel size (μm)	200 × 600	169 × 507	138 × 415	98 × 294
PPI	42.3	50	61.2	86.4

four stages: (1) reset, (2) PWM data input and T_PWM compensation, (3) CCG data input and T_CCG compensation, and (4) μLED emission. In the reset stage, the SPWM1 and SPWM2 signals are set to a high level, and DATA is applied as V_{REF}, 3 V. All TFTs in PWM circuit are turned on, and the voltage stored in C2 is initialized to V_{REF}. In the PWM data input and T_PWM compensation stage, SPWM2 signal is set to a low level, and SPWM1[N] signal is set to a high level line by line. At the N_{th} line, only T6-T9 are turned on, and DATA is applied as $-V_{DATA\_PWM}[N] + V_{REF}$. Then, the left node voltage of C2 is kept at this value, whereas the right node voltage of C2 is decreased to $-V_{DATA\_PWM}[N]$ at first by charge conservation and gradually increased to V_{REF}

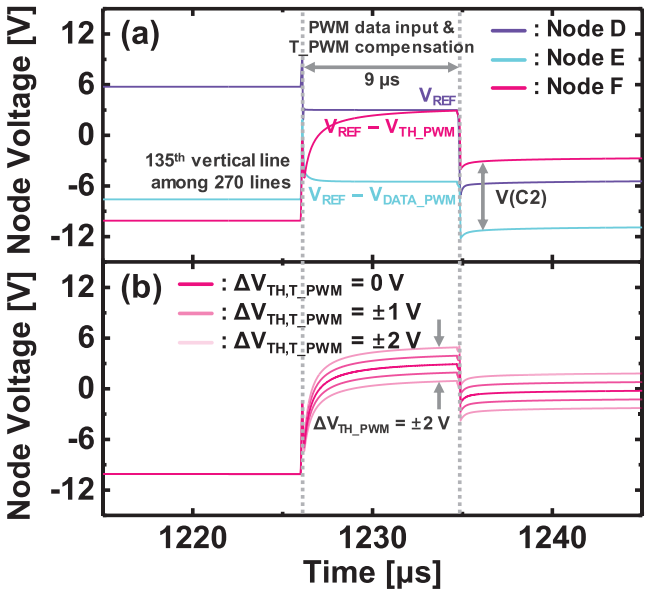

FIGURE 2. (a) Simulated voltage of node D, E, and F when the V_{DATA_PWM} is −8.5 V, and (b) simulated voltage of node C when the V_{TH_PWM} shift ranges from −2 V to 2 V. The PWM data input and T_PWM compensation time for each line is 9 μs.

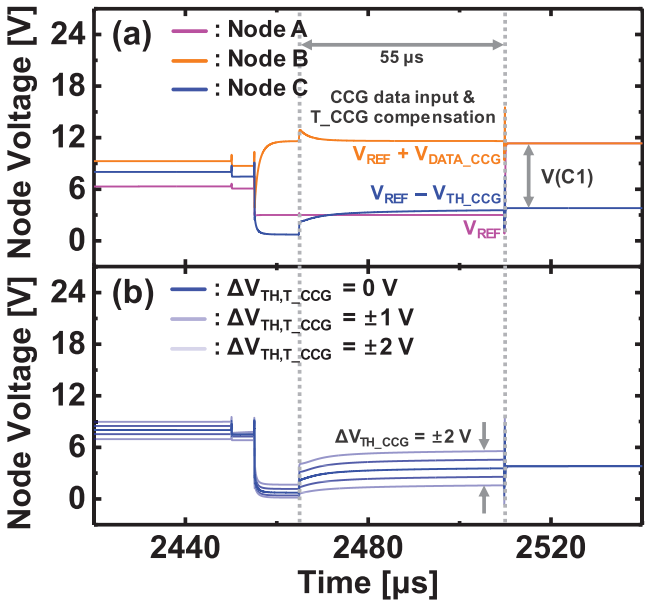

FIGURE 3. (a) Simulated voltage of node A, B, and C, and (b) simulated voltage of node C when the V_{TH_CCG} shift ranges from −2 V to 2 V. The CCG data input and T_CCG compensation time for all lines is 55 μs.

$-V_{TH\_PWM}$. Here, V_{TH_PWM} is the V_{TH} of T_PWM. This process is repeated line by line for the number of vertical lines in the display. At the end of this stage, SPWM2 signal is set to a high level, and C2 stores $-V_{DATA\_PWM}[N] + V_{TH\_PWM}$ for each line. Fig. 2(a) shows the simulated transient waveforms of node D, E, and F voltage during this stage. The simulation is performed for modular-type 480 × 270 resolution display panel, and the timing of Fig. 2(a) is at the 135th vertical line. The total time for PWM data input and T_PWM compensation is 9 μs. Each node voltage exhibits high consistency with the theoretical value described above. Fig. 2(b) shows the node F voltage when the V_{TH_PWM} shifts from −2 V to 2 V. The shift range is set to check the operating margin in case of severe change, and the node F voltage successfully reflects such shift despite the wide variation range.

In the CCG data input and T_CCG compensation stage, SCCG1 and SCCG2 signals are set to a high level, and DATA is applied as $V_{DATA\_CCG} + V_{REF}$. T1, T2, and T5 are turned on, and the voltage stored in C1 is initialized to $V_{DATA\_CCG} + V_{REF}$. After that, SCCG2 signal is set to a low level and T5 is turned off. Then, the left node voltage of C1 is increased to $V_{REF} - V_{TH\_CCG}$, whereas the right node voltage of C1 is kept at $V_{DATA\_CCG} + V_{REF}$. Here, V_{TH_CCG} is the V_{TH} of T_CCG. At the end of this stage, SCCG1 signal is set to a low level and C1 stores $V_{DATA\_CCG} + V_{TH\_CCG}$. As V_{TH_CCG} is included in the voltage stored in C1, a uniform current can be supplied to each pixel regardless of V_{TH_CCG} variation across the panel. The voltage stored in C2 is hardly perturbed during this stage. Fig. 3(a) shows the transient waveforms of node A, B, and C voltage during this stage. Since the proposed μLED pixel circuit adopts a simultaneous emission method, CCG data input and T_CCG compensation is performed at the same time for all vertical lines. The CCG data input and T_CCG compensation time is 55 μs, and each node voltage also exhibits high consistency with the theoretical value described above. Fig. 3(b) shows the node C voltage successfully reflects V_{TH_CCG} variation from −2 V to 2 V, as in previous stage. For both CCG and PWM circuits, V_{TH} compensation and data input are performed in the same stage with only one capacitor, so area-efficient design and operation are possible with achieving high compensation accuracy. In the μLED emission stage, EM signal is set to a high level, and SWEEP voltage begins sweeping from 0 V. T3 and T4 are turned on, and uniform current flows to the μLED in all subpixels. At the same time, the gate voltage of T_PWM is increased with SWEEP voltage sweeping. As the gate voltage gradually increases, the gate-to-source voltage (V_{gs}) of T_PWM, $-V_{DATA\_PWM} + V_{TH\_PWM} +$ VSWEEP, reaches threshold, and T_PWM turns on. If so, the current flows out through T_PWM, and the stored voltage in C1 is discharged by the current. As a result, μLED stops emitting light. Since the proposed μLED pixel circuit uses the PWM driving method of discharging storage capacitor, not turning off the intermediate switching TFT, additional discharging stage is not needed.

III. SIMULATION AND DISCUSSION

For a reliable simulation of the proposed pixel circuit, we first fabricated 25 a-IGZO TFTs. After that, the median values of V_{TH}, mobility, and subthreshold swing (SS) were extracted from the measurement data of fabricated TFTs. These values were −0.68 V, 7.64 $cm^2/V{\cdot}s$, and 345 mV/dec, respectively. By fitting the parameters of the HSPICE RPI

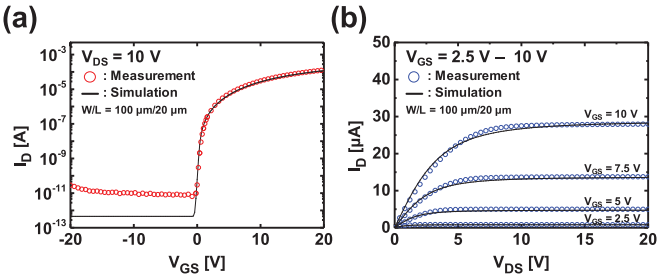

FIGURE 4. **Measured and simulated (a) transfer characteristic and (b) output curves of a-IGZO TFT with a size of 100 μm/20 μm.**

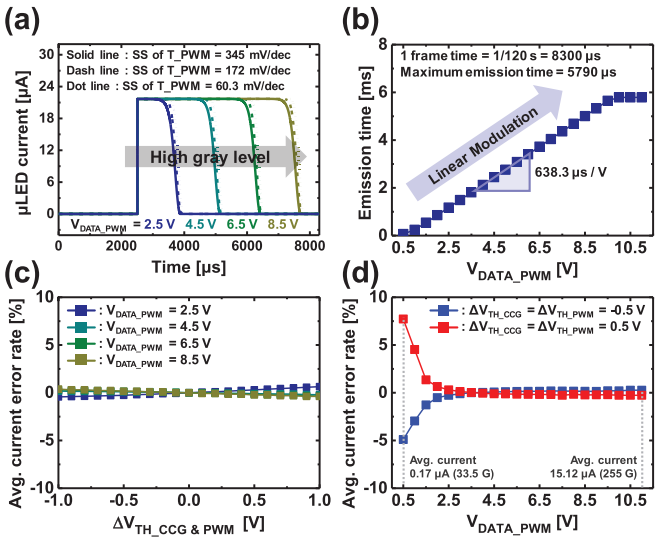

FIGURE 5. **(a) Simulated μLED current for different gray levels when SS of T_PWM is 345 mV/dec (solid line), 172 mV/dec (dash line), and 60 mV/dec (dot line). (b) Emission time according to V_{DATA_PWM}. (c) Average μLED current error rate according to the simultaneous change of V_{TH_CCG} and V_{TH_PWM} when V_{DATA_PWM} is 2.5, 4.5, 6.5, and 8.5 V. (d) Average μLED current error rate according to V_{DATA_PWM} when V_{TH_CCG} and V_{TH_PWM} are simultaneously changed by 0.5 V.**

TFT model library to these values, we developed a new oxide TFT model library. The measured and simulated transfer characteristic and output curves of the reference a-IGZO TFT with a size of 100 μm/20 μm are shown in Fig. 4. The off current in the measured data is about 10^{-11} A, because the lower measurement range of our experimental condition was limited due to the instrument resolution [22]. However, it has been reported that the off current of a-IGZO TFT is much lower than 10^{-11} A, so we modeled the off current as the conventional value [23], [24]. The coefficient of determination (R^2) between the measurement data and the simulated result is very high as 0.9999, confirming the highly reliable simulation.

The simulated μLED current of the proposed pixel circuit is shown in Fig. 5(a). The μLED emission period becomes longer as V_{DATA_PWM} increases, since a longer VSWEEP sweep range is required for V_{gs} of T_PWM to reach the threshold. Based on this result, we confirmed that the PWM driving of the proposed pixel circuit is properly implemented as intended. The emission time according to V_{DATA_PWM} is shown in Fig. 5(b). The emission time increases linearly as V_{DATA_PWM} increases, and the modulation rate is extracted to be about 638.3 μs/V. Therefore, the gray level can be adjusted very precisely since the emission time can be modulated in few μs unit. Also, we verified the compensation accuracy of the proposed circuit by calculating error rates of μLED current when V_{TH_CCG} and V_{TH_PWM} are simultaneously changed from 0.1 V to 1 V, with 0.1 V interval. The current error rates are shown in Fig. 5(c), and the maximum value is only 0.6% when V_{DATA_PWM} is 2.5 V.

In addition, error rates according to V_{DATA_PWM}, when V_{TH_CCG} and V_{TH_PWM} are changed by 0.5 V, are also calculated and plotted in Fig. 5(d). When V_{TH_CCG} and V_{TH_PWM} are changed in the same direction, the CCG compensation error causes a current level variation and the PWM compensation error causes an emission time variation, where each variation has the opposite effects on the average current. For example, if both V_{TH}s are increased in the positive direction, the CCG compensation error lowers the current level and the PWM compensation error increases the emission time. Then, the former decreases the average current and the latter increases the average current. Therefore, the total average current throughout all gray levels is determined by the combination of those two opposite effects.

However, the dominant effect can be differed depending on the gray level. In the high gray level where the emission time is long, the current level variation is the most important factor that causes luminance non-uniformity, so the effect of CCG compensation error is dominant. Whereas, as the gray level gets lower and the emission time gets shorter, the emission time variation grows into the most important factor of luminance non-uniformity, so the effect of PWM compensation error becomes more dominant. The error rate reversal in Fig. 5(d) also shows that the effect of PWM compensation error becomes stronger than that of CCG as V_{DATA_PWM} decreases. Meanwhile, as the emission time becomes shorter, the emission time difference due to the PWM compensation error accounts for a significant portion of the total emission time, and thus the absolute error rate increases inevitably. However, the proposed pixel circuit shows only a very small error rate of less than 10% even at the low gray level of about 33.5 G.

Here, the 33.5 G is the operation limit, where the emission time is almost the same as the falling time. Below the 33.5 G, the V_{DATA_PWM} is very small; thus, T_PWM is already turned on even before the emission stage. Hence, C1 is discharged as soon as the emission begins, causing the falling time reduction. Consequently, the emission time difference, the dominant effect of the error rate at the low gray level, is also reduced significantly. Due to these results, the current error rate below 33.5 G decreases as the gray level is lowered. However, this PWM operation below 33.5 G is different from the intended PWM driving by the proposed pixel circuit, so the current error rate in low gray levels was not analyzed in this paper. To overcome this issue, a new driving method will be required.

Meanwhile, the solid line of Fig. 5(a) shows a falling time of about 320 μs, which is slightly longer than the previous work using LTPS TFTs [8]. In order to control the falling time, the electrical property of TFTs should be optimized. We suggest that reducing the SS of T_PWM, the driving TFT of the PWM circuit, is the most effective optimization approach for reducing the falling time of the proposed pixel circuit. This is because the discharge delay of C1 is related to the subthreshold current of T_PWM. In other words, since T_PWM with low SS can flow a higher current at the same VSWEEP voltage right after it is turned on, C1 can be discharged faster with a smaller VSWEEP voltage. The shorter the VSWEEP sweep range between turning on T_PWM and discharging C1, the shorter the falling time to turn off the μLED.

The SS of the oxide TFT model used in the simulation is about 345 mV/dec, and it is higher than the SS of the typical LTPS TFT, about 200 mV/dec [25]. Hence, we decreased only the SS of T_PWM by adjusting parameter VTO and ETA, and verified the relationship between the falling time and the SS of T_PWM. If the SS of T_PWM decreases to about half of its value, the falling time is shortened to about 250 μs as shown in the dash line of Fig. 5(a). Also, if the SS of T_PWM decreases to theoretical minimum, the falling time is further shortened to about 220 μs as shown in the dot line of Fig. 5(a). From this result, we confirmed that more accurate PWM operation can be achieved in the a-IGZO TFT pixel circuit by optimizing the electrical property, such as SS. It is interesting that the SS optimization direction of μLED is different from that of OLED due to the difference in LED driving method. The high SS is desirable for OLED pixel circuits which modulate the amplitude of subthreshold current to precisely express low gray levels [26], [27], whereas the low SS is advantageous for μLED pixel circuits which modulate the width of emission time for the same operation.

IV. CONCLUSION

In this paper, we proposed an a-IGZO pixel circuit for active matrix μLED displays, which adopts PWM driving method to express gray levels without wavelength shift. The PWM driving operation and μLED current uniformity of the proposed pixel circuit were verified using HSPICE with an oxide TFT model based on measurement data. Simulation result showed that the proposed circuit can modulate the μLED emission period by adjusting PWM data, and can supply uniform current to μLED in spite of V_{TH} variation. Even though the V_{TH_CCG} and V_{TH_PWM} were simultaneously changed by 0.5 V, the maximum error rate in low gray level of 33.5 G was only about 7%. This small error rate confirmed that the proposed CCG and PWM circuit, which perform V_{TH} compensation and data input in the same stage, are not only efficient in reducing the layout size, but also effective in compensating for V_{TH} variation of TFTs. Since each circuit requires only one capacitor, the designed layout has a very small size of 96 μm × 294.3 μm, and thus the proposed pixel circuit can be applied to the modular type UHD displays of 55-inch or larger. In addition, we verified that PWM driving could be further improved by reducing SS of T_PWM. Based on this approach, we expect that the proposed μLED pixel circuit will achieve much higher performance than now by optimizing electrical property of a-IGZO TFTs.

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