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Impact of Channel Thickness on the NBTI Behaviors in the Ge-OI pMOSFETs With Al_2O_3/GeO_x Gate Stacks

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ABSTRACT The impact of channel thickness on the negative-bias temperature instability (NBTI) behaviors has been studied for the Germanium-on-Insulator (Ge-OI) pMOSFETs. It is found that the permanent and recoverable defects are generated simultaneously during the NBTI stress of Ge-OI pMOSFETs. The lower NBTI is confirmed for the Ge-OI pMOSFETs with a thinner channel, due to the reduction of the band bending of E_v under a fixed electrical field of NBTI stress. Thus, the channel thickness scaling could be an effective method to improve the NBTI reliability for Ge-OI pMOSFETs.

INDEX TERMS Germanium-on-Insulator (Ge-OI), metal-oxide-semiconductor field-effect transistor (MOSFET), negative-bias temperature instability (NBTI).

I. INTRODUCTION

Ge has been attracting a lot of interest as an alternative channel material for future CMOS technologies, especially for the pMOSFET applications due to its much higher hole mobility than that in Si [1], [2], [3]. Recently, high mobility Ge pMOSFETs have been demonstrated with superior electrical properties through the metal-oxide-semiconductor (MOS) interface passivation using either the Si capping layer or the GeO_2 interfacial layer [4], [5], [6], [7], [8], [9], [10]. These progresses suggest that Ge pMOSFETs are sufficiently mature and reproducible to warrant research into their reliability [11], [12], [13]. For Si-based CMOS technologies, negative-bias temperature instability (NBTI) degradation is the most severe reliability issue, since it results in a lifetime of pMOSFETs shorter than that of nMOSFETs [14], [15]. It has been found that the NBTI degradation in the Si-capped Ge MOSFETs is suppressed by using the Si-capping layer [12], [13], [16], [17]. However, the suppression of the NBTI degradation in the GeO_x interfacial layer passivated Ge pMOSFETs is still not sufficiently studied, which is one of the critical issues in the reliability improvement of Ge pMOSFETs.

Additionally, Germanium-on-Insulator (Ge-OI) is one of the most promising channel structures to improve the gate bias modulation and suppress the short channel effects in scaled Ge MOSFETs. The Ge-OI pMOSFETs have been realized with planar MOSFET and FinFET structures fabricated on Ge-OI substrates [8], [9], [18], [19], [20], [21], [22], [23], [24]. Superior electrical properties have been realized for these devices, thanks to the high hole mobility in the channels [19], [25], [26], [27], [28]. These results promote the applicability of Ge-OI pMOSFETs in future CMOS technologies. Thus, the examination of the NBTI behaviors in Ge-OI pMOSFETs is important.

In this study, the NBTI behaviors in the Ge-OI pMOSFETs are examined, and the impact of the channel thickness on the NBTI reliability of Ge-OI pMOSFETs has been investigated. It is found that the Ge-OI pMOSFETs with a thinner channel thickness represent a lower NBTI, suggesting the scaling down of channel thickness is

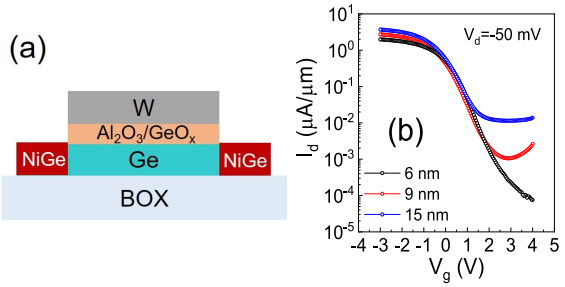

FIGURE 1. **(a): The schematic map of the device structure of the Ge-OI pMOSFETs; (b): The I_d-V_g characteristics of a Ge-OI pMOSFET with the channel thickness of 6 nm.**

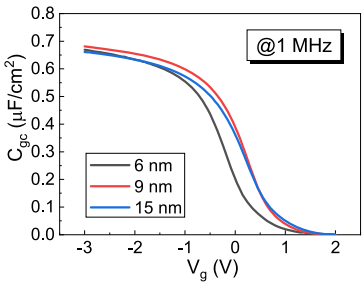

FIGURE 2. **The C_{gc}-V_g curves of the Ge-OI pMOSFETs with different channel thicknesses of 6, 9 and 15 nm.**

effective in the enhancement of NBTI reliability for Ge-OI pMOSFETs.

II. EXPERIMENTAL

The device structure of the Ge-OI pMOSFETs is shown in Fig. 1 (a). The Smart-Cut Ge-OI (undoped, (100) orientation, 140 nm buried oxide (BOX)) substrates were used to fabricate the Ge-OI pMOSFETs. The Ge-OI substrate was trimmed to 6-, 9- and 15-nm-thick by 550 °C thermal oxidation, followed by the wet etching of the GeO_2 layer. The Ge layers in these Ge-OI substrates are fully-relaxed. The Al_2O_3 (10 nm)/GeO_x (0.3 nm)/Ge gate stack was fabricated with ozone post oxidation [29]. The capacitance equivalent thickness (CET) of the Al_2O_3/GeO_x gate stack is evaluated from C_{gc} curves (Fig. 2) with eliminating the parasitic capacitance. The CET is ~5.1 nm for all Ge-OI pMOSFETs. It has been confirmed that the Al_2O_3/GeO_x gate stack exhibits a superior MOS interface quality with a low interface trap density of $\sim 3\times10^{11}$ $cm^{-2}eV^{-1}$ (data not shown) [30], [31], [32]. The post deposition annealing was carried out at 400 °C for 30 min in N_2 ambient. The tungsten (W) was deposited by sputter as the gate metal. After the gate metal patterning and gate stack etching, the self-aligned NiGe metal S/D structures were fabricated by Ni deposition and metallization annealing at 400 °C for 1 min. Subsequently, the unreacted Ni was removed by HCl etching. Finally, the Ni contact pads were deposited for the gate and S/D, and the Al back contact was deposited.

III. RESULTS AND DISCUSSION

A. DEVICE CHARACTERIZATIONS

It is observed in Fig. 1 (b) that the 6-nm-thick Ge-OI pMOSFET shows the p-channel MOSFET operation with

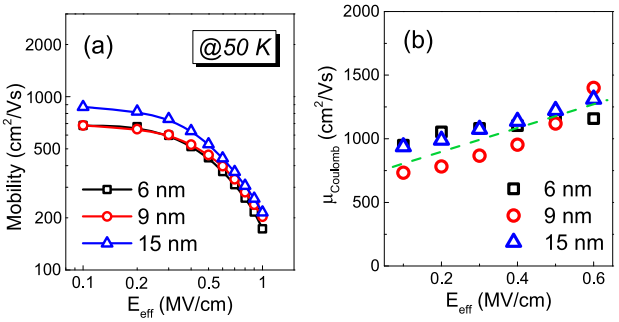

FIGURE 3. **(a): The low temperature mobility (@50 K) and (b): The Coulomb scattering limited mobility in the Ge-OI pMOSFETs with different channel thicknesses of 6, 9 and 15 nm.**

an ON/OFF ratio of $\sim 10^5$. The normal operation has also been confirmed for the 9- and 15-nm-thick Ge-OI pMOSFETs. The large I_d of ~2 μA/μm is obtained for the 6-nm-thick Ge-OI pMOSFETs at $V_g - V_{th} = V_d = -50$ mV with the gate length of 10 μm and the *CET* of 5 nm. These results indicate a small interface defect density for the initial Ge-OI pMOSFETs during the NBTI investigation in this study. The wave function penetration into gate oxide for hole varies in Ge-OI pMOSFETs with different channel thicknesses, which may result in change of NBTI behaviors. Since the wave function penetration effect decreases with increasing the gate oxide thickness [33] and the Ge-OI pMOSFETs feature sufficiently thick, the wave function penetration effect is neglected in this study.

$$\frac{1}{\mu_{Coulomb}} = \frac{1}{\mu_{total}} - \frac{1}{\mu_{fluctuation}} - \frac{1}{\mu_{sr}} \quad (1)$$

It is noted that the MOS interface quality exhibits a remarkable impact on the bias temperature instability (BTI) properties in MOSFET devices. The MOS interface properties were examined for Ge-OI pMOSFETs, with different channel thicknesses of 6, 9 and 15 nm. Fig. 3 (a) shows the low temperature mobility in Ge-OI pMOSFETs measured at 50 K, where the impact of phonon scattering is eliminated. The Coulomb scattering limited mobility ($\mu_{Coulomb}$) was extracted using the Matthiessen's rule as shown in equation (1) [34]. It is found that the 6-, 9- and 15-nm-thick Ge-OI pMOSFETs show almost the same $\mu_{Coulomb}$ (Fig. 3 (b)), indicating that devices with three different channel thicknesses have similar MOS interface quality and thus the NBTI behavior in the Ge-OI pMOSFETs would be dominated by channel thickness.

B. IMPACT OF ELECTRICAL FIELD

In order to evaluate the NBTI behaviors in the Ge-OI pMOSFETs, the devices with gate length of 10 μm and channel width of 5 μm were employed. The NBTI test was carried out at room temperature following the standard stress-and-sense procedure [35], with a DC gate bias stress (V_g) for stress phase and V_g=0 V for recovery phase. Here the measurement delay of 10 ms was used for the NBTI stress and recovery measurements. To monitor the threshold voltage (V_{th}), the V_g stress was periodically interrupted and the I_d-V_g curve was

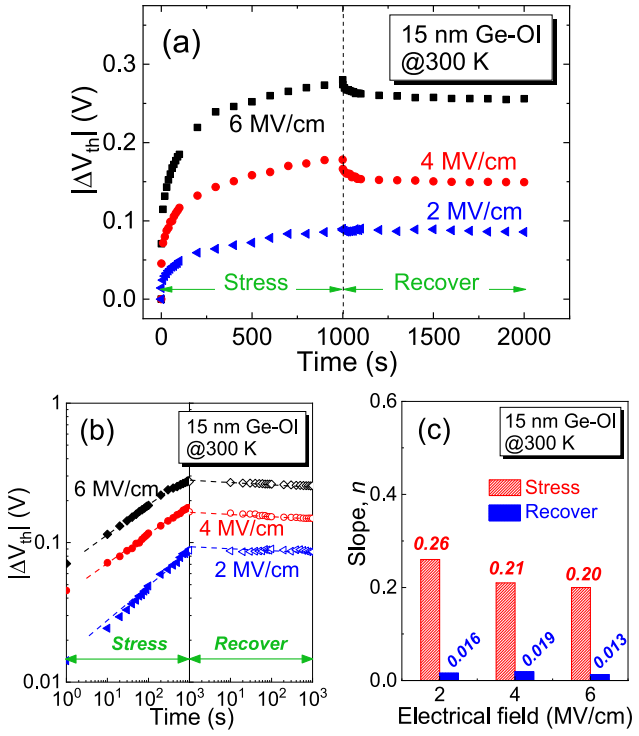

FIGURE 4. (a) and (b): The V_{th} shift with different NBTI stress times and recover times for the Ge-OI pMOSFET having the channel thickness of 15 nm with different NBTI stresses E_{ox} of 2, 4 and 6 MV/cm. (c): The slope n for the ΔV_{th} – time relationship in a power law.

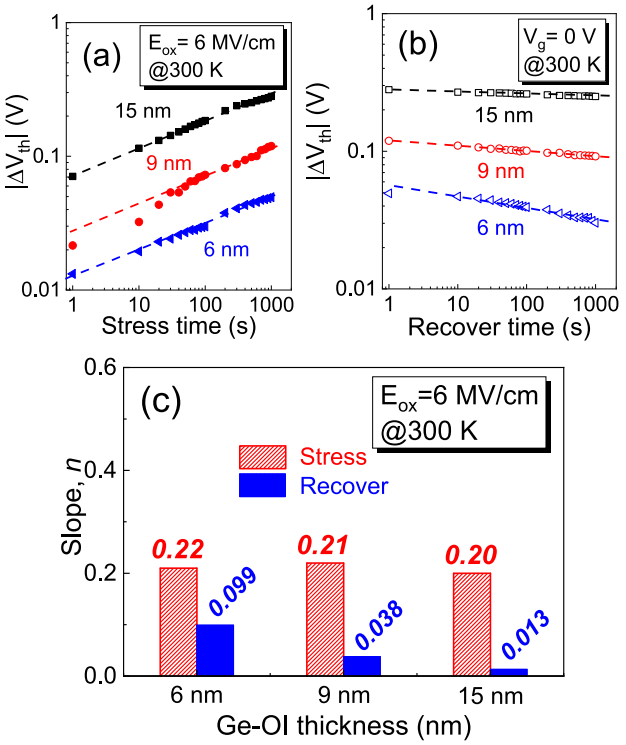

FIGURE 5. The ΔV_{th} with different NBTI stress times (a) and recover times (b) for the Ge-OI pMOSFETs with different channel thicknesses of 6, 9 and 15 nm. The NBTI stress is fixed at E_{ox}=6 MV/cm. (c): The slope n for the ΔV_{th} – time relationship in a power law.

recorded under a V_d of −100 mV. The NBTI behaviors of the Ge-OI pMOSFETs were evaluated at various gate bias with different electrical field (E_{ox}). The E_{ox} was calculated from $|V_g\text{-}V_{th}|/CET$. The V_{th} recovery was performed at V_g=0 V for all devices. Since the V_{th} difference in these Ge-OI pMOSFETs is minor (−0.28, −0.15 and −0.11 V for 6-, 9- and 15-nm-thick channels) and the gate stacks for these devices are relatively thick, the electrical field difference in these devices at V_g=0 V is ignored. Fig. 4 shows the NBTI degradation and recovery characteristics in the 15-nm-thick Ge-OI pMOSFETs. It is found in Fig. 4 (a) that the V_{th} exhibits a remarkable shift during the stress region for all E_{ox}, attributable to the defect generation in the gate stack. However, the threshold voltage shift (ΔV_{th}) is significantly weaker in the recovery region than that in the stress region. This result suggests that the ΔV_{th} during the stress region for the Ge-OI pMOSFETs is contributed by both recoverable and permanent defects. The similar phenomenon was also observed for the Ge MOSFETs fabricated on bulk-Ge substrates [36].

$$\Delta V_{th} = k \cdot t^n \tag{2}$$

The V_{th} shift for the Ge-OI pMOSFETs is plotted with a log-scale figure (Fig. 4 (b)), and the exponent n values are extracted according to equation (2). Here the n values are employed to compare the defect generation and recovery rate during the stress and recover regions. It is found that the n values for Ge-OI pMOSFETs during stress with all E_{ox} values are significantly larger than those during recovery regions (Fig. 4 (c)), indicating the remarkable generation of permanent fix charges for Ge-OI pMOSFETs during NBTI stress.

C. IMPACT OF CHANNEL THICKNESS

The impact of channel thickness on the NBTI behaviors for the Ge-OI pMOSFETs has been examined and shown in Fig. 4. The parallel shift of the power law between ΔV_{th} and stress time refers to the same charge traps generation behaviors for all the Ge-OI pMOSFETs (Fig. 5 (a)). The n values are comparable for Ge-OI pMOSFETs with all channel thicknesses, indicating a similar defect generation behavior for all devices originated from the electrical and material properties of the Al_2O_3/GeO_x gate stack. Additionally, the 15-nm-thick Ge-OI pMOSFETs show much larger ΔV_{th} than those in 9- and 6-nm-thick Ge-OI pMOSFETs. Under an NBTI stress of E_{ox}=6 MV and stress time of 1000 s, the ΔV_{th} of ~280 mV is observed for the 15-nm-thick Ge-OI pMOSFETs. In contrast, the ΔV_{th} is significantly reduced to ~50 mV for the 6-nm-thick Ge-OI pMOSFETs. Since these Ge-OI pMOSFETs feature the same gate stack, the different NBTI degradations are attributable to the physical structure of the Ge-OI pMOSFETs. Fig. 5 (b) shows the ΔV_{th} in Ge-OI pMOSFETs in the recovery region after 1000 s' stress at E_{ox}=6 MV/cm. The same amount of recovery has been confirmed in each decade for all Ge-OI pMOSFETs, which is consistent with the common sense of NBTI recovery behaviors.

The electrical field and the band diagram were examined to investigate the physical origin of the suppressed NBTI

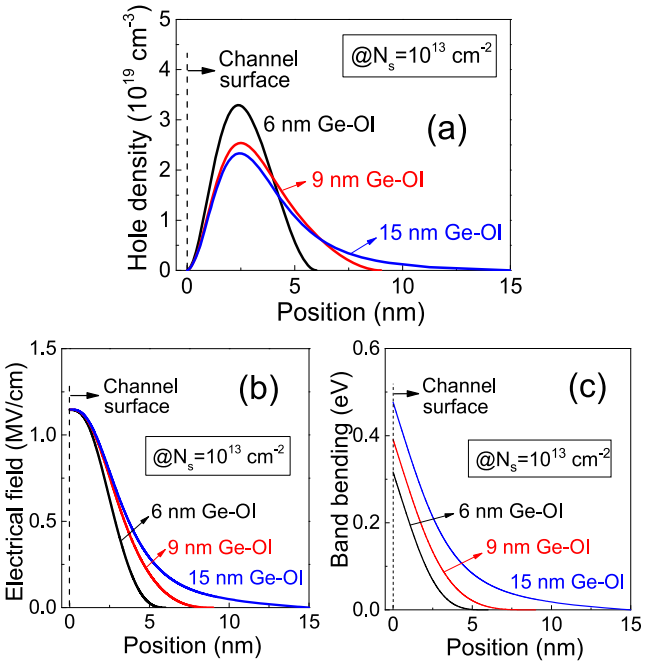

FIGURE 6. The hole distribution (a), the electrical field (b) and the valence band energy (c) in the Ge-OI pMOSFETs with different channel thicknesses of 6, 9 and 15 nm, under a fixed N_S of 10^{13} cm^{-2}.

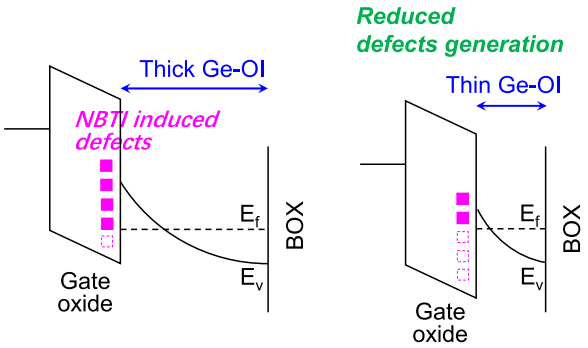

FIGURE 7. The schematic map of the physical origin for the suppressed NBTI in the Ge-OI pMOSFETs with a thinner channel thickness.

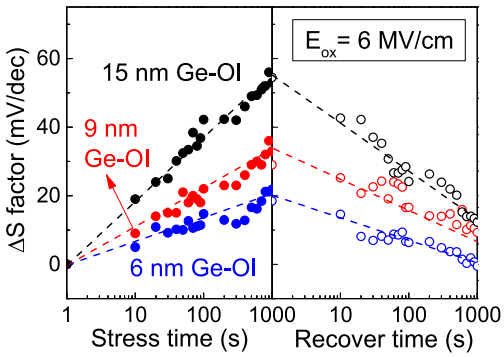

FIGURE 8. The ΔS factors as functions of stress time and recover time in the Ge-OI pMOSFETs with different channel thicknesses of 6, 9 and 15 nm, under a fixed NBTI stress of E_{ox}=6 MV/cm.

degradation in the thinner Ge-OI pMOSFETs. Fig. 6 (a) shows the hole distribution in the Ge-OI channels with different thicknesses, by solving the 1-dimensional Schrödinger-Poisson equations. The accuracy of the Schrödinger-Poisson solution has been confirmed by comparing the equivalent oxide thickness (EOT) value of the gate stack obtained by experimental C-V curve (~4.87 nm) and by theoretical calculation (4.79 nm) using permittivity of gate insulator (k(GeO_x): 5.5, k(Al_2O_3): 8.5). The surface charge density (N_s) of 10^{13} cm^{-2} is used for simplicity. As a result, the electrical field and the energy change of valence band (ΔE_v) are evaluated and shown in Fig. 6 (b) and (c), respectively. The same electrical field is obtained at the channel surface for different Ge-OI thicknesses of 6, 9 and 15 nm. On the other hand, the thinner Ge-OI channel exhibits a smaller band bending of E_v with the same N_s, suggesting a decrease of the accessible defect band during NBTI stress. Thus, the physical mechanism of the suppressed NBTI degradation in the thin Ge-OI pMOSFETs can be interpreted in Fig. 7 [37], [38]. The defects generated during NBTI of Ge-OI pMOSFETs are composed of permanent defects and recoverable defects, located either near MOS interface or deeper within the gate stack, resulting in an unrecoverable ΔV_{th}. Additionally, because of the reduced band bending in the thinner Ge-OI channel, the Fermi level E_f at the MOS interface is closer to the E_v of Ge and leads to a narrower accessible defects band. Therefore, the amount of defects generated by NBTI stress is suppressed in the Ge-OI pMOSFETs with a thinner channel thickness.

On the other hand, it is also observed in Fig. 5 (b) that all the Ge-OI pMOSFETs do not show the fully recovery of the V_{th} shift due to the NBTI stress. The Ge-OI pMOSFETs with thinner channels represent larger n values during the recovery phase (Fig. 5 (c)). The n value increases from 0.013 to 0.038 and 0.099 with decreasing the Ge-OI channel thickness from 15 to 9 and 6 nm. This phenomenon suggests that the proportion of recoverable defects is larger for the thinner channel Ge-OI pMOSFETs. Since the E_v band bending is smaller for the 6-nm-thick Ge-OI pMOSFETs than the 9- and 15-nm-thick devices, the possible mechanism for the larger n value during recovery is that the recoverable defects are more pronounced at the energy nearer to the valence band edge.

D. PHYSICAL MECHANISM OF SUPPRESSED NBTI

The NBTI stress-induced defects resulting in the V_{th} shift for the Ge-OI pMOSFETs could be fix charge and interface traps. In order to clarify the nature of NBTI stress induced defects for the Ge-OI pMOSFETs, the sub-threshold slopes (S factors) were characterized as functions of NBTI stress and recover time. It is noted that the measurement method in current study may cause a slight V_{th} difference for each point in I_d-V_g curve and lead to a voltage sweeping rate related error for S factor evaluation. However, this effect is neglected because the S factor in current Ge-OI devices is relatively large (~490 mV/dec). As shown in Fig. 8, the S factor increases for Ge-OI pMOSFETs by elongating the stress time, attributing to the generation of MOS interface traps. The larger S factor increase is confirmed for the Ge-OI

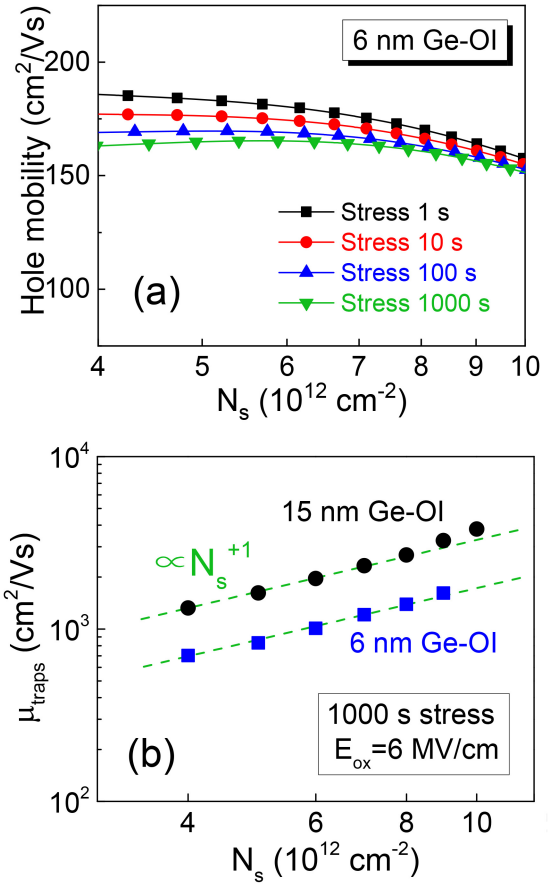

FIGURE 9. **(a): The hole mobility in the 6-nm-thick Ge-OI pMOSFETs after different NBTI stress time with an E_{ox}=6 MV/cm. (b): The mobility limited by the NBTI induced interface traps (μ_{traps}) for 6- and 15-nm-thick Ge-OI pMOSFETs after 1000 s stress at E_{ox}=6 MV/cm.**

pMOSFETs with thicker channel thicknesses. With an electrical stress of E_{ox}=6 MV/cm, the S factor increases by ~60 mV/dec for the 15-nm-thick Ge-OI pMOSFET, and the 6-nm-thick Ge-OI pMOSFET exhibits an S factor increase of ~20 mV/dec. This phenomenon is similar to the ΔV_{th} result shown in Fig. 5 that the degradation of electrical properties is stronger in Ge-OI pMOSFETs with thicker channels, due to the increased band bending with an increase of channel thickness. This conclusion is also supported by the hole mobility in the Ge-OI pMOSFETs after the NBTI stress. The hole mobility of the Ge-OI pMOSFETs are calculated with equation (3). Fig. 9 (a) shows the hole mobility in the 6-nm-thick Ge-OI pMOSFET after NBTI stress at E_{ox}=6 MV/cm, as a function of inversion carrier density (N_s). It is found that the hole mobility decreases with increasing the stress time, attributable to the increase of interface traps. A similar mobility degradation behavior is also observed for the 9- and 15-nm-thick Ge-OI pMOSFETs. The Matthiessen's rule has been employed to evaluate the mobility limited by the NBTI-induced interface traps (μ_{traps}), as illustrated in equation (4). Here the μ_{before} and μ_{after} refer to the hole mobility before and after the NBTI stress. Fig. 9 (b) shows the μ_{traps} for 6- and 15-nm-thick Ge-OI pMOSFETs after

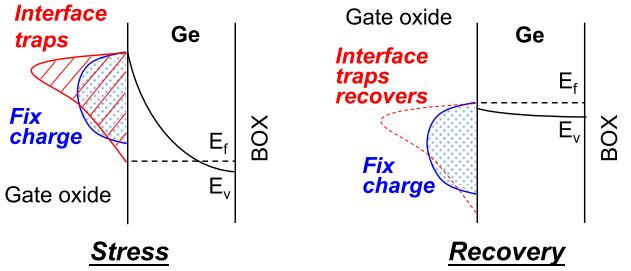

FIGURE 10. **The schematic map of the defect generation and recover behaviors in the Ge-OI pMOSFETs with Al_2O_3/GeO_x gate stack during NBTI stress and recovery phases.**

1000 s stress at E_{ox}=6 MV/cm. It is confirmed that the μ_{traps} are proportional to N_s^{+1} for both devices, following the behavior of Coulomb scattering [39]. This phenomenon is a strong evidence that the NBTI results in a generation of interface traps. The μ_{traps} for 6-nm-thick Ge-OI pMOSFET is much lower than that for 15-nm-thick device, suggesting an increased interface traps generation in Ge-OI pMOSFETs with thicker channels. This result is consistent with the S factor change represented in Fig. 8.

$$I_d = \mu C_{ox} \frac{W}{L}\left(V_g - V_{th} - \frac{V_d}{2}\right)V_d \tag{3}$$

$$\frac{1}{\mu_{after}} = \frac{1}{\mu_{before}} + \frac{1}{\mu_{traps}} \tag{4}$$

Meanwhile, it is interestingly noted in Fig. 8 that the S factor increases after the NBTI stress and fully recovers during the NBTI recovery phase for all the Ge-OI channel thicknesses, which is inconsistent with the ΔV_{th} shown in Fig. 5 (a). This phenomenon indicates that the NBTI stress induced MOS interface traps are recoverable and the permanent defects behave as the fix charge in the Ge-OI pMOSFETs. Therefore, the defects generation behavior during NBTI for the Ge-OI pMOSFETs with Al_2O_3/GeO_x gate stack is illustrated in Fig. 10. Both fix charge and MOS interface traps are generated within the NBTI stress phase for the Ge-OI pMOSFETs. And during the recovery phase, the MOS interface traps can be recovered (or mostly recovered). Considering the different defect recovery rates induced by the n factor (in Fig. 5 (c)), the MOS interface traps density may be larger near the valence band edge. In contrast, the fix charge appears to be permanent defects in the gate stack, resulting in an unrecoverable ΔV_{th}.

IV. CONCLUSION

In summary, the NBTI behaviors of the Ge-OI pMOSFETs are investigated in this study. It is found that the defects generated during NBTI are composed of permanent defects and recoverable defects, where the recoverable defects show a possible nature of MOS interface traps and the permanent ones could be fix charge. Additionally, the weaker NBTI is confirmed for the Ge-OI pMOSFETs with the thinner channel, attributable to the reduced band bending under a fixed electrical field of NBTI stress. A feasible approach

has been indicated to improve the NBTI reliability for Ge-OI pMOSFETs by scaling down the channel thickness. the effectiveness of ultra-thin-body Ge-OI pMOSFETs in future CMOS technology.

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