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Ultrafast $I_D - V_G$ Technique for Reliable Cryogenic Device Characterization

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ABSTRACT An in-depth understanding of the transient operation of devices at cryogenic temperatures remains experimentally elusive. However, the impact of these transients has recently become important in efforts to develop both electronics to support quantum information science as well as cryogenic high-performance computing. In this paper, we discuss a fast time-dependent device characterization technique, capable of examining the charge trapping dynamics of devices operating at cryogenic temperatures. Careful calibrations allow for the acquisition of accurate fast I-V and transconductance transients down to 20 ns for devices operating down to 8 K. The trap charging dynamics was monitored via shifts in both threshold voltage and transconductance. The combination of fast measurements and cold temperatures were used to shift the observable measurement window to reveal charge trapping/de-trapping time dynamics of both fast and slow traps in high-k devices to demonstrate the utility of the fast I-V for cryogenic device characterization.

INDEX TERMS Cryogenic-CMOS, fast I-V, transient device characterization, quantum electronics.

I. INTRODUCTION

Recent large-scale infrastructural investments in quantum information science has spawned a renewed interest in cryogenic device operation. Scaling up quantum systems require the development of low-power cryogenic analog and digital electronics to control, manipulate, and detect the fragile quantum state variables. The cryogenic environment (4 K – 77 K) greatly modifies the underlying device physics and the consequent parametric shifts must be accommodated in circuit designs. Considering that the current understanding of modern device physics is largely based on characterizations over a relatively small temperature range (295 K – 395 K), it is unsurprising that cryogenic characterizations reveal interesting deviations from the expected extrapolated device behavior [1], [2], [3].

Typical cryogenic device characterizations involve quasi-static measures of current and voltage that are used to create cryogenic device models and subsequent cryogenic circuits [1], [2], [3]. Some efforts have even included limited frequency-domain characterizations to further improve the modeling accuracy [4]. These comprehensive quasi-static DC and frequency-domain characterizations do occasionally yield functioning digital circuits with minor adjustments to operating voltages. However, functional cryogenic analog circuitry is far less common [5], due to inadequate cryogenic device characterizations and analog circuit's known susceptibility to time and temperature dependent parametric fluctuations.

Accurate time-domain device characterizations in the range from ns to μs are essential toward building accurate device models as well as tracking a wealth of reliability concerns [6], [7], [8], [9] spanning charge trapping to self-heating. When designing analog circuits like the DC converters, ADC/DAC and low noise amplifiers used for signal detection in quantum computers, accuracy of the modeling parameters such as the threshold voltage, capacitance, mobility etc. are important for reliable working of these circuits. Imprecisions in these parameters in a device model would

lead to unknown time/frequency dependent performance of the circuits such as inaccurate frequency dependent amplifier gain [9]. Especially at low temperatures due to the increased SS, a small change in the threshold voltage would lead to significant change in the operating current [10]. So, care must be taken to ensure the extracted parameter is correct when designing the circuits. There are some measurements done to address this problem by using frequency measurements, but the time domain measurements will give more information about the devices [9]. Exertions to unravel this complicated confluence at cryogenic environments and precise fast time-domain characterizations are rare [7] and non-trivial [8]. A novel idea of using a warm (310 K) amplifier close to the device for cold (<8 K) measurements is proposed and experimental hurdles to achieve accurate and reliable measurements with this unconventional setup with warm amplifier inside a cryostat is described in this paper.

This unique ultrafast I-V platform for device characterization at cryogenic temperatures can capture fast I-V transients ($\geq$ 20 ns rise/fall times (RT/FT)) in a cryogenic probe station with sufficient accuracy for reliable threshold voltage (V_t) and transconductance (g_m) extraction. The experimental platform is used to measure the charge trapping/de-trapping transients in hafnium oxide-based devices. We show that the cryogenic environment and the fast measurement speed combine to shift the charge trapping/de-trapping kinetics to reveal components which are normally obscured in typical slower room temperature characterizations. Though only bulk CMOS devices are used in this paper, the utility of this platform can easily extend to other lower power device technologies which are being considered for quantum computing applications [11], [12].

II. EXPERIMENTAL SETUP

Throughout this work, extensive measurements were performed on conventional planar Si/SiO_2 n-channel metal oxide semiconductor field effect transistors (nMOSFETs) from a 180 nm technology (t_{ox} = 3.5 nm). Careful measurements of the Si/SiO_2 devices allowed for validation of the fast characterization platform for all temperatures and measurement speeds. Subsequent measurements on 1 nm SiO_2 / 3 nm HfO_2 nMOSFETs with measured CET (capacitance equivalent thickness [13]) of 2 nm were then performed to demonstrate the technique's capability by examining the measurement time and temperature-dependent hysteresis in the drain current (I_D) characteristics.

The experimental setup for the fast acquisition of the I_D turn-on/off transients in response to a gate voltage (V_G) pulse (fast I-V) is shown in Fig. 1a. In this arrangement, a voltage pulse is applied to the gate terminal (V_G) through a probe which is 50 Ω terminated very near the tip to minimize reflections. All signal grounds are shorted near the probe tips to minimize signal integrity distortions. The V_G pulse is monitored using a pick-off tee, which captures the waveform created by the generator as well as any distortions in the signal. A typical V_G pulse is shown in Fig. 1b

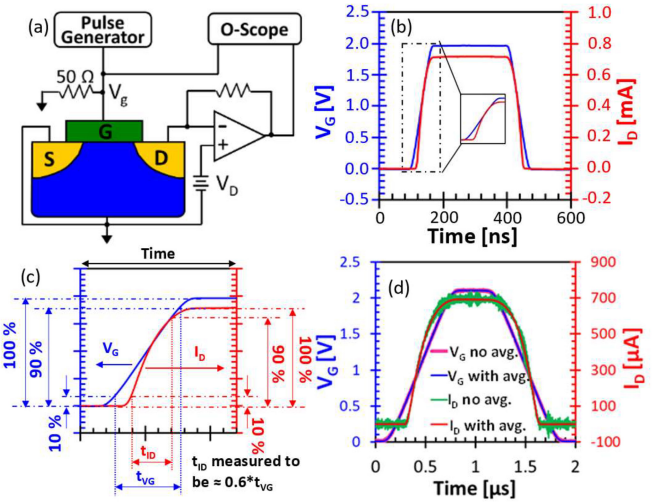

FIGURE 1. (a) Setup for single pulse fast-IV measurement. b) A typical time domain fast-IV for 10 μm x 0.18 μm Si/SiO_2 nMOSFET using pulse with RT/FT of 50 ns and pulse width of 300 ns at 300K. V_D = 50 mV, inset: rising edge of I_D and V_G. c) Calculation of rising edge of I_D(t_{ID}) compared to the rising edge of V_G(t_{VG}), t_{ID} was obtained to be ≈ 60% of t_{VG}. d) Time domain data for $V_G$and I_D with and without averaging (1000 samples) of the data points with RT/FT of 1 μs.

which confirms the signal integrity of the gate pulse. A custom built transimpedance amplifier (TIA, using operational amplifier (op-amp) OPA 695) was used to measure the I_D response, like the setup discussed in [14], [15]. Both I_D and V_G are monitored by a high-resolution digital oscilloscope. A typical room temperature time domain fast I-V response is shown in Fig. 1b for reference. Note that the rising and the falling edges (time taken to change from 10% to 90% of the maximum value) for the I_D are shorter than that for V_G, consistent with the $I_D - V_G$ characteristics of a MOSFET (rising edge highlighted in the inset of Fig. 1b). This shorter rising time of the current compared to the applied voltage implies that RT/FT of the current is shorter than that of the applied V_G. Detailed procedure of approximation of the rising edge of I_D (t_{ID}) compared to the rising edge of V_G (t_{VG}) is shown in Fig. 1c. The data for Fig. 1b and c were obtained by averaging 1000 samples. Comparison of single shot measurements with 1000 averaging in Fig. 1d is shown to verify that the setup is stable for obtaining reliable averaged data. Such verification is done for all the measurements here after where averaging is done.

The gain of the TIA is 250 V/A and the drain voltage (V_D) is applied through the non-inverting terminal of the TIA (Fig. 1a). The custom TIA was utilized to avoid the 50 Ω input impedance present in most commercial high-speed amplifiers as well as the input of the oscilloscope which becomes problematic in direct fast I-V acquisition schemes [8]. In both cases, the 50 Ω resistance introduces an unintended drain voltage drop as the channel resistance becomes comparable to 50 Ω. The resultant V_G-dependent drain bias modification is a common issue encountered in high-speed measurements [8] and the required deconvolution greatly complicates analysis. The low input impedance of

the TIA in Fig. 1a eliminates the drain bias convolution [14], [15]. However, the same low input impedance introduces an unavoidable mismatch with the coaxial transmission line. This mismatch introduces large reflections which distort the measured I_D transient. These reflections cannot be avoided, but their impact can be minimized by reducing the time (distance) between the mismatch points (device and the TIA). In this study, the amplifier is placed within $\approx$ 5 cm of the I_D probe tip. This corresponds to a 500 ps round trip propagation time in coaxial transmission lines, (10 cm /(2x10^{10}cm/s) = 500 ps). Since this effort prioritizes the capture of accurate fast current transients, we only tolerate signal distortions within 5% of signal rise time (this is much more stringent than the commonly accepted 20%) [16]. Thus, this approach will be able to track the I_D transient response $\approx$ 10 ns (500 ps being 5% of 10 ns). As observed in Fig. 1b and c, the rising and falling edges of I_D transient is faster than that of V_G. Using information in Fig. 1c we empirically determine that for the devices in this study, 10 ns of t_{ID} corresponds to t_{VG} of 16 ns. To ensure the accuracy of the measurements we have restricted our rising edge of V_G to be >20 ns so that the rising edge of the current being measured does not go below the limit (10 ns) of the measurement setup.

Experimental implementation of a TIA-based fast I-V setup entails mitigation of several factors which can act to distort the transient responses. These factors include the amplifier's 'output DC offset' (due to input offset voltage and input bias current of the op-amp) and displacement current (I_{dis}) [17]. Fig. 2a illustrates the raw I_D response to a V_G pulse in which all probes are lifted off the device. In this example measurement, we observe a DC offset current of $\approx$ 105 μA. In addition to the DC current, Fig. 2a also illustrates the I_{dis} at the rising and falling edges of the V_G pulse. Somewhat surprisingly, the dominant I_{dis} ($I_{dis} = C_p\ (dv/dt)$) in this setup is the parasitic capacitance (C_p) between adjacent probe tips. This was confirmed by measuring current as shown in Fig. 2 using same probe and setup but with current measuring probe at various distance from the gate probe. The results showed that there was measurable change in parasitic current dependent on probe location suggesting the capacitance between the probes being dominant. The I_D transients in Fig. 2a can be viewed as an experimental background which can be subtracted from the subsequent fast I-V measurements to yield the corrected $I_D - V_G$ plot of Fig. 2b. Difference between I-V plots with and without background subtraction is shown in Fig. 2c. The current distortions below 10 μA are due to the limited sensitivity of the amplifier. Details of the sensitivity of the amplifier setup are explained later in this section. The similarity of the $I_D - V_G$ curves for the rising and falling edges confirms that the I_{dis} correction for the setup is the dominant contributor and the gate to channel/source/drain C_p is negligible for these devices. The correction is minimal in this example. However, faster RT/FT in lower current devices leads to significant distortions to the measurements which must be corrected.

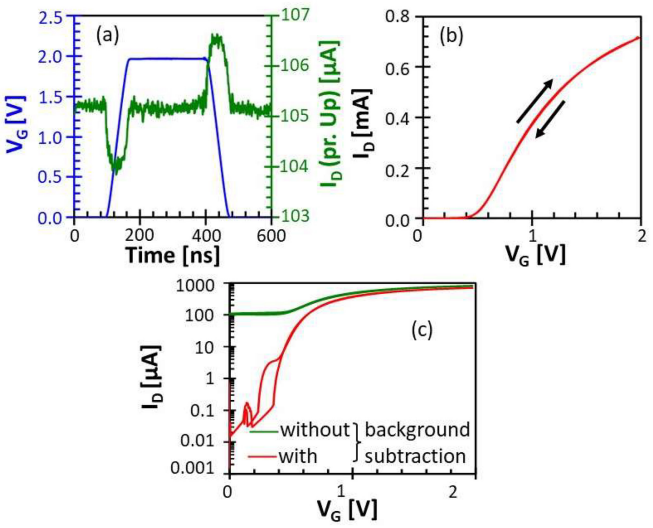

FIGURE 2. (a) Raw V_G and I_D (probes lifted up) versus time traces illustrating the offset and displacement current experimental backgrounds. b) $I_D - V_G$ plot with background subtraction. c) Semi-logarithmic $I_D - V_G$ plot with and without background subtraction. Device: W x L = 10 μm x 0.18 μm, Si/SiO_2 nMOSFET and 50 ns RT/FT at 300K, V_D = 50 mV.The corresponding time responses of V_G and I_D are shown in Fig. 1b.

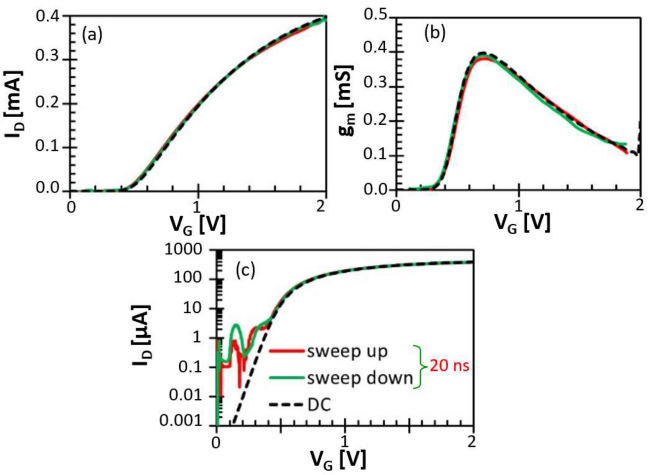

FIGURE 3. (a) $I_D - V_G$ measured with 20 ns(— sweep up, — — sweep down) RT/FT and DC(– –) using a parameter analyzer. b) Corresponding $g_m - V_G$ illustrating excellent agreement. c) $I_D - V_G$ plotted on a logarithmic scale illustrating the lower bounds of sensitivity (~ 5 μA). Device: W x L = 10 μm x 0.36 μm, Si/SiO_2 nMOSFET, 20 ns RT/FT at 300K, V_D = 50 mV.

The experimental approach described above was implemented in a series of room temperature measurements which show excellent agreement between 20 ns fast I-V measurements and those taken by using a conventional quasi-DC parameter analyzer (Fig. 3a). This agreement is also notably observed in the corresponding transient g_m measurements (Fig. 3b). The close correspondence between the DC and fast-g_m curves are an indication of minimal distortion given its sensitivity to measurement artifacts and establishes the reliability of the fast I-V measurement for reliable device characterization [14]. Throughout this work, the parameterization of device transients relies on these precise g_m

measurements to facilitate consistent V_t extraction (using linear extrapolation of $I_D - V_G$ to $I_D = 0$ at the maximum slope point (max g_m)). When plotted on a logarithmic scale, the fast I-V curves exhibit close agreement down to ≈ 5 μA (Fig. 3c). The lower limit on current depends on the gain bandwidth product and the input bias current of the chosen op-amp. In these measurements, speed was prioritized over sensitivity. However, if higher sensitivity is desired (i.e., sub-threshold swing measurements), different op-amps with reduced input bias current could be used to increase the gain at the cost of measurement speed. More elaborate multi-stage amplification is also possible. Low repetition rate fast I-V measurements were averaged to minimize noise. Each fast I-V measurement consists of $\approx$ 1000 averages. Careful analysis of the rising edge of consecutive $I_D - V_G$ transients helped establish the necessary delay times between pulses ($V_G = 0$ V) to ensure no residual artifacts due to charge trapping, self-heating, etc. for temperature ranging from 300 K down to 8 K. To avoid such artifacts, duty cycle ratios were $< 10^{-4}$ for both the high-k and SiO_2 devices and all the temperatures used for measurements.

Incorporation of this fast I-V experimental approach into a cryogenic environment unsurprisingly introduces further complications. The requirement to minimize the distance between the TIA and the probe tip dictates that the TIA must be located *within the cryogenic environment*. However, many of the amplifier characteristics (gain, offset, etc.) are temperature dependent. To avoid this unruly temperature dependence, we have modified a cryogenic probe station to include an internal heated stage to maintain the TIA at an elevated temperature (310 K) while the remainder of the probe station and devices can be cooled to cryogenic temperatures (Fig. 4a). Maintaining the TIA at 310 K introduces a heat load which somewhat elevates device temperatures depending on the thermal conductance between the device and the cold chuck which varies from device to device. To avoid this variable heat load, the chuck is actively heated to maintain a base temperature of about 8 K (sometimes somewhat higher based on the device to chuck thermal resistance). We observe that this moderate increase to the system base temperature results in a remarkably stable thermal environment. Fast I-V and the corresponding fast-g_m measurements on the Si/SiO_2 devices confirm the validity of this experimental approach for RT/FT ranging from 20 ns to 1 ms at 300 K, 80 K and 8 K compared to generic DC measurements done using parameter analyzer (Fig. 4b and Fig. 4c). This identical fast $g_m - V_G$ curve for various RT/FT ranging from 20 ns to 1 ms with DC shown in Fig. 4c is a significant achievement that to the best of our knowledge has never been realized for any ultrafast I-V measurements in ns range. The plots shown in Fig. 4b and 4c are used to obtain the maximum $g_m(g_{m-max})$ and threshold voltage (V_t) using linear extrapolation of $I_D - V_G$ at g_{m-max} (Fig. 5a and 5b). The heated amplifier inside the cryo-chamber raising the device temperature during the measurements is a concern. The actual local temperature of the device is somewhat difficult to discern

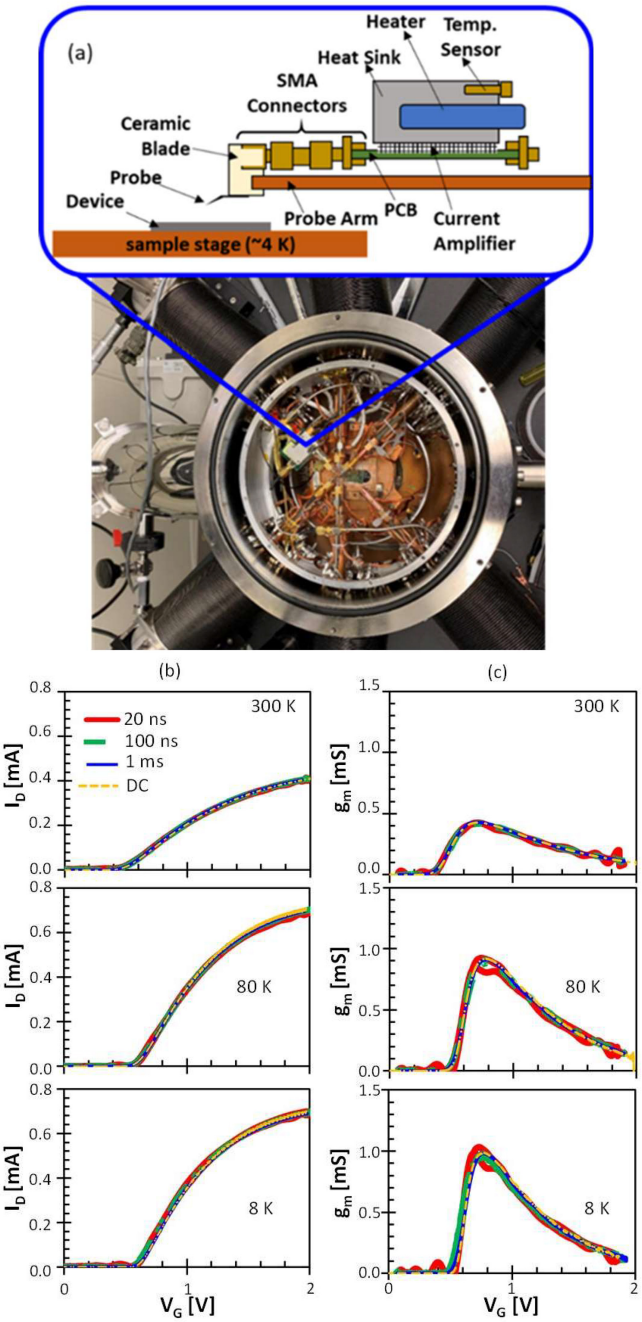

FIGURE 4. **(a) Top view of the cryogenic probe station showing all the probes and high-speed cables in the chamber and schematic side view of the probe arm with attached amplifier showing heat sink, heater and temperature sensor used to maintain the temperature of the amplifier inside the chamber along with device and the cold sample stage that is temperature controlled down to ~4 K. b) Fast IV done with RT/FT of 1 ms(—— ——), 100 ns(— — —) and 20 ns(——) at 300K, 80 K and 8 K compared to DC IV(— — —). c) corresponding $g_m - V_G$ plot showing good agreement for all the RT/FT measurements done at various temperatures and RT/FT compared to DC validating the accuracy of the setup. Device: W x L = 10 μm x 0.36 μm, Si/SiO_2 nMOSFET, V_D = 50 mV.**

with the closest temperature sensor monitoring the sample stage. The sample is placed on the stage using silver paste to achieve good thermal contact. To make sure that the elevated temperature of the amplifier was not affecting the

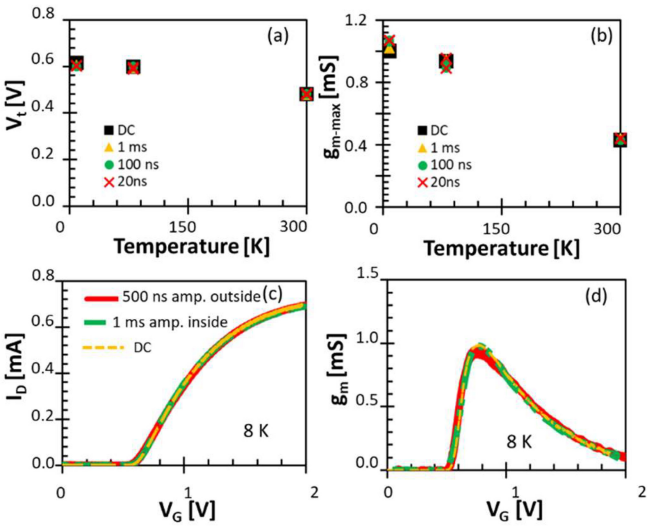

FIGURE 5. a) V_t and b) g_{m-max} versus temperature (8K, 80 K and 300 K) plot obtained for data set shown in Fig. 4b and c for both up and down sweep. c) I_D-V_G and d) $g_m - V_G$ measurements for same device with various measurement setup, i) with amplifier outside with RT/FT = 500 ns, ii) with the same amplifier inside as shown in Fig. 4a with RT/FT = 1 ms and iii) DC measurement with parameter analyzer. Device: W x L = 10 μm x 0.36 μm, Si/SiO_2 nMOSFET, V_D = 50 mV.

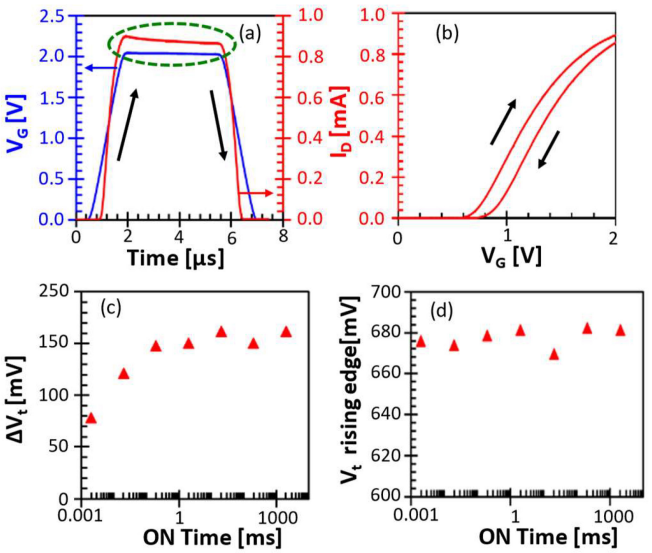

FIGURE 6. (a) V_G and I_D versus time characteristics for a slower RT/FT of 1 μs and a pulse width (ON time) of 5 μs. The chosen HfO_2-based device (W x L = 10 μm x 0.2 μm, V_D = 50 mV) exhibits bulk electron trapping even at 300 K (green oval). b) This corresponds to near parallel V_{th} shift in the $I_D - V_G$ characteristic. c) V_t shift ($\Delta V_t = V_t(down) - V_t(up)$) as a function of ON time showing electron trapping being dominant effect for ON voltage of 2 V with RT/FT of 1 μs with de-trapping of >5 s. d) Shows the measured V_t for varying ON time after 5 s showing complete within the standard deviation of 4 mV after 5 s. All the measurements were done at 300 K on the same device.

device temperature, measurements were done with the same amplifier outside the chamber at 8 K and compared to the measurements done with amplifier inside and with DC (no amplifier) measurements for the same sample stage temperature (Fig. 5c and 5d). The close correspondence between the measurements in Fig. 5c and 5d confirm that the heated amplifier was effectively thermally decoupled from the sample. The RT/FT of 500 ns is used to do the fastest possible measurement with the amplifier outside the chamber. Any measurements with RT/FT below it was plagued with measurements artifacts further supporting the need for placing the amplifier as close as possible to the device being measured. There have been reports of self-heating [18] in devices at low temperatures. For the measurements shown in Figs. 4 and 5, there was no change in the IV characteristics with RT/FT variation or with and without the amplifier close to the device for a fixed RT/FT of 500 ns. It is reasonable to infer any changes due to self-heating, if any, are minimal for the time scales shown in Fig. 4 and are not affected by nearby amplifier. To ensure this remains the case for all the measurements shown in later sections, V_D is limited to 50 mV to minimize dissipated power.

III. RESULTS AND DISCUSSION

Upon validation of the experimental setup, a series of charge trapping/de-trapping measurements on high-k devices were performed to demonstrate the capability of the technique described in Section II. High-k nMOSFETs with shallow traps [6] were used to accentuate the impact of temperature and measurement speed on the charge trapping/de-trapping dynamics. The high-k devices ($V_{DD} = 1.6$ V) were also interrogated at somewhat elevated V_G (2V) to clearly illustrate the reversible hysteretic charge trapping without notable defect generation (Fig. 6). At 300 K, the chosen devices exhibit a non-negligible electron trapping component in the bulk of the dielectric. Note that hysteresis seen in Fig. 6b) is due to the device and not the setup as confirmed by Fig. 4b) and c) as the same setup was used for the measurements shown in Fig. 6. Electron trapping is evident in the I_D transient when the V_G is high (ON) (Fig. 6a). The electron trapping induced droop in the I_D (green oval) when the V_G is ON, manifests as a lateral shift in the fast I-V taken on the rising and falling edges of the gate pulse (Fig. 6b). The lateral shift can be parametrized as a V_t shift (obtained by linear extrapolation of $I_D - V_G$ at max g_m) which increases as a function of ON time. A hysteretic V_t shift ($\Delta V_t = V_{t(down)} - V_{t(up)}$) as a function of pulse width or ON time is shown in Fig. 6c. An examination of the ΔV_t for longer ON times (Fig. 6c) reveals that the ΔV_t saturates for over 3 decades in time. In these devices, the hysteric effects dissipate quickly via a de-trapping process upon removal of the V_G pulse. At the conclusion of every pulse, more than 5 s of de-trapping time ($V_G = 0$ V) was inserted to ensure the device had returned to the initial state (within a standard deviation of 4 mV as shown in Fig. 6c). This longer-term ΔV_t saturation exhibited in Fig. 6c is consistent with earlier observations in high-k gate stacks with shallow traps which exhibit a nearly insatiable ability to capture negative charge into bulk traps [6], [19]. The ΔV_t is measured at the falling edge of a pulse (Fig. 6a) and the only measurement

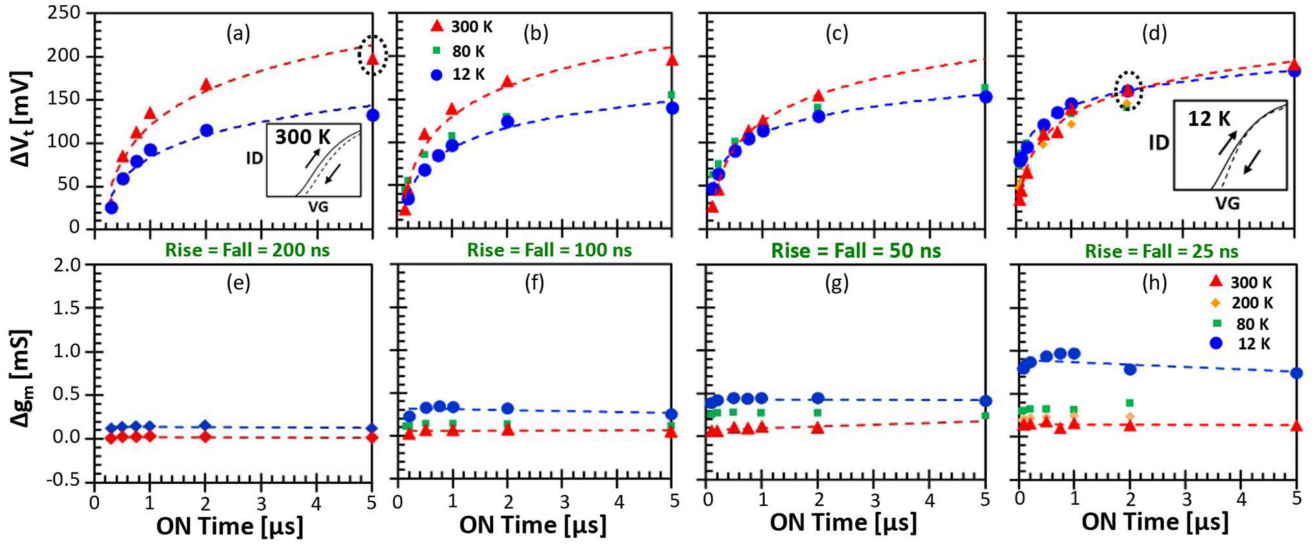

FIGURE 7. ΔV_t-ON time plots for RT/FT of a) 200 ns, b) 100 ns, c) 50 ns and d) 25 ns measured at 300 K and 12 K. Insets in (a) and (d) correspond to the $I_D - V_G$ transients from the measurements denoted with the dashed circles. Δg_m-ON time plots for RT/FT of e) 200 ns, f) 100 ns, g) 50 ns and h) 25 ns measured at 300 K (▲) and 12 K (●). 80 K measurements (■) shown in b), c) d), f), g) and h) and 200 K (♦) measurements shown in d) and h) all fall between the 300 K and 12 K boundaries. The dashed lines serve as a guide to the eye which can be approximated as an exponential fit only for short ON times. Device: W x L = 10 µm x 0.2 µm, high-k nMOSFETs, V_D = 50 mV. The uncertainty in the ΔV_t and Δg_m parametric extractions is a maximum for the fastest and coldest measurements (d) and (h). For the 12 K measurements taken with 25 ns rise and fall times, the standard deviation (1s) in the extracted V_t is 2 mV and the standard deviation (1s) in the extracted maximum g_m value is 15 mS. The error bars for the standard deviations in this worst-case scenario (fast and cold) are smaller than the size of the data points and are omitted for clarity.

delay (recovery) occurs during this FT. Note that the observations as these can be used to extract key parameters of BTI measurements for device reliability [20], [21]. For this example, observations of complete de-trapping coupled with the saturating ΔV_t for ON times > 1 ms does not support the generation of additional charge trapping defects. Any trap generation (if present) is far smaller than the saturating bulk electron trapping component. The precise details of the observed trapping dynamics in these devices and their possible impact on the greater BTI understanding [22] requires a much richer set of experiments, such as multiple bias and stress time conditions.

Fig. 7(a-d) illustrates ΔV_t as a function of ON time for a variety of RT/FT at 12 K and 300 K. The ΔV_t hysteresis is always positive which indicates the falling edge of the $I_D - V_G$ transient is always shifted to more positive values due to an accumulation of negative charge (electron trapping). At longer ON times and longer RT/FT, the hysteretic ΔV_t trends towards the typical explanation of charge trapping in these devices formulated from much slower measurements. For example, Fig. 7a illustrates a slowly saturating increase in ΔV_t for increasing ON time for both cryogenic and room temperature measurements. It should be noted that for long ON times > 1 µs the trapping will mostly be dominated by the ON time and less affected by the RT. When the V_G is high (ON), electron trapping proceeds to fill these bulk traps and eventually saturates. It is not surprising that this general trend is also observed at cryogenic temperatures, albeit in smaller proportions. The decreased charging at 12 K is largely due to the reduced charge capture probability at lower temperatures. The reduced capture probability is led by low temperature effects such as reduced thermal velocity [23], [24], [25] and sharp energy distribution of traps due to small phonon scattering that are energetically aligned for tunneling into these existing bulk dielectric traps. Evidence of bulk dielectric electron trapping is also borne out in the inset of Fig. 7a which illustrates that the ΔV_t hysteresis for longer ON times (dashed oval) is linked to a near perfect lateral shift in the fast I-V transients (with no notable change in the g_m).

As the RT/FT decreases, this general behavior starts to change in interesting ways. An examination of Fig. 7d also reveals the same increase in ΔV_t hysteresis for increasing ON times. However, we observe that ΔV_t at 12 K is *larger* than the 300 K measurement for shorter ON times. As the ON time increases, the 300 K measurement catches and eventually outpaces the 12 K measurement. Furthermore, the inset of Fig. 7d for 12 K shows that the ΔV_t hysteresis at the fastest RT/FT and coldest temperatures involve both a lateral shift (slow electron trapping) as well as a change in g_m (fast trap participation). The term fast traps are given to traps capable of following the RT/FT of gate sweep (likely interface and/or near interface traps that affects the g_m) and slow electron traps are bulk traps that are slow to respond to the gate sweep but are present and cause the I-V transient to laterally shift (resulting in ΔV_t with little or no *change* in g_m). The larger change in g_m and ΔV_t, for 12 K in Fig. 7d therefore suggests that the V_t shift is mostly due to fast traps

for fastest RT/FT and coldest temperature. For longer term stability considerations, these measurements were performed at 12 K instead of 8 K.

This interesting behavior is further illustrated in Fig. 7(e-h) which show the complementary hysteretic g_m shifts ($\Delta g_m = g_m(down) - g_m(up)$) as a function of ON time for various RT/FT at 12 K as well as 300 K. Fig. 7h demonstrates that the Δg_m decreases with increasing temperature. We note that for slower RT/FT (closer approximation to conventional I-V characterizations) there is almost no Δg_m hysteresis regardless of ON time or measurement temperature (Fig. 7e). However, for faster RT/FT we observe a much larger Δg_m hysteresis (almost a factor of 6 for 25 ns RT/FT) at cryogenic temperatures as well as a weak ON-time dependence. This Δg_m hysteresis is always positive which indicates that the $I_D - V_G$ transient on the *falling edge* has a *larger* g_m than on the rising edge indicating improved mobility. This striking improvement of g_m can be speculated as the outcome of passivation of a base line defect population (positive charge centers) reducing the columbic scattering like in [14]. In general, we note a more pronounced $\Delta V_t$and a larger Δg_m hysteresis for the faster measurements at colder temperatures (Figs. 7d and 7h) and a reduced $\Delta V_t$and almost no Δg_m hysteresis for slower measurements at the same colder temperatures (Figs. 7a and 7e).

To clearly realize the effects of ON time and RT/FT, ΔV_t in Fig. 7(a-d) and Δg_m in Fig. 7(e-h) is delineated with respect to the ON time and RT/FT in Fig. 8. Fig. 8a suggests that irrespective of the temperature and RT/FT, the V_t shift increases with ON time which can be taken as the approximate stress time. This is consistent with, more stress time leading up to more charge trapping and increased V_t shift. But the V_t dependence on RT/FT in Fig. 8b shows that at 300 K charge trapping is not much affected by the RT/FT as much as it is affected by the ON time suggesting slow traps being dominant. But at 12 K negative charge trapping reduces for longer RT/FT signifying the longer RT/FT measurements were underestimating the charge trapping (overlooking the fast traps) at lower temperatures. This is further validated by Fig. 8c and 8d where Δg_m is not much affected by the ON time but strongly affected by the RT/FT at 12 K compared to 300 K. This is because the fast/interface traps affect the channel mobility, therefore shifts in g_m are more pronounced when fast traps are involved.

Investigating the time constants of the charge trapping depicted by the ΔV_t in Fig. 7(a-d) as a function of the FT or the recovery time after stress (ON time) and temperature would allow for better understanding of these traps. But, to investigate the time constants more data points for higher resolution of stress time and detailed set of experiment with more bias conditions would be required. It will therefore be beyond the scope of the paper and will be discussed in later publications. Similarly, de-trapping will also have to be investigated in detail measuring the ΔV_t shifts for various recovery times. Studies like this would be

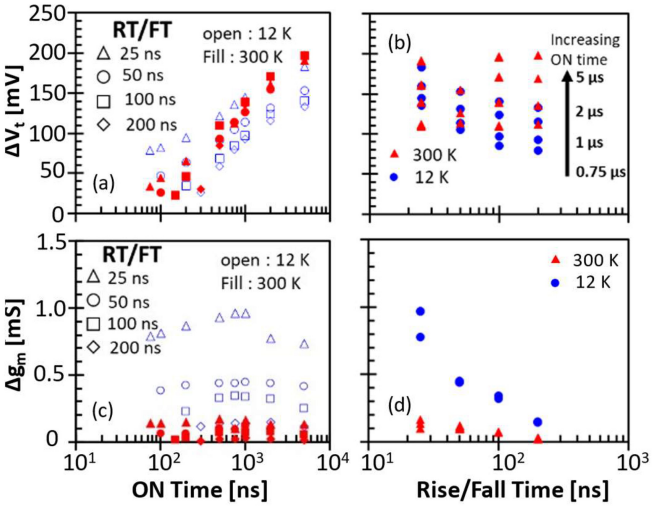

FIGURE 8. a) ΔV_t– ON Time for all the data shown in Fig. 7 showing increase in the V_t shift with increasing stress time for 300 K a well 12 K measurements. b) ΔV_t– Rise/Fall time for ON-Times of 0.75 µs, 1 µs and 2 µs of 300 K and 12 K measurements. Showing clear difference in rise and fall time dependent V_t shift for 12 K (decrease with increasing RT/FT) and 300 K (no significant RT/FT time dependence). c) Δg_m – ON Time showing no significant g_m shift with increasing stress time for 300 K a well 12 K measurements. d) Δg_m – Rise/Fall time for ON-Times of 0.75 µs, 1 µs, 2 µs and 5 µs of 300 K and 12 K measurements. Note: 5 µs data for 300 K is missing due to missed measurement. Showing clear difference in rise and fall time dependent g_m shift for 12 K (decrease with increasing RT/FT) as well as 300 K. With significantly more RT/FT dependence at 12 K compared to 300 K.

beneficial to understand and verify charge trapping models at low temperatures [26].

This work provides evidence of the importance of careful fast I-V characterizations at cryogenic temperatures. The non-equilibrium cryogenic environment shifts charging transients, which are typically ignored, directly impact cryogenic circuit operation. This information is specifically important in analog circuit design, like those being employed in quantum computation schemes, as these charging transients can be quite impactful. This fast characterization setup can also be used to obtain a substantial wealth of information in understanding more traditional reliability aspects of the devices [10] operated in cryogenic environments. In addition, the fast time dynamics and cryogenic environments accessible through these measurements could be quite beneficial to efforts studying the BTI charge trapping through time-dependent defect spectroscopy [20].

IV. CONCLUSION

This manuscript details the experimental setup capable of accurately measuring fast I-V for RT/FT as short as 20 ns at temperatures at and down to 8 K. The accuracy of the technique was established by presenting never realized identical $g_m - V_G$ curve for RT/FT ranging from 20 ns to 1 ms for ultrafast $I_D - V_G$ measurements. Time- and temperature-dependent trapping dynamics in bulk trap rich

high-k devices were measured to demonstrate the capabilities of cryogenic ultrafast $I_D - V_G$ technique. ΔV_t and Δg_m were measured for varying pulse RT/FT and ON times at 300 K and 12 K for high-k devices. The low temperature and high-speed measurement conditions allowed for observations linked to an underlying participation of fast traps (likely interface and/or near-interface states) capable of affecting the device g_m shown by variation in Δg_m. If unaccounted for in the analog circuit design phase, these transients could impact cryogenic circuit operations. Thus, low temperature fast measurements fill a growing characterization void to understand unknown trapping dynamics which are unique to circuits operating in cryogenic environments.

Certain commercial equipment, instruments, or materials are identified in this paper to specify the experimental procedure adequately. Such identification is not intended to imply endorsement by NIST, nor to imply that the materials or equipment identified are necessarily the best for the purpose.

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