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Cell Design Consideration in SiC Planar IGBT and Proposal of New SiC IGBT With Improved Performance Trade-Off

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ABSTRACT In silicon carbide (SiC) planar insulated-gate bipolar transistor (IGBT), a large distance between neighboring p-bodies is beneficial to enhance the on-state conductivity modulation, but will expose the gate oxide to high electric field in off-state. With p-bodies placed closer, the gate oxide field is reduced, but the conductivity modulation is suppressed. In this work, a new SiC planar IGBT with oxide shield is proposed and studied by TCAD simulations. The proposed SiC IGBT achieves improved trade-off between on-state voltage drop (V_{ON}) and maximum gate oxide electric field ($E_{ox\text{-}m}$). When a quite larger distance between neighboring p-bodies is adopted in the proposed SiC IGBT, a low V_{ON} is obtained, while the $E_{ox\text{-}m}$ can be kept at a small value with the oxide shielding structures protecting the gate oxide. Switching characteristics are also studied, and the proposed SiC-IGBT delivers much better trade-off between turn-off energy loss (E_{OFF}) and V_{ON} than the conventional SiC planar IGBT.

INDEX TERMS SiC IGBT, oxide shield, on-state voltage drop, maximum gate oxide electric field, turn-off energy loss.

I. INTRODUCTION

Due to the superior properties of silicon carbide (SiC), such as wide bandgap, large critical electric field, and high temperature endurance, SiC based devices are widely studied for high-power and high-temperature applications [1], [2], [3], [4], [5], [6]. For ultrahigh voltage applications, the bipolar SiC IGBTs are preferred over the unipolar MOSFETs. With conductivity modulation, SiC insulated-gate bipolar transistors (IGBTs) boast low on-state voltage drop (V_{ON}) [7], [8], [9], [10], [11], [12], [13], [14]. An important design issue for the IGBTs is to enhance the conductivity modulation near the surface side of the device. However, in the SiC IGBTs, the grounded p-bodies extract holes around them which leads to a degradation of conductivity modulation. Like in silicon IGBTs, enlarging the JFET region between neighboring p-bodies can effectively enhance the conductivity modulation, since the accumulation electron layer beneath the MOS-gate leads to an injection enhancement effect [15], [16]. However, the critical breakdown field of SiC material is nearly ten times higher than silicon. For the SiC IGBT with a wide JFET region, the high electric field cannot be effectively shielded by the p-bodies, so the device would suffer an increase of maximum gate oxide field ($E_{ox\text{-}m}$) over the JFET region. The gate oxide field is a critical reliability concern for SiC power devices [17], [18], [19], [20], [21]. A high oxide field may reduce the lifetime of the SiC power devices. During short-circuit events and avalanche events, the high oxide field facilitates hot carriers to bump against

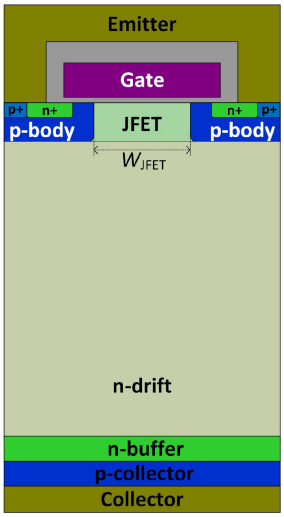

FIGURE 1. Schematic cross-section of the conventional SiC planar IGBT.

the gate oxide and to be trapped in the oxide, resulting in device failure [22]. In SiC power MOSFETs, various shield structures have been proposed to suppress the gate oxide field [20], [21], [23], [24], [25], [26]. The essence of these structures is to use a grounded p-region to shield the gate oxide from high electric field [23], [24]. As grounded p-type shielding structures degrade the conductivity modulation in SiC IGBTs, they cannot be readily transferred to SiC IGBTs [27].

In this paper, we investigate the SiC planar-gate IGBT designs using Synopsys Sentaurus TCAD simulations. Electron/hole continuity equations and Poisson equation are solved selfconsistently with Shockley-Read-Hall recombination, Auger recombination, incomplete dopant ionization, doping dependent transport, high-field saturation mobility, band narrowing, anisotropic material properties, and impact ionization included. The trade-off between conductivity modulation and the gate oxide field in conventional planar IGBT structure will be analyzed firstly. To address this dilemma, a new SiC IGBT structure is proposed with oxide shielding structures implemented. For the proposed SiC IGBT, the V_{ON} can be significantly reduced without worrying the rise of oxide field.

II. V_{ON}-E_{OX-M} TRADE-OFF IN SIC PLANAR-GATE IGBT

Firstly, the cell design of SiC planar IGBT is investigated. Figure 1 shows the schematic cross-section of the conventional SiC planar IGBT. The doping concentration and thickness of the n-drift region are 2.5×10^{14} cm^{-3} and 180 μm respectively for 20-kV voltage level. The thickness of the gate oxide is 50 nm. The channel length is 0.5 μm [28], [29]. The channel mobility is set to be 30 cm^2/V-s [29], [30]. The doping concentration and depth of the p-body are 1×10^{17} cm^{-3} and 0.8 μm, respectively. The doping concentration of the JFET region between neighboring p-bodies is 1×10^{16} cm^{-3}. The width of the JFET region (W_{JFET}) plays a critical role to the performances of

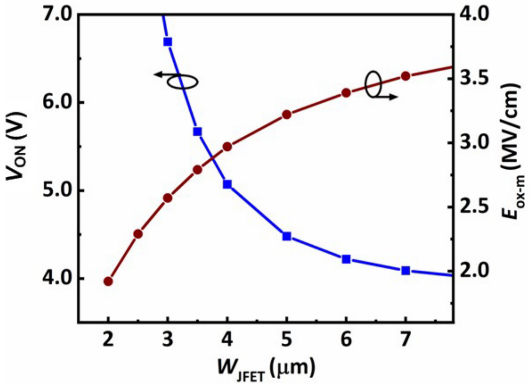

FIGURE 2. The influence of W_{JFET} on V_{ON} and E_{ox-m} in the conventional SiC IGBT.

the SiC IGBT, and is a design parameter to be investigated. The device area is fixed at 1 cm^2 by adjusting the respective area factor for each design accordingly. The carrier lifetime is set as 2 μs [29], [31]. The n-buffer layer thickness and doping concentration are 10 μm and 4×10^{17} cm^{-3} respectively. The p-collector region is designed with thickness of 5 μm and doping concentration of 1×10^{19} cm^{-3}, and the study in this paper is at room temperature, unless otherwise specified.

Figure 2 shows the influences of the W_{JFET} upon V_{ON} and E_{ox-m} in the conventional SiC planar IGBT. With the increasing of W_{JFET}, V_{ON} decreases. For an IGBT, the electron accumulation layer under the MOS-gate helps to enhance the conductivity modulation of the device. On the contrary, the grounded p-bodies serve as a sink for minority carriers and thus suppress the conductivity modulation. A larger W_{JFET} increases the area ratio of MOS-gate region over the p-body region, and thus helps to enhance conductivity modulation, as evidenced by the higher plasma density.

The other crucial design consideration for the SiC IGBT is the strength of gate oxide field in off-state. With the p-bodies placed apart, a large number of off-state electric field lines have to be terminated at the gate termination. Therefore, the gate oxide above the JFET region experiences an increased electric field. In the IGBTs with a small W_{JFET} of 2.5 μm, the maximum oxide field E_{ox-m} is 2.29 MV/cm, as shown in Fig. 2. With a narrow JFET region, the gate oxide is protected by the p-bodies more efficiently from the high collector bias. With a larger W_{JFET}, E_{ox-m} increases with it. For W_{JFET} of 7 μm, E_{ox-m} rises to 3.52 MV/cm, because the MOS-gate far away from the p-bodies are less effectively protected. Hence, a larger W_{JFET} would lead to higher E_{ox-m} in the conventional SiC IGBT.

Thus, with the increasing of W_{JFET}, V_{ON} decreases while E_{ox-m} increases. The V_{ON}-E_{ox-m} relationship is a trade-off for the design of the SiC planar-gate IGBTs.

III. DEVICE STRUCTURE AND PERFORMANCE OF PROPOSED SIC IGBT

Figure 3 shows the proposed SiC IGBT. The proposed IGBT features oxide shields, i.e., a series of p$^+$ islands beneath

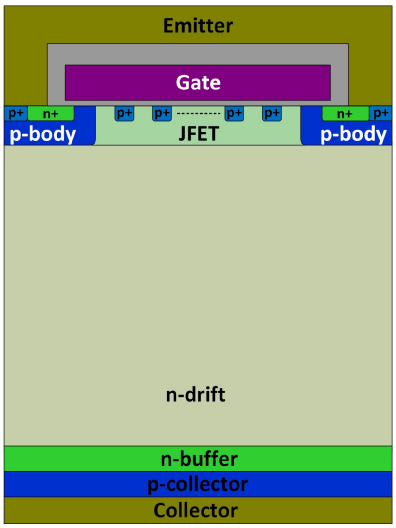

FIGURE 3. Schematic cross-section of the proposed SiC IGBT with surface p^+ islands.

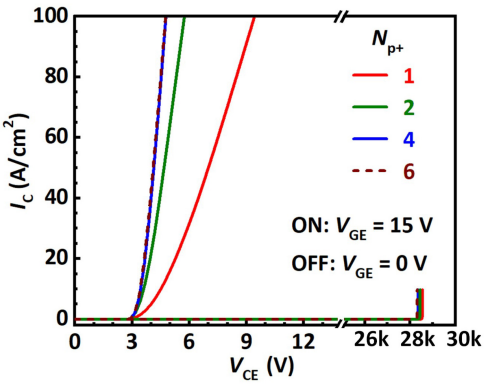

FIGURE 4. *I-V* characteristics of the proposed SiC IGBTs with different numbers (N_{p+}) of the surface p^+ islands.

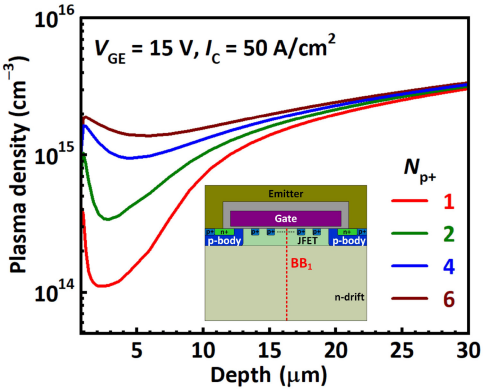

FIGURE 5. Plasma density (cut across the middle line BB_1 of the cell) along the depth of the drift region in the proposed SiC IGBT.

the MOS-gate. Unlike SiC MOSFET that uses grounded p-regions to protect the gate oxide [20], [24], here, the proposed IGBT utilizes floating p-islands as oxide shield structure. The p-regions in SiC MOSFET need to be grounded, because floating p-regions will lead to dynamic degradation in MOSFETs [23], [32]. However, the surface p^+ islands in the proposed IGBT are floating, because grounded p-islands will extract holes and degrade conductivity modulation in on-state. Dynamic degradation is not an issue in IGBTs, since the minority carriers quickly eliminates the charge storage in the floating p-islands once the device is turned on [27]. The fabrication process of the proposed SiC IGBT is compatible with the conventional planar-gate IGBTs, since the floating p-islands can be formed using the same step as the p^+ Ohmic implantation at the surface of the p-body. Hence, no extra fabrication processes are needed for the proposed SiC IGBT, compared to the conventional SiC IGBT. In literature, grounded surface p-shield has been demonstrated for SiC power MOSFET, and the method can be transferred to SiC IGBT except the p-islands are floating [20].

The proposed SiC IGBT uses the same set of device parameters with the conventional SiC IGBT, except the floating p^+ islands. In the study, the width of every p^+ island is 1 μm. The thickness of the p^+ islands is 0.3 μm. The distance between the p-body and its nearest p^+ island is 1 μm. The distance between two neighboring p^+ islands is 1 μm. Hence, in the proposed SiC IGBT, the W_{JFET} increases with the number of p^+ islands in one cell (N_{p+}), and satisfies the relationship $W_{JFET} = 2 \times N_{p+} + 1$.

The *I-V* characteristics of the proposed SiC IGBTs with different N_{p+} are shown in Fig. 4. The implementation of the p-shield structure has nearly no observable influence upon the off-state breakdown voltage of the SiC IGBT. In the on-state, the V_{ON} of the SiC IGBTs decreases with increased number of surface p^+ islands (i.e., a wider JFET region), which agrees with the observation in conventional SiC IGBT. When only one surface p^+ island is adopted in one cell pitch, the V_{ON} (defined at collector current of 50 A/cm^2) is as large as 7.0 V. While with more than 4 surface p^+ islands, the V_{ON} is reduced to ~4.1 V. Fig. 5 shows the plasma density (cut across the middle line BB_1 of the cell in the inset) in the SiC IGBTs at a collector current of 50 A/cm^2. With more surface p^+ islands, the JFET region becomes widened which increases the area ratio of MOS-gate region over the p-body region. The grounded p-bodies exact minority carriers, while the electron accumulation layer under the MOS-gate helps to enhance the carrier density. Thus the conductivity modulation is clearly enhanced. The widened JFET region and enhanced conductivity modulation will not weaken the short circuit capability of the proposed SiC IGBT, as the distance between p-body and its nearest p^+ island is only 1 μm which helps to clamp saturation current. A smaller saturation current indicates better short circuit capability. Details of the short circuit capability improvement of the proposed SiC IGBT need to be proved by experiments.

With larger and larger W_{JFET}, the $E_{ox\text{-}m}$ of the conventional SiC IGBT increases soon to >3 MV/cm, as shown in Fig. 2. But the $E_{ox\text{-}m}$ performance of the proposed SiC IGBT is quite different to the conventional SiC IGBT. Fig. 6 displays the

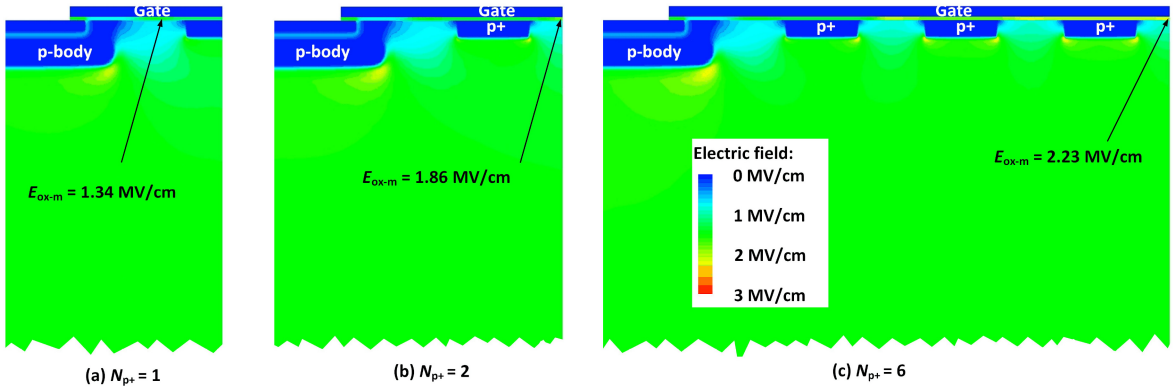

FIGURE 6. Electric field distributions of the proposed SiC IGBTs (under $V_{CE} = 20$ kV and $V_{GE} = -5$ V) with different N_{P+}.

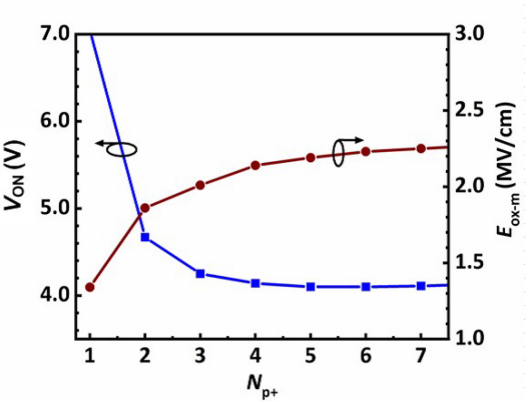

FIGURE 7. The dependencies of V_{ON} and $E_{ox\text{-}m}$ on N_{P+} in the proposed SiC IGBT.

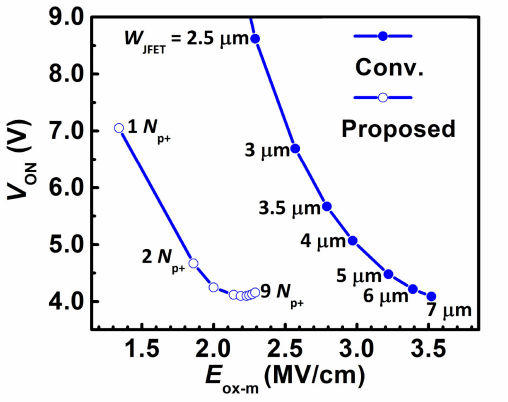

FIGURE 8. V_{ON}-$E_{ox\text{-}m}$ trade-off of the conventional and proposed SiC IGBT by changing the JFET width.

electric field distributions of the SiC IGBT with different N_{p+}. With a smaller number of N_{p+}, the p-bodies serve as a protection for the gate oxide, since they terminate most of the electrical lines. With a larger number of N_{p+}, the shielding effect from the p-bodies becomes very weak, so the electric field in oxide increases. However, thanks to the protection from the surface p^+ islands, the $E_{ox\text{-}m}$ of the proposed SiC IGBT is still kept at small values even the p-bodies are very far apart. The potential of the p^+ islands is determined by V_{CE} in off-state. The influences of the N_{p+} on both the V_{ON} and $E_{ox\text{-}m}$ are plotted in Fig. 7. With more and more surface p^+ islands, the V_{ON} decreases to the lowest value, while the $E_{ox\text{-}m}$ are kept at a small value.

IV. COMPARISON OF SIC IGBTS

For comparison, Fig. 8 summarizes the trade-off between V_{ON} and $E_{ox\text{-}m}$ by changing the distance between neighboring p-bodies in both the conventional SiC IGBT and the proposed SiC IGBT (i.e., changing the number of p-islands in proposed IGBT). The proposed SiC IGBT features much better V_{ON}-$E_{ox\text{-}m}$ trade-off than the conventional SiC IGBT. In the proposed SiC IGBT, the $E_{ox\text{-}m}$ is kept at a low level even if the W_{JFET} is large enough for a very strong conductivity modulation. While in the conventional SiC IGBT, with wider JFET regions, the $E_{ox\text{-}m}$ increases to very large value.

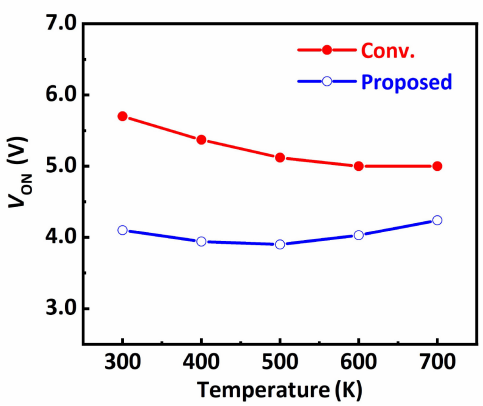

FIGURE 9. The influence of temperature on V_{ON} of the studied SiC IGBTs.

Silicon carbide devices are more suitable for higher temperature operation. The influence of temperature on V_{ON} of the conventional and proposed SiC IGBT is shown in Fig. 9. The conventional SiC IGBT with W_{JFET} of 3.5 μm, which has an $E_{ox\text{-}m}$ of 2.75 MV/cm and a V_{ON} of 5.67 V, is presented here. The proposed SiC IGBT with the lowest V_{ON}

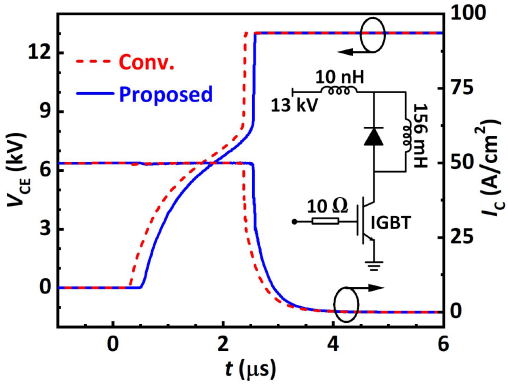

FIGURE 10. Turn-off transients for the studied SiC IGBTs in an inductive load switching configuration which is plotted inside.

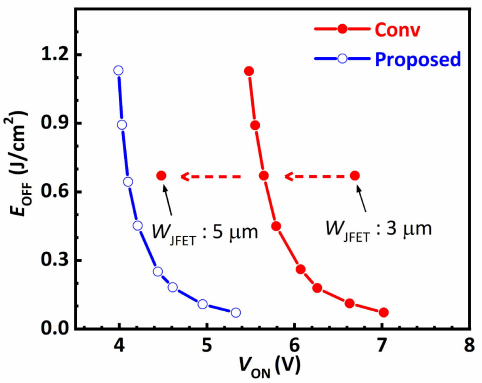

FIGURE 11. Trade-off between E_{OFF} and V_{ON} in the conventional SiC IGBTs (W_{JFET} = 3 μm, 3.5 μm and 5 μm) and the proposed SiC IGBT (N_{p+} = 6) by changing the collector doping concentration.

(4.1 V) is presented here, which has a N_{p+} of 6, and an $E_{ox\text{-}m}$ of 2.23 MV/cm. With the increasing of temperature, the reason for the result is complicated with combined influence from plasma density, carrier mobility, and lifetime, etc. For the critical characteristic $E_{ox\text{-}m}$, $E_{ox\text{-}m}$ of each device does not change with temperature, because electric field strength is same under the same condition of $V_{CE} = 20$ kV and $V_{GE} = -5$ V.

Figure 10 presents the turn-off characteristics of the studied SiC IGBTs. The testing circuit is illustrated in the inset of the figure. The DC bus voltage is set to be 13 kV. The load current is 50 A/cm^2. The load inductor value is 156mH. A 10-nH stray inductance is assumed in the power loop. A gate resistor R_G of 10 Ω is adopted. The proposed SiC IGBT ($N_{p+} = 6$) presents a smaller V_{ON}, because it has higher plasma density than the conventional MOSFET ($W_{JFET} = 3.5$ μm). The higher plasma density has to be extracted out in the initial stage of turn-off transient, which delays the turn-off transient. Apart from the delay, the switching characteristics of the proposed IGBT are similar with the conventional IGBT. The higher plasma density at the top side of the proposed IGBT does not obviously add to the turn-off loss, since during the initial stage, the voltage across the IGBT is still very low.

Figure 11 compares the E_{OFF}-V_{ON} trade-off of the studied SiC IGBTs under the variation of collector dose (multiplication of collector doping concentration and collector thickness). The collector thickness is fixed at 5 μm, while its doping concentration is varied with 1.8×10^{19} cm^{-3}, 1.4×10^{19} cm^{-3}, 1×10^{19} cm^{-3}, 7×10^{18} cm^{-3}, 4×10^{18} cm^{-3}, 3×10^{18} cm^{-3}, 2×10^{18} cm^{-3}, and 1.5×10^{18} cm^{-3}. The E_{OFF}-V_{ON} trade-off performance of the proposed SiC IGBT is superior to that of the conventional SiC IGBT. For the conventional SiC IGBT, to obtain a better E_{OFF}-V_{ON} trade-off, a larger W_{JFET} should be adopted. Fig. 11 also presents the conventional SiC IGBT with $W_{JFET} = 3$ μm and that with $W_{JFET} = 5$ μm. The conventional SiC IGBT with a larger W_{JFET} of 5 μm has an E_{OFF}-V_{ON} trade-off approaching that of the proposed IGBT. However, the conventional SiC IGBT with a larger W_{JFET} of 5 μm has to suffer a high $E_{ox\text{-}m}$ of 3.22 MV/cm, which the conventional SiC IGBTs with smaller W_{JFET} of 3 μm and 3.5 μm have much lower $E_{ox\text{-}m}$ of 2.57 MV/cm and 2.75 MV/cm, respectively. Therefore, the proposed SiC IGBT with oxide shield provides a promising solution to improve E_{OFF}-V_{ON} trade-off while keep oxide field at a low level.

V. CONCLUSION

In conventional SiC planar IGBT, a wide JFET region is beneficial to decrease the on-state voltage drop (V_{ON}), but degrade the gate oxide reliability easily. In this paper, a new SiC IGBT with oxide shields is proposed to improve trade-off between V_{ON} and maximum electric filed in gate oxide ($E_{ox\text{-}m}$). Simulation results show, a low V_{ON} is obtained in the proposed SiC IGBT with a wide JFET region, while a low $E_{ox\text{-}m}$ is maintained by the floating surface p$^+$ islands. As a result, an improved $E_{ox\text{-}m}$-V_{ON} trade-off is obtained in the proposed IGBT while the oxide field keeps at a low level. The proposed SiC IGBT provides a cost-effective approach towards high-performance and high-reliability ultrahigh voltage power transistors.

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