Received 18 December 2022; revised 23 February 2023; accepted 2 March 2023. Date of publication 7 March 2023; date of current version 15 March 2023.
The review of this article was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2023.3253137

High Temperature Operation of E-Mode and D-Mode AlGaN/GaN MIS-HEMTs With Recessed Gates

HANWOOL LEE, HOJOON RYU, JUNZHE KANG, AND WENJUAN ZHU (Senior Member, IEEE)

Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL 61801, USA

CORRESPONDING AUTHOR: W. ZHU (e-mail: wjzhu@illinois.edu)

This work was supported by the Defense Advanced Research Projects Agency (DARPA) under Grant HR0011-20-1-0005BS123456.

ABSTRACT High temperature operation of enhancement-mode (E-mode) and depletion-mode (D-mode) AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) was demonstrated. By using the circular device structure, off-state current was effectively suppressed, and record high Ion/Ioff ratio around 10^8 was obtained at 400 °C. Atomic layer etching was used for formation of the gate recess structure in the E-mode device, and good interface was made which enabled stable normally-off operation up to 400 °C. D-mode device experienced positive threshold voltage shift during the high temperature operation and after cooling down to room temperature, due to strain relaxation. On the other hand, due to the very thin AlGaN layer retained under the gate of the E-mode device, the threshold voltage of the E-mode device is nearly unchanged when the sample is heated up and cooled down. A direct coupled field-effect transistor logic (DCFL) inverter was fabricated based on the E-mode and D-mode devices and showed stable operation up to 400 °C.

INDEX TERMS AlGaN/GaN, MIS-HEMT, high temperature electronics, enhancement-mode, normally-off, depletion-mode, direct-coupled FET logic, inverter.

I. INTRODUCTION

High temperature electronics are required in many industry applications, such as automotive, spacecraft, deep-well drilling, and engine systems [1]. However, high temperature operation of the electronic devices suffers from increase of the leakage current, poor stability, and degraded mobility [2], [3]. Gallium nitride (GaN) is one of the most promising candidates for the high temperature electronics, due to many advantageous properties such as large bandgap, high breakdown field, high saturation velocity, and high thermal stability [4], [5], [6].

AlGaN/GaN Schottky HEMTs have been tested for high temperature electronics, but gate metal diffusion into the barrier layer and large gate leakage induced severe degradation of the device characteristics at high temperature [7], [8], [9]. MIS-HEMT device, which has gate dielectric layer between the gate metal and AlGaN barrier layer, could overcome some of the difficulties by reducing the gate leakage current and improving the stability of the gate stack [8]. Various attempts were made with MIS-HEMT structure to achieve the stable high temperature operation, but most of them suffered from threshold voltage instability caused by AlGaN strain relaxation and interface traps [10], [11], [12], [13], [14]. Most of the studies only tested the high temperature operation up to 200 °C [11], [12], [13], [14], [15], [16], but device operation at higher temperature is necessary for meeting the requirement of the industry applications. Moreover, most of the demonstrated devices showed normally-on operation. There have been few reports about the normally-off high temperature MIS-HEMT, which is much more versatile for practical purposes [12], [13], [14].

In this work, we used circular device structure and gate recess made by atomic layer etching to suppress the leakage current and enhance the device stability at high temperature. Stable high temperature operation of both E-mode and D-mode devices were demonstrated. E-mode device showed

better threshold voltage stability compared to D-mode device at high temperature, which implies that the main reason for the threshold voltage instability is the AlGaN strain relaxation, and gate recess formation is beneficial for reducing this effect. DCFL inverter was fabricated by connecting the E-mode and D-mode devices, and it showed stable operation up to 400 °C, which shows potential of the AlGaN/GaN MIS-HEMT device as a promising candidate for high temperature logic device.

II. DEVICE FABRICATION

The MIS-HEMTs were fabricated on a commercial AlGaN/GaN on silicon substrate, which consists of a 2 nm GaN cap layer, 20 nm $Al_{0.25}Ga_{0.75}N$, 1 nm AlN interlayer, and 4.2 μm unintentionally doped (UID) GaN. Both E-mode and D-mode devices were fabricated. For E-mode devices, 4.3 nm AlGaN was retained under the gate after etching, and AlGaN layer was not etched in D-mode devices. In this work, two types of device structure, which are rectangular and circular structures, were used. In the circular device structure, mesa isolation is not needed since gate electrode is surrounding the circular drain electrode, which enables complete electrical isolation. This greatly reduces the off-state current of the device at high temperatures by removing the leakage current component caused by mesa isolation [17]. Both E-mode and D-mode devices had a gate-to-source distance (L_{GS}) of 12 μm, a gate length (L_G) of 2 μm, a gate-to-drain distance (L_{GD}) of 12 μm, and a channel width (W) of 0.44 mm in the case of the circular device.

Fabrication process of the AlGaN/GaN MIS-HEMT devices is as follows. After cleaning the wafer, mesa isolation was done by inductively coupled plasma reactive ion etching (ICP-RIE) using Cl_2 and BCl_3 for the rectangular devices. Ti/Al/Ni/Au (20 nm/120 nm/60 nm/50 nm) stack was deposited by e-beam evaporator and annealed at 900 °C in N_2 for 30 s for ohmic contact formation. AlGaN surface was passivated by 150 nm plasma-enhanced chemical vapor deposition (PECVD) silicon nitride. Silicon nitride under the gate was patterned and etched away by ICP-RIE using SF_6. To minimize the etching induced damage on the AlGaN surface, atomic layer etching with Cl_2 and Ar was used for the formation of gate recess in the E-mode device. 10 nm Al_2O_3 was deposited by atomic layer deposition (ALD) at 250 °C, 10 nm SiO_2 was deposited by ALD at 200 °C, and 10 nm silicon oxynitride (SiON) was deposited by PECVD at 300 °C, consecutively, for the gate dielectric of the device. Source and drain windows were opened by using ICP-RIE, and Ni/Au (50 nm/150 nm) gate electrode was deposited by e-beam evaporator. 200 nm SiO_2 was deposited by PECVD for passivation, and contact pads were opened by ICP-RIE using SF_6. Post-metallization annealing was done at 500 °C for 30 min under vacuum.

III. RESULTS AND DISCUSSION

The schematic of a D-mode GaN MIS-HEMT without gate recess is illustrated in Fig. 1a. Transfer and output characteristics of the circular D-mode device measured at room temperature are shown in Fig. 1b and 1c, respectively. D-mode device showed stable operation with threshold voltage of −14.7 V, indicating the normally-on behavior. Since this D-mode device did not have gate recess structure and relatively thick dielectric, threshold voltage was large negative value. Maximum current of 490 mA/mm and peak transconductance of 56.4 mS/mm were measured from the D-mode device. The device was measured at high temperatures up to 400 °C under vacuum condition. Transfer characteristics and gate current of the D-mode device at high temperature are shown in Fig. 1d and 1e, respectively. The circular D-mode device maintained stable operation with suppressed off-state current and steep subthreshold slope, and gate current was smaller than 10^{-6} mA/mm at 400 °C, which shows the stability of the gate dielectric stack. Output drain current is monotonically decreasing as the temperature increases since the mobility of the AlGaN/GaN channel decreases due to the increased phonon scattering (Fig. 1f) [2]. At 400 °C, maximum drain current and peak transconductance of the D-mode devices were 195 mA/mm and 19.1 mS/mm, respectively.

To test the high temperature device characteristic depending on the device geometry, two different types of devices

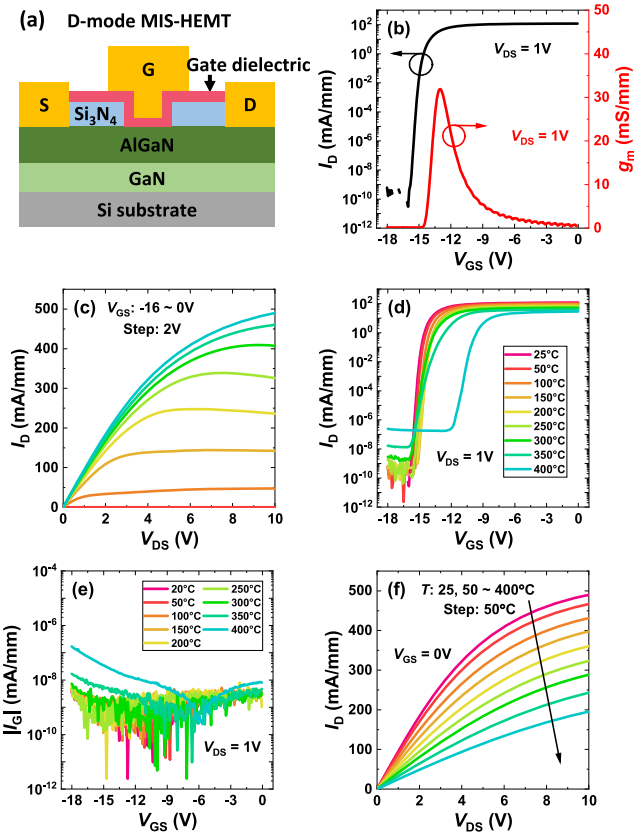

FIGURE 1. (a) Schematic of a D-mode circular AlGaN/GaN MIS-HEMT. (b) Transfer characteristic, transconductance (g_m), and (c) output characteristics of a circular D-mode MIS-HEMT without gate recess at room temperature. (d) Transfer characteristic, (e) gate current, and (f) output characteristics of the D-mode MIS-HEMT measured at various temperatures.

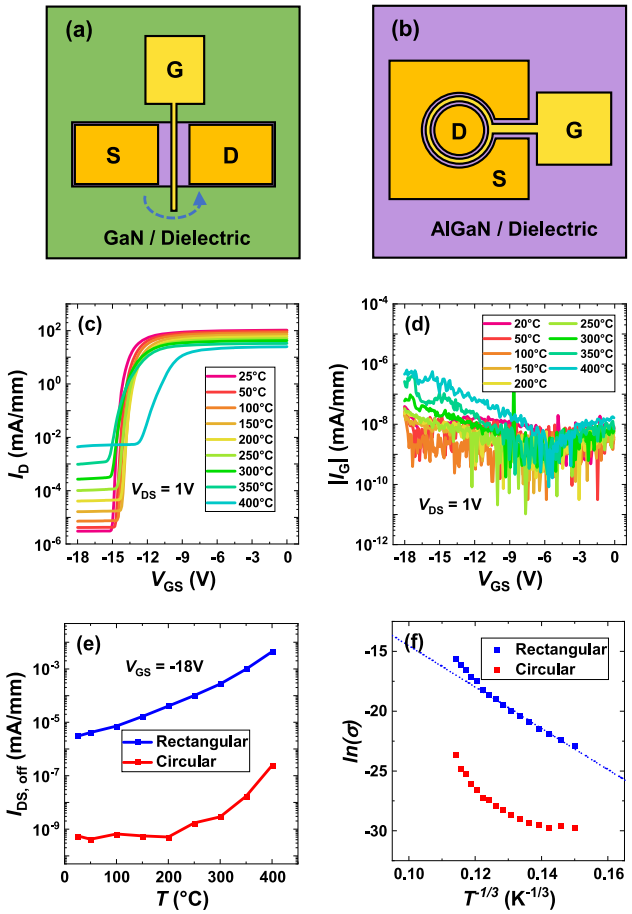

FIGURE 2. D-mode rectangular AlGaN/GaN MIS-HEMT and its comparison with circular MIS-HEMT. Top view of the (a) rectangular and (b) circular AlGaN/GaN MIS-HEMT. (c) Transfer characteristics and (d) gate current of a D-mode rectangular MIS-HEMT at high temperatures. Temperature dependence of the (e) off-state drain current and (f) off-state channel conductance of the rectangular and circular D-mode AlGaN/GaN MIS-HEMT.

are fabricated. The structures of the rectangular and circular devices are illustrated in Fig. 2a and 2b. For the rectangular device, rectangular active region was defined by mesa isolation before the source/drain electrode deposition using ICP-RIE with Cl_2 and BCl_3. All the other fabrication processes were the same as the process discussed previously. In this device structure, gate finger was placed between the source and drain electrode across the active region of the device, so that the electrode can have the complete control of the channel. On the other hand, in the case of the circular device structure, device isolation was not made. Instead, circular drain electrode is surrounded by the gate electrode so that the gate controls all the current flowing between source and drain through the AlGaN/GaN channel. Clear differences between the circular and rectangular device characteristics were observed when they were measured at high temperatures. The transfer characteristic and gate current of the rectangular device measured at high temperatures are shown in Fig. 2c and 2d. The rectangular device also showed stable operation up to 400 °C with steep subthreshold slope and suppressed gate current. The threshold voltage of the rectangular device showed similar values and trend at high temperatures when compared to the circular device characteristic. However, the off-state current of the rectangular device was much larger than that of the circular device. The off-state drain current of the rectangular and circular devices measured at $V_{GS} = -18$ V and $V_{DS} = 1$ V is shown in Fig. 2e. It is obvious that the off-state current increases as the temperature increases for both types of devices. In the temperature range between the room temperature and 400 °C, off-state current of the rectangular device was more than 3 orders of magnitude larger than that of the circular device. For the rectangular device, since gate current is always much smaller than the off-state drain current, gate leakage is not the main contributor of the off-state drain current. Therefore, off-state current conduction primarily occurs between the drain and source on the surface of the etched GaN. Two-dimensional variable range hopping (2D-VRH) would be the main conduction mechanism. To clarify this, the logarithmic off-state channel conductance was plotted as a function of cube root of temperature, as shown in Fig. 2f. The off-state channel conductance was measured for both circular and rectangular devices with $V_{GS} = -18$ V, from 25 °C to 400 °C in 25 °C step. The temperature dependent conductance of the 2D-VRH conduction can be described as the following formula:

$$\sigma \propto exp\left[-\left(\frac{1}{T}\right)^{\frac{1}{3}}\right]. \quad (1)$$

From the linear fitting of the plot, it is clear that the off-state current conductance of the rectangular device follows the formula until it reaches 300 °C, which confirms that the off-state current conduction of the rectangular device is dominated by 2D-VRH taking place at the interface between GaN and silicon nitride. Note that the conductance starts to deviate from the linear trend at temperatures higher than 300 °C, which implies existence of the additional current component at extreme high temperature. On the contrary, off-state conductance of the circular device does not follow such trend, indicating that 2D-VRH is not the primary off-state current conduction mechanism for the circular device. When the mesa isolation is made by ICP-RIE for the rectangular device, AlGaN layer outside of the active rectangular region was etched away and bare GaN surface was revealed. This etching process will induce damage and form interface states on the surface of the GaN layer, which act as the source of 2D-VRH. Since both rectangular and circular devices showed stable high temperature operation, and both devices have similar device characteristics except the off-state current, both device structures can be considered for high temperature purposes. If suppression of the off-state current and more stable device operation are required, circular device structure would be preferred.

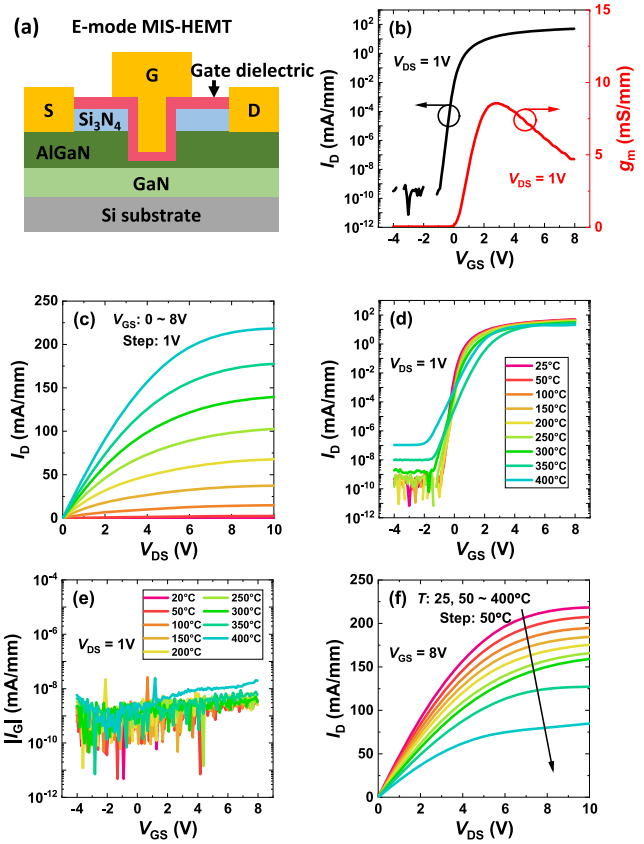

FIGURE 3. **(a) Schematic of an E-mode circular AlGaN/GaN MIS-HEMT with gate recess. A thin layer of AlGaN layer is remained in the gate region to protect the GaN surface. (b) Transfer characteristic, transconductance, and (c) output characteristics of an E-mode circular MIS-HEMT at room temperature. (d) Transfer characteristics, (e) gate current, and (f) output characteristics of the E-mode MIS-HEMT at high temperature.**

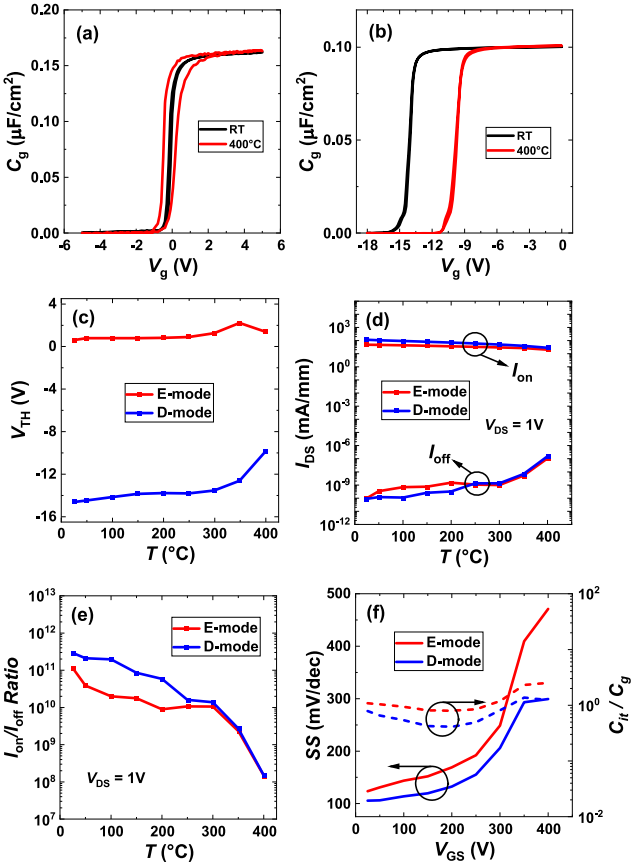

FIGURE 4. **Comparison of thermal stability of E-mode and D-mode AlGaN/GaN MIS-HEMTs. Gate capacitance measured from (a) E-mode and (b) D-mode capacitor devices at room temperature and 400 °C. (c) Threshold voltage, (d) on-state current and off-state current of the circular E-mode and D-mode devices at high temperatures. (e) Ion/Ioff ratio of the circular E-mode and D-mode devices at high temperatures. (f) Average subthreshold swing and interface-trap capacitance of the E-mode and D-mode devices at high temperatures.**

By using the atomic layer etching and forming the gate recess with 4.3 nm of remaining AlGaN layer, E-mode AlGaN/GaN circular MIS-HEMT was fabricated, as illustrated in Fig. 3a. The transfer characteristic and output characteristic at room temperature are shown in Fig. 3b and 3c. Due to the gate recess structure, negligible amount of two-dimensional electron gas (2DEG) at the AlGaN/GaN interface was remaining in the E-mode devices [18], and positive threshold voltage of 0.6 V was extracted using the linear extrapolation method [19]. Reasonably large maximum current (218 mA/mm) and peak transconductance (30.1 mS/mm) were obtained, considering that gate capacitance was small due to the thick tri-layer gate dielectric. This device was also tested at high temperatures. Temperature dependence of the transfer characteristics, gate current and output characteristics are shown in Fig. 3d, 3, and 3f. The E-mode circular device maintained stable operation with steep threshold slope and suppressed off-state current. Suppressed gate current indicates stability of the tri-layer gate dielectric. Output characteristic also showed monotonic decrease as the temperature increases due to the increased phonon scattering.

Capacitance of the gate stack was measured at 25 °C and 400 °C for both E-mode and D-mode devices from the separate diode devices fabricated together with MIS-HEMTs (Fig. 4a and 4b). Capacitance of the E-mode gate stack showed larger hysteresis at 400 °C compared to the room temperature measurement result, whereas D-mode gate stack capacitance showed small hysteresis even at 400 °C. The larger hysteresis of E-mode device can be attributed to the higher density of interface traps at the gate dielectric/AlGaN interface induced by the gate recess process. As the temperature increases, defect assisted conduction via AlGaN layer or dielectric layer increases, and the interface traps can be depleted and refilled more easily, which leads to larger hysteresis [10]. Positive flatband voltage shift was also observed for the D-mode gate stack capacitance. For both E-mode and D-mode devices, the gate capacitance values were nearly unchanged throughout the whole temperature range.

Temperature dependence of the threshold voltage of the E-mode and D-mode devices is shown in Fig. 4c. Overall,

threshold voltage of the E-mode device was stable throughout the temperature range, whereas the D-mode device showed gradual increase of the threshold voltage, especially between 300 °C and 400 °C. E-mode device maintained normally-off behavior at all the temperatures. To the best of the authors' knowledge, this is the first demonstration of the normally-off AlGaN/GaN MIS-HEMT operating up to 400 °C. We believe AlGaN strain relaxation starts to occur at around 350 °C due to thermal stress. It has been reported in several studies that AlGaN barrier layers exhibit significant strain relaxation above 300 °C [3], [5], [20]. Since AlGaN strain relaxation involves reduction of the amount of 2DEG, it is the primary reason for the sudden increase of the D-mode device threshold voltage at high temperature, considering the temperature independence of gate capacitance for both E-mode and D-mode devices. The effect of the strain relaxation was smaller in the case of the E-mode device due to the very thin AlGaN layer retained under the gate of the E-mode device.

On-state and off-state drain currents measured on the circular E-mode and D-mode devices with $V_{DS} = 1$ V are shown in Fig. 4d, and the calculated on/off ratios were plotted as functions of temperature shown in Fig. 4e. At room temperature, both devices have a large Ion/Ioff ratio around 10^{11}, and the ratio gradually decreases as the temperature increases. Since the off-state current does not show dependence on the gate bias at high temperatures, we believe that the off-state current is dominated by the bulk leakage current that flows through the UID GaN layer. By taking advantage of the extremely small intrinsic carrier concentration of GaN, off-state current is greatly suppressed at high temperatures, which enables record high Ion/Ioff ratio around 10^8 at 400 °C.

Average subthreshold swing (SS) and interface trap capacitance at high temperature are plotted in Fig. 4f. For both E-mode and D-mode MIS-HEMTs, subthreshold swing increased as the temperature increased, and the amount of increase got larger at higher temperature. Subthreshold swing can be obtained from the following equation:

$$SS = \frac{k_B T}{q} \ln(10)\left(1 + \frac{C_Q + C_{it}}{C_g}\right), \quad (2)$$

where k_B is Boltzmann constant, T is temperature, q is elementary charge, C_Q is quantum capacitance at the AlGaN/GaN interface, C_{it} is interface trap capacitance, and C_g is gate capacitance [21]. Considering that C_Q is negligible, ratio between the interface trap capacitance and the gate capacitance could be calculated. Note the gate capacitance is nearly temperature independent as shown in Fig. 4a and 4b. We can see that the interface trap capacitance of the D-mode device at 400 °C is nearly the same as that at 350 °C. This result indicates that interface trap is not the primary cause of the dramatic increase of threshold voltage in the D-mode device between 350 °C and 400 °C, which further confirms that strain relaxation is the key mechanism for the threshold voltage shift in this case. It is worth mentioning that the trap density at the dielectric/AlGaN interface stayed stable overall for both E-mode and D-mode MIS-HEMTs, which contributed to the high thermal stability of these devices.

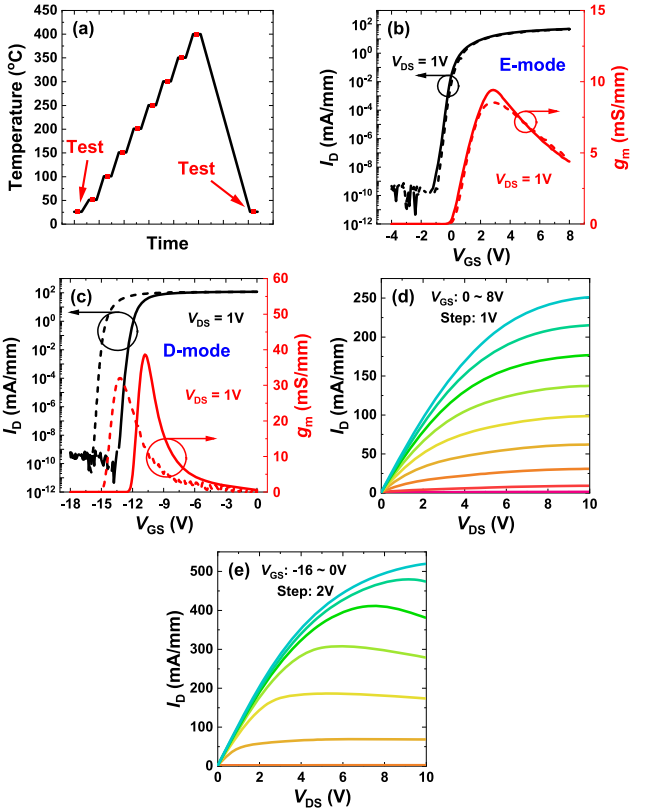

FIGURE 5. Reversibility of E-mode and D-mode AlGaN/GaN MIS-HEMTs. (a) Temperature profile of the thermal stress and the measurement before and after thermal stress. Transfer characteristic and transconductance of the (b) E-mode and (c) D-mode devices after high temperature operation. Dashed lines represent the initial characteristics measured at room temperature before heating up, and solid lines represent the characteristics measured at room temperature after cooldown. Output characteristic of the (d) E-mode and (e) D-mode devices measured at room temperature after the thermal stress.

Transfer characteristic of the E-mode and D-mode devices after the high temperature operation is compared with the initial characteristic before the high temperature operation. During the high temperature operation, the device was measured at each temperature for 30 min, and temperature ramp-up between each temperature took 20 min. The temperature profile for the thermal stress and measurement is illustrated in Fig. 5a. In the case of the E-mode device, negligible threshold voltage shift was observed, and the transconductance slightly increased from 30.1 mS/mm to 32.5 mS/mm (Fig. 5b). On the other hand, transfer curve of the D-mode device showed positive shift. Threshold voltage increased from −14.7 V to −12.1 V, and transconductance slightly increased from 56.4 mS/mm to 60.1 mS/mm (Fig. 5c). Output characteristics of the E-mode and D-mode

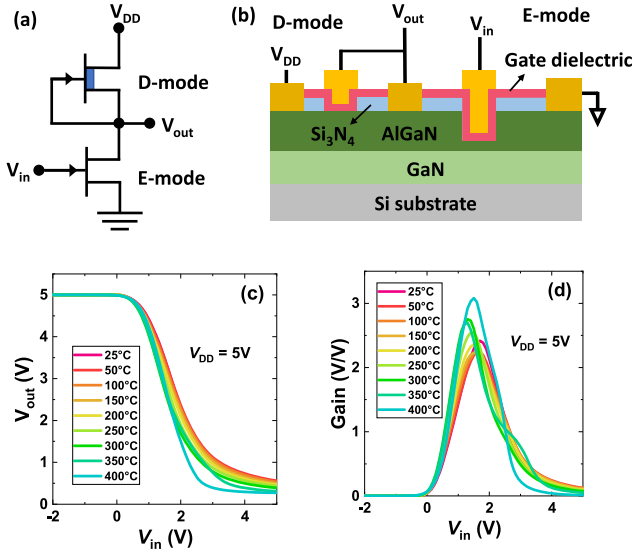

FIGURE 6. DCFL inverter based on E-mode and D-mode AlGaN/GaN MIS-HEMTs. (a) Circuit diagram and (b) device schematics of DCFL inverter based on E-mode and D-mode AlGaN/GaN MIS-HEMTs on the AlGaN/GaN substrate. (c) Transfer characteristics and (d) voltage gain of the DCFL inverter measured at various temperatures.

devices after the thermal stress are shown in Fig. 5d and 5e. Since transconductance and drain current did not decrease, it was clear that channel quality was not degraded during the high temperature operation. Therefore, the positive shift of the I_d-V_g curve of the D-mode device is mainly caused by the strain relaxation of AlGaN layer. Due to the thin retained AlGaN layer of the E-mode device, E-mode device showed good reversibility with negligible threshold voltage shift after the cooldown. Note that we observe the increase of Hall mobility and decrease of the 2DEG density after the thermal stress from Hall measurement for AlGaN/GaN sample, which further supports that the thermal stress induces AlGaN strain relaxation. Since the amount of mobility increase was larger than the decrease of 2DEG density, resistance of the access region decreases after the thermal stress, which would lead to the decrease of series resistance and increase of the drain current.

By connecting the E-mode and D-mode devices in series, a DCFL inverter was fabricated. The circuit diagram and device schematic of the DCFL inverter are illustrated in Fig. 6a and 6b. The ratio of the channel width of the E-mode and D-mode devices was 17.6:1 in the fabricated inverter. Transfer characteristic of this inverter was measured at high temperatures, and voltage gain was calculated (Fig. 6c and 6d). The transfer curve gradually shifted to the negative direction but did not show dramatic distortion until the temperature reached 400 °C. Gain of the inverter also did not show the large variation. Peak gain of the inverter gradually increased as the temperature increases. This indicates that both devices operated without severe thermal degradation, and threshold voltage stability of the E-mode device is maintained even after integrated into the inverter.

IV. CONCLUSION

By conjunctively using circular device structure and atomic layer etched gate recess, we demonstrated stable operation of the E-mode and D-mode AlGaN/GaN MIS-HEMT up to 400 °C. The devices showed record high Ion/Ioff ratio around 10^8 and large transconductance of 21.4 mS/mm and 19.1 mS/mm at 400 °C. E-mode device maintained normally-off operation at high temperatures with stable threshold voltage, whereas D-mode device showed gradual shift of the threshold voltage due to strain relaxation. DCFL inverter was fabricated with E-mode and D-mode devices and showed stable transfer characteristics at high temperatures, which indicates the feasibility of high temperature logic and memory.

REFERENCES

[1] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics—A role for wide bandgap semiconductors?" *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002, doi: 10.1109/JPROC.2002.1021571.

[2] N. Maeda, K. Tsubaki, T. Saitoh, and N. Kobayashi, "High-temperature electron transport properties in AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 79, no. 11, pp. 1634–1636, Sep. 2001, doi: 10.1063/1.1400779.

[3] Y. Q. Tao et al., "High-temperature transport properties of 2DEG in AlGaN/GaN heterostructures," *J. Electron. Mater.*, vol. 35, no. 4, pp. 722–725, Apr. 2006, doi: 10.1007/s11664-006-0128-7.

[4] A. Hassan, Y. Savaria, and M. Sawan, "GaN integration technology, an ideal candidate for high-temperature applications: A review," *IEEE Access*, vol. 6, pp. 78790–78802, 2018, doi: 10.1109/ACCESS.2018.2885285.

[5] P. H. Carey et al., "Extreme temperature operation of ultra-wide bandgap AlGaN high electron mobility transistors," *IEEE Trans. Semicond. Manuf.*, vol. 32, no. 4, pp. 473–477, Nov. 2019, doi: 10.1109/TSM.2019.2932074.

[6] M. N. Yoder, "Wide bandgap semiconductor materials and devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1633–1636, Oct. 1996, doi: 10.1109/16.536807.

[7] S. Kargarrazi, A. S. Yalamarthy, P. F. Satterthwaite, S. W. Blankenberg, C. Chapin, and D. G. Senesky, "Stable operation of AlGaN/GaN HEMTs for 25 h at 400 °C in air," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 931–935, 2019, doi: 10.1109/JEDS.2019.2937008.

[8] A. J. Suria, A. S. Yalamarthy, H. So, and D. G. Senesky, "DC characteristics of ALD-grown Al_2O_3/AlGaN/GaN MIS-HEMTs and HEMTs at 600 °C in air," *Semicond. Sci. Technol.*, vol. 31, no. 11, Oct. 2016, Art. no. 115017, doi: 10.1088/0268-1242/31/11/115017.

[9] Y. Cai, Z. Cheng, Z. Yang, C. W. Tang, K. M. Lau, and K. J. Chen, "High-temperature operation of AlGaN/GaN HEMTs direct-coupled FET logic (DCFL) integrated circuits," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 328–331, May 2007, doi: 10.1109/LED.2007.895391.

[10] M. Meneghini et al., "Negative bias-induced threshold voltage instability in GaN-on-Si power HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 474–477, Apr. 2016, doi: 10.1109/LED.2016.2530693.

[11] F. Husna, M. Lachab, M. Sultana, V. Adivarahan, Q. Fareed, and A. Khan, "High-temperature performance of AlGaN/GaN MOSHEMT with SiO_2 gate insulator fabricated on Si (111) substrate," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2424–2429, Sep. 2012, doi: 10.1109/TED.2012.2204888.

[12] S. Yang, S. Liu, C. Liu, Z. Tang, Y. Lu, and K. J. Chen, "Thermally induced threshold voltage instability of III-nitride MIS-HEMTs and MOSC-HEMTs: Underlying mechanisms and optimization schemes," in *IEDM Tech. Dig.*, Dec. 2014, pp. 1–4, doi: 10.1109/IEDM.2014.7047069.

[13] C. Liu et al., "Thermally stable enhancement-mode GaN metal-isolator-semiconductor high-electron-mobility transistor with partially recessed fluorine-implanted barrier," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 318–320, Apr. 2015, doi: 10.1109/LED.2015.2403954.

[14] J. He, M. Hua, Z. Zhang, and K. J. Chen, "Performance and stability in E-mode GaN fully recessed MIS-FETs and partially recessed MIS-HEMTs with LPCVD-SiNx /PECVD-SiNx gate dielectric stack," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3185–3191, Aug. 2018, doi: 10.1109/TED.2018.2850042.

[15] R. Sarkar et al., "Epi-Gd_2O_3-MOSHEMT: A potential solution toward leveraging the application of AlGaN/GaN/Si HEMT with improved I_{ON}/I_{OFF} operating at 473 K," *IEEE Trans. Electron Devices*, vol. 68, no. 6, pp. 2653–2660, Jun. 2021, doi: 10.1109/TED.2021.3070838.

[16] H. Sun et al., "Fabrication of high-uniformity and high-reliability Si_3N_4/AlGaN/GaN MIS-HEMTs with self-terminating dielectric etching process in a 150-mm Si foundry," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4814–4819, Nov. 2018, doi: 10.1109/TED.2018.2869703.

[17] J. Zhu et al., "Variable range hopping mechanism and modeling of isolation leakage current in GaN-based high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 116, no. 22, Jun. 2020, Art. no. 222101, doi: 10.1063/5.0004957.

[18] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 356–362, Feb. 2006, doi: 10.1109/TED.2005.862708.

[19] D. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2006, ch. 6.

[20] D. J. Chen et al., "Temperature-dependent strain relaxation of the AlGaN barrier in AlGaN/GaN heterostructures with and without Si_3N_4 surface passivation," *Appl. Phys. Lett.*, vol. 88, no. 10, Mar. 2006, Art. no. 102106, doi: 10.1063/1.2186369.

[21] J. Chung, X. Zhao, and T. Palacios, "Estimation of trap density in AlGaN/GaN HEMTs from subthreshold slope study," in *Proc. 65th Annu. Device Res. Conf.*, 2007, pp. 111–112, doi: 10.1109/DRC.2007.4373674.