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Development and Challenges of Reliability Modeling From Transistors to Circuits

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ABSTRACT The integration density of electronic systems is limited by the reliability of the integrated circuits. To guarantee the overall performance, the integrated circuit reliability must be modeled and analyzed at the early design stage. This paper reviews some of the most important intrinsic aging mechanisms of MOSFETs and elaborates the physical mechanism of the coupling between aging effects. Then the progress in reliability modeling under static and dynamic operational voltages is reviewed. It is found that although these models can accurately predict the degradation in short term, they are with large errors for the long-term degradation prediction. Besides, for the circuit-level reliability modeling and simulation approach, there are still problems to be solved. This article aims to provide guidance for researchers and practitioners in integrated circuit field, and highlight the challenges for reliability research. It is of great significance to the optimization of the reliability of integrated circuits.

INDEX TERMS Aging model, circuit reliability, bias temperature instability (BTI), hot-carrier injection (HCI), SPICE simulation.

I. INTRODUCTION

The downscaling rate of the supply voltage is slower than that of its size for the transistors, which results in soaring current density and temperature in the transistor channel, and accelerated transistor degradation. Therefore, aggressive transistor downscaling causes unavoidable reliability issues in modern integrated circuits (IC). On the one hand, among all the reliability issues, the aging effects such as bias temperature instability (BTI) [1], [2], [3] and hot carrier injection (HCI) [4], [5], [6] manifest themselves as an increase in the absolute threshold voltage (V_{th}) and reduction in the carrier mobility (μ), thus gradually degrading circuit performance [7], [8]. On the other hand, there are booming demand of high reliability circuits in the markets of autonomous vehicles, space operations and biomedical electronics. To have a better analysis of the circuit degradation and improve its lifetime, it is necessary to conduct degradation modeling and simulation at the early design stage of circuits.

The studies describing aging mechanisms have matured as a result of years of refinement to the existing theories. Many previous works have been done to extend the aging models for transistors to a circuit-level reliability analysis [9], [10], [11], [12]. However, there are difficulties to achieve that. At the circuit level, BTI and HCI can occur either simultaneously or sequentially, and the two effects could also interact with each other, which makes the modeling difficult. The model only considering one degradation mechanism is difficult to accurately predict the lifetime of the circuit, causing an unnecessary compromise in IC design. A physical-based reliability model that can deliver accurate lifetime prediction at both transistor and circuit levels is urgently required, while there are still challenges in accurate modeling of the aging effect at the moment.

In this review, we take a comprehensive look at the progress of the reliability research. First, we briefly introduce the main reliability physics mechanism and the coupling between them. Next, we provide a comprehensive survey of the reliability models for BTI and HCI. Then, the relationship between the transistor degradation model and circuit lifetime prediction is studied. At the end of this paper, we summarize

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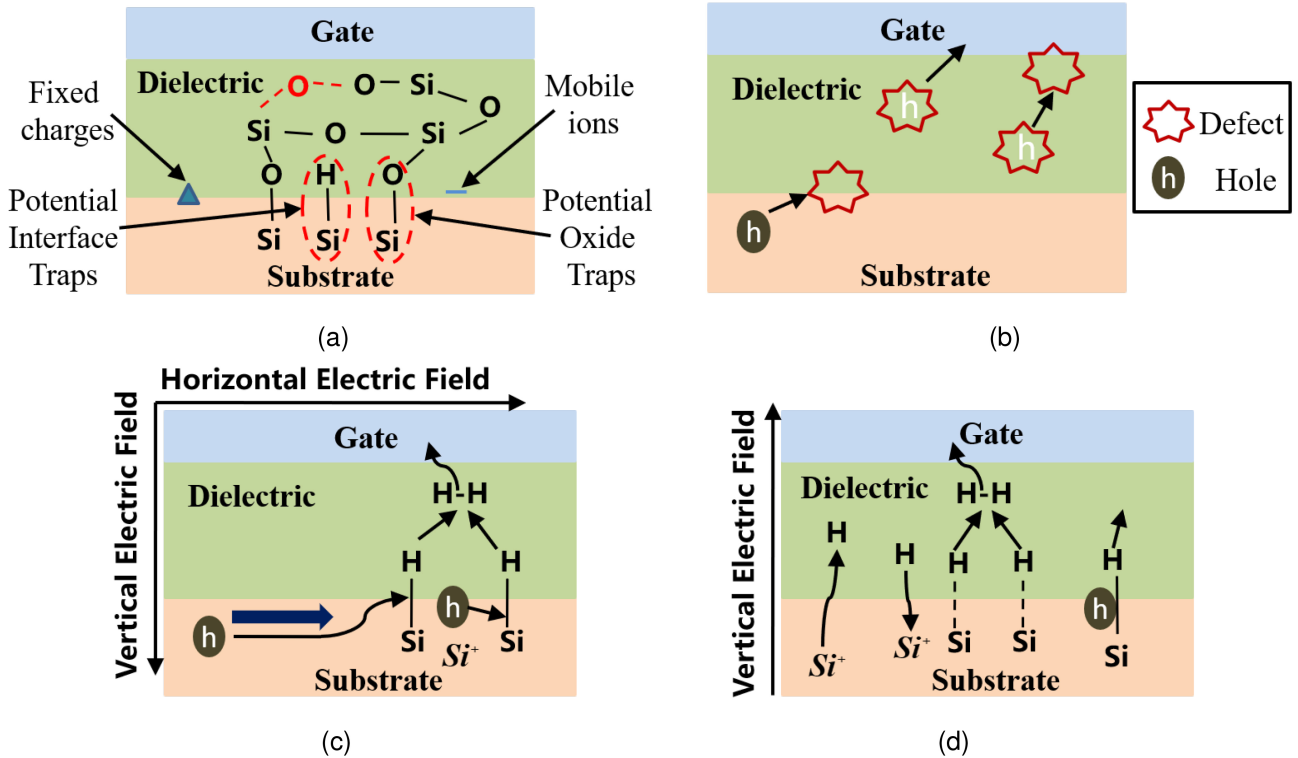

FIGURE 1. Key factors for the degradation of PMOS transistor. (a) The four types of charge distribution in the oxide layer. (b) The process of trapping holes by defects at the substrate/dielectric layer interface. (c) The process of interface trap generation for HCI effect. (d) The process of interface trap generation and recovery for NBTI effect.

the challenges of reliability simulation and potential ways of pushing forward researches of this field.

II. RESEARCH ON MOSFET DEGRADATION MECHANISMS

The basis of studying the degradation mechanism is the analysis of the defect state inside the transistors, for which the most direct method is to measure the defect density generated by the degradation mechanism. Charge pumping and low-frequency noise 1/f measurements are widely used to evaluate the defects state [13], [14], [15]. Besides the study on the trap spatial distribution of high-k and ultra-thin oxide layer, charge pumping techniques based on the variation of the charge pumped with frequency and employed ring-oscillator-connected devices are proposed in [16], [17]. According to the analysis of the trap density, some literatures have focused on revealing the physical mechanisms underlying aging in semiconductor devices [18], [19], [20], [21], [22], [23], [24], [25], [26], [27].

From the physical mechanisms, it can be found that charge distribution in the gate oxide layer mainly includes four types: potential interface traps, potential oxide traps, mobile ions and fixed charges, as shown in Fig. 1(a). The interface of Si/SiO_2 have some defects, trapping holes and degrading the transistor performance, as shown in Fig. 1(b). Due to the non-epitaxial amorphous structure on the crystalline silicon, the Si – H or Si – O bonds are prone to dissociate at the substrate/gate oxide interface. When an electric field between gate and source is applied, holes can be captured by these bonds, resulting in the bond break [19], [20], as seen in Fig. 1(c) and Fig. 1(d). These are the key factors for the parameter degradation of transistors.

A. HOT CARRIER INJECTION

As described in the literature [21], [22], HCI occurs as carriers shoot out from the source of a transistor, accelerated in the channel, and experiencing ionization near the end of the drain. As shown in Fig. 2(a), these carriers at the drain gaining sufficient energy to be injected into the gate oxide is called the drain avalanche hot carrier (DAHC). This effect generally occurs at the stress conditions with high drain voltage and low gate voltage. When the gate voltage is approximately equal to the drain voltage, carriers gain sufficient energy to penetrate the Si/SiO_2 barrier at the end of the drain in the channel, without losing energy due to collisions with atoms in the channel, which is called the channel hot electron (CHE) injection effect, as shown in Fig. 2(b).

The hot-carrier-induced damage has been found to cause either trapping of carriers on defect sites in the oxide or the creation of interface states at the silicon-oxide interface, or both. The damages cause a degradation in its transconductance (G_m), a shift in the threshold voltage (V_{th}), and a decrease in drain current (I_{ds}). Since the carrier velocity, which decides the trapping process rate, is sensitive to the

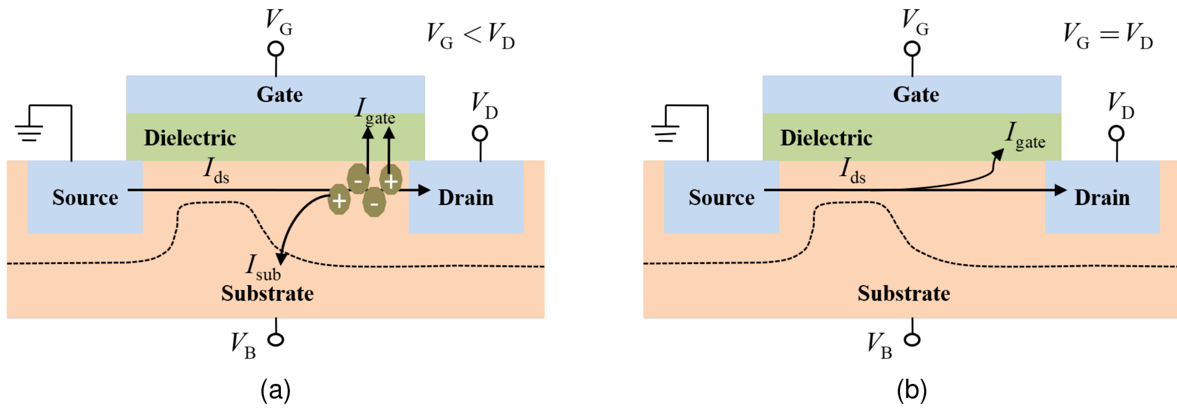

FIGURE 2. Two mechanisms of HCI effect. (a) DAHC. (b) CHE.

electric field, temperature, and frequency, thus HCI effect is a complex function of these factors [23].

B. BIAS TEMPERATURE INSTABILITY

BTI includes negative BTI in PMOS and similar wear-out positive BTI in more advanced high-k metal gate NMOS transistors. Based on published works, both reaction-diffusion (RD) [24] and trapping/de-trapping (TD) [25] theories could explain the process of the BTI effect in current semiconductor devices.

The major difference between the two theories is the nature of the diffusing behaviors and the medium that facilitates the diffusion. In the RD theory, the reaction process is that the Si – H or Si – O bonds triggered by hot holes in NBTI or hot electrons in HCI are broken. The diffusion process is that the reaction-generated carriers diffuse away from the interface toward the gate, driven by the gradient of the carrier density. When the stress voltage is removed, they diffuse back toward the interface, re-passivating the broken bond and restoring some of the degradation from NBTI, as shown in Fig. 1(d). The TD theory essentially elaborates the capture and emission mechanism of the oxide traps, as shown in Fig. 3. When gate voltage is positive, a positive electric field is formed across the channel interface, positive charges are captured by acceptor-type traps and negative charges are emitted from the donor-type traps. Positive gate bias leads to positive drift while negative gate bias leads to negative drift [26].

According to the mechanism of single aging effect, it can be found that the traps generated by the BTI effect are distributed uniformly in the channel, while the traps generated by the HCI effect are mainly at the drain end [27]. When operating voltages are applied to both gate and drain of the transistor, the traps created by the two aging effects will work together. As shown in Fig. 4, there is trap competition at the drain end. Therefore, the two mechanisms can occur either simultaneously or sequentially, and they can also interact with each other. In practice, BTI and HCI can occur sequentially in transistors in ring oscillators. The final degradation is much smaller than summing the degradation

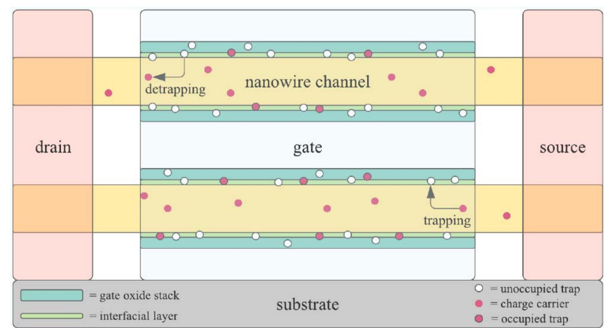

FIGURE 3. Simplified demonstration of BTI trapping/detrapping model.

induced by each mechanism alone. This can be understood like this: although occurring at different energy/spatial locations, both mechanisms are related to similar types of traps. Therefore, the increase of traps induced by one mechanism will suppress the degradation caused by the following stress. Without considering such coupling effect, the degradation can be overestimated. However, there is limited research on this case, most studies consider only the dominant mechanisms and ignore the secondary ones. With the decreasing of transistor size in advanced technologies, such coupling effect will become stronger. It is necessary to analyze the decoupling method and establish a more accurate physical model.

III. THE RELIABILITY MODEL IN TRANSISTOR LEVEL

In order to evaluate the transistor's lifetime and optimize its reliability, it is crucial to establish aging models based on the degradation mechanisms. The prerequisite for accurate modeling is to obtain the degradation data of the transistors. For the sake of time-save, over-biased voltage and temperature stress are applied in the experiments to accelerate the degradation. Conventionally, the value of stress is confirmed based on the substrate current (I_{sub}) measurement [28]. Then I-V test is used to measure the parameters shift of the transistor after degradation. However, when testing I_{sub}, it is difficult to clearly separate degradation data from noise in

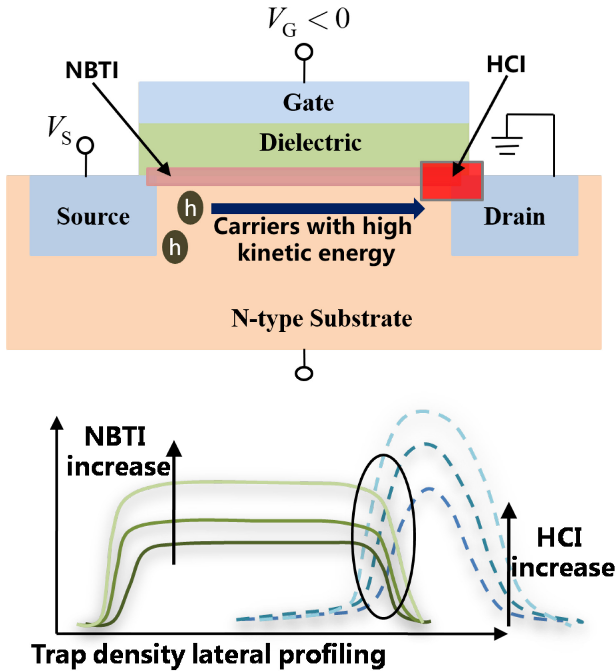

FIGURE 4. Defects location for coupling between HCI and BTI in a transistor.

practice. We adopt the voltage stress according to the median degradation of the electrical indicators for the aging test [29].

A. AGING MODEL UNDER STATIC STRESS

By studying the degradation mechanisms and incorporating test data of aging effects, a great number of studies have established BTI and HCI reliability models to estimate the transistor's expected lifetime. As shown in Table 1 (See [30], [32], [33], [34], [35], [36], [37], [38], [39] for more details), many aging models show that the degradation agrees with a power-law dependence on time except for [38]. It points out that degradation is log-dependent on time for BTI. Relevant verifications are also carried out in their experiments as shown in Fig. 5 and Fig. 6. We used the transistors of the 0.18 μm technology to test the HCI effect in [29]. The power-law relationship is verified again and the degradation value could saturate. Generally, the industry takes the degradation of 10% for I_{ds} or shift of 50 mv for V_{th} as the failure standard [40].

The degradation of transistor parameters predicted by these models is accurate in the short term. Among them, the degradation of transistor is mostly represented by the parameter V_{th} or I_{ds}. As shown in the these models, the relationship between parameter degradation and temperature conforms the Arrhenius equation. The degradation value induced by HCI is not only related to the stress voltage and temperature, but also to the transistor size. This is because the degradation is mainly caused by the trapped charges at the junction, which is caused by the impact ionization. The ionization probability decreases dramatically when the size of transistors increases. Compared with the transistors of smaller sizes, the impact of ionization for the larger size ones is less severe, resulting in fewer interface states and oxide traps.

According to the current research, it is founded that the HCI effect is affected by the drain voltage (V_{ds}), the gate voltage (V_{gs}) and temperature, while NBTI is only affected by V_{gs} and temperature, and its relationship with V_{ds} remains unclear. We summarize the degradation model at transistor level for calculating the HCI and BTI effect under static stress as:

$$\Delta P_{\text{HCI}} = A_{\text{HCI}} \cdot {V_{\text{gs}}}^{r_vgs} \cdot {V_{\text{ds}}}^{r_vds} \cdot L^{r_L} \cdot W^{r_W} \cdot t^n \cdot e^{-\frac{E_a}{k_B T}} \tag{1}$$

$$\Delta P_{\text{BTI}} = A_{BTI} \cdot {V_{\text{gs}}}^{r_vgs} \cdot e^{-\frac{E_a}{k_B T}} \cdot t^n \tag{2}$$

TABLE 1. Transistor aging models under static voltage stress.

Model formula	Ref
$\Delta I_{\text{dslin}} = A \cdot t^{\text{n}}$	[30]
$\Delta I_{\text{on}} = A \cdot e^{\frac{E_a}{k_B T}} \cdot V^b \cdot L^{-\text{m}} \cdot t^{\text{n}}_{\text{stress}}$	[32]
$\Delta V_{th} = A \cdot t^n \cdot V_{gs}^m$	[33]
$\Delta V_{\text{th}} = A\left(\frac{I_{\text{ds}}}{W}\right)^{\text{n}}\left(\frac{I_{\text{sub}}}{I_{\text{ds}}}\right)^{\text{m}} L^{-\text{p}} t^{\text{n}} \exp\left(-\frac{E_a}{k\left(\frac{T_{\text{ref}}-T}{T \cdot T_{\text{ref}}}\right)}\right)$	[34]
$\Delta V_{th} = A \cdot \exp\left(-\frac{E_a}{KT}\right) \cdot V^{\alpha} \cdot t^n$	[35]
$\Delta V_{\text{th}} = W^{-\text{a}} \cdot L^{-\text{b}} \cdot \exp\left(-\frac{c}{\lvert V_{\text{gs}}\rvert}\right) \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot t^n$	[36]
$\Delta V_{th} = \frac{q}{C_{ox}} K_2 \sqrt{Q_i} \exp\left(\frac{E_{ox}}{E_0}\right) \cdot \exp\left(a \cdot \frac{E_m - \varphi_{it}}{\lambda}\right) t^n$	[37]
$\Delta V_{th} = \phi\left[A + B \log\left(1 + Ct\right)\right]$	[38]
$\Delta I_{\text{dsat}} = A \cdot L^{\alpha} \cdot \exp\left(-\frac{\beta}{V_{\text{ds}}}\right) \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot t^n$	[39]

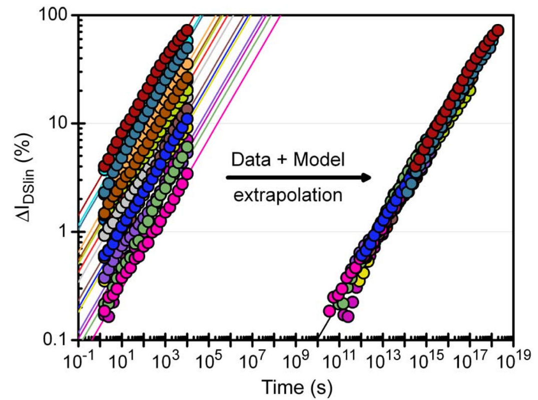

FIGURE 5. An extrapolation of the experimental data and the model is done at nominal bias condition showing a single power law trend in [30].

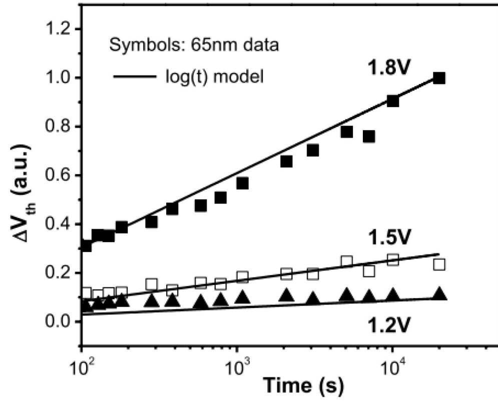

FIGURE 6. TD-based compact model matches the logarithmic time dependence and exponential voltage dependence in [36].

$$\Delta P_{\mathrm{BTI}} = \phi\left[A + B\log(1+Ct)\right] \quad (3)$$

where, ΔP is the degradation of the transistor parameters, such as the shift of V_{th} and G_{m}. n, r_vds, r_vgs, r_L, r_W and A are the model parameters that need to be extracted by data fitting. t is the stress time. W and L are the width and length of the transistor, respectively. The size and temperature parameters in (1) are integrated into A for calculation in some literature [30], [31]. Likewise, (2) and (3) indicate that the degradation caused by BTI conforms to the power law (short term) and logarithmic (long term) relationship with time, respectively.

The above mentioned studies are static stress related. However, transistors are seldom applied with static operation voltage (SOV). Instead, transistors experience a series of dynamic voltages and various workloads in large systems. As a result, these models are likely to overestimate the degradation, and a large margin is designed in the circuit to guarantee the functions over the entire lifetime.

B. AGING MODEL UNDER DYNAMIC STRESS

Accordingly, some researchers have carried out works predicting the lifetime of transistors under dynamic operation voltage (DOV), as shown in Table 2 (See [32], [38], [40], [41], [42], [43], [44] for more details). These models could be broadly divided into two categories. One is that the duty ratio factor added to the degradation model of SOV, as illustrated by the red color in Table 2, which is mainly for the HCI effect. The others are calculating the degradation value according to the stress state, mainly for the BTI effect. Relevant verification was also carried out in their experiments as shown in Fig. 7 and Fig. 8.

For the HCI effect under DOV, [45] concluded that the different alternating stresses can reduce or enhance the degradation, which mainly depends on the stress condition of the latter cycle, as shown in Fig. 9. HCI only occurs during switching under DOV, which is its transition from non-conducting to conducting state [43], as shown in Fig. 10. HCI-induced degradation is also affected by operating frequency [46], [47]. However, whether there is recovery phase in the HCI effect needs further study.

Although the degradation induced by BTI will have a partial recovery phase under DOV, the recovery phase does not fully reverse the aging process. Therefore, NBTI degradation under DOV stresses is modeled using a comprehensive framework [19], which can roughly predict the long-time degradation of transistors. In some works [48], [49] the aging model calculating the degradation induced by NBTI follows a logarithmic dependence on time under DOV stress.

Previous studies mainly focused on NBTI-only and ignored PBTI. Both the NBTI and PBTI are studied by applying a stochastic, workload-dependent, atomistic trap-based BTI model [50]. The impact of PBTI degradation may be lower, equal, or even higher than the NBTI impact [51]. The physical process of PBTI and NBTI is shown in Fig. 11, the voltage applied on the gate of transistors alternates continuously between on-state and off-state under dynamic gate stress. Holes will be captured under negative gate bias, while electrons will be captured under positive gate bias. The AC BTI depends on the capture efficiency of electrons and holes. In addition, [52], [53] indicate that acceptor-like interface traps, positive oxide charges, and neutral electron traps were generated by the off-state stress. They are accelerated by a high lateral electric field, inducing impact ionization, and causing reliability problems. By this token, the defects induced by the off-state stress should also be taken into account in the modeling.

TABLE 2. Transistor aging models under dynamic voltage stress.

Model formula	Ref
$\Delta V_{\mathrm{th}}(Stress) = A \cdot t^n \cdot e^{\Gamma E_{ox}} \cdot e^{\frac{-E_{AIT}}{kT}}$ $\Delta V_{\mathrm{th}}(\mathrm{Recovery}) = \Delta V_{th} \cdot e^{-\left(\frac{t}{\tau}\right)^{\beta}}$	[32]
$\Delta V_{th}(t+t_0) = \Delta_1 + \Delta_2$ $\Delta_1 = \phi\left[A + B\log(1+Ct)\right]$ $\Delta_2 = \Delta V_{th}(t_0)\left(1 - \frac{k+\log(1+Ct)}{k+\log(1+C(t+t_0))}\right)$	[38]
$\Delta V_{\mathrm{th}} = K \cdot \exp\left(\frac{B \cdot V}{t_{\mathrm{ox}}kT} - \frac{E_{\mathrm{a}}}{kT}\right) \cdot \log\left(1 + \frac{\frac{t_{\mathrm{s}}}{\tau_{\mathrm{c}}}}{1+\left(\frac{t_{\mathrm{s}}}{\tau_{\mathrm{c}}}\right)^{\beta}}\right)$	[40]
$\Delta V_{th} = f_{DOV}(sp) \cdot k_{SOV} \cdot t^n$	[41]
$\Delta V_{th} = A \cdot {V_{gstr}}^{\Gamma} \cdot e^{-\frac{Ea}{kT}} \cdot t_{str}^{n} \cdot PDC^{\alpha}$	[42]
$\Delta V_{\mathrm{th}} = \phi_0 \cdot \exp\left(-\frac{E_{\mathrm{a}}}{kT}\right) \cdot g\left(\frac{t_{\mathrm{stress}}}{t_{\mathrm{stress}}+t_{\mathrm{rec}}}\right)$ $\cdot \left(A + B\ln\left(t_{\mathrm{stress}} + t_{\mathrm{rec}}\right)\right)$	[43]
$\lvert\Delta V_{th}(t)\rvert \approx A \cdot SP^n \cdot t^n$	[44]

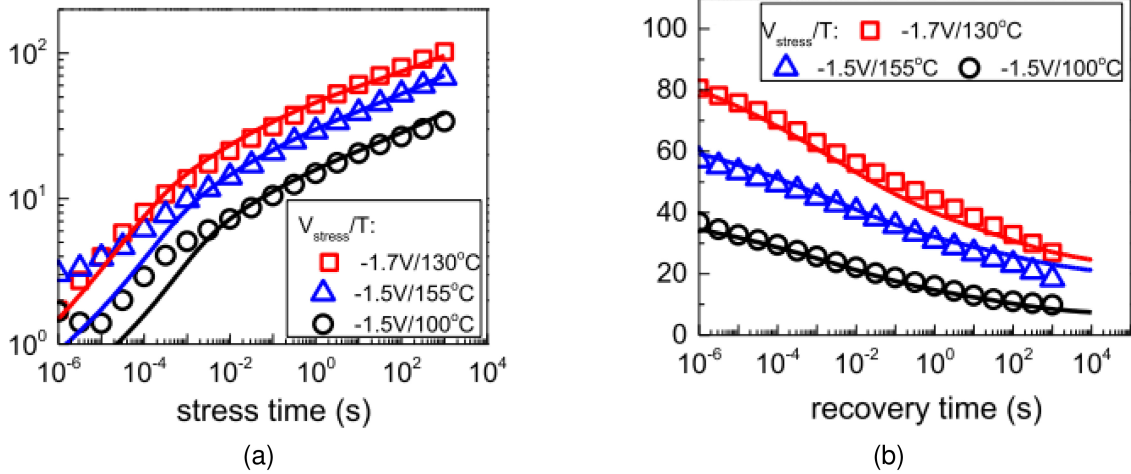

FIGURE 7. BTI-induced V_{th} degradation and recovery under stress for multiple Vdd, Temperature pairs in [32]. (a) Degradation. (b) Recovery.

The reliability models on the down-scaling transistors with new materials are also worth studying. For the transistors with novel materials, such as the typical *SiC* and *GaN* power devices, whose performance under dynamic bias gate stress have also been experimentally investigated in [54], [55]. A unified physical and statistical compact model of BTI on the down-scaling technology nodes was developed, which realized cycle-to-cycle/device-to-device reliability evaluations [56]. In [57], data from workloads through machine learning techniques were extracted to establish the aging model. But these studies are fairly preliminary at the moment.

It can be seen from the above studies that the degradation model development has experienced a shift from predicting short-term aging to predicting long-term aging. Long-term degradation needs to consider not only the off-state stress of the transistors but also the actual process and the operational conditions. In addition, modeling for the interaction of different aging mechanisms is still a challenge.

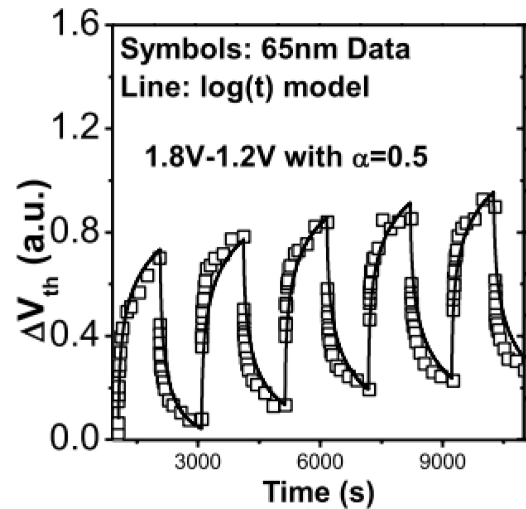

FIGURE 8. Validation of the model under different voltages and duty cycles in [38].

IV. CIRCUIT RELIABILITY ANALYSIS BASED ON TRANSISTOR AGING MODEL

The purpose of establishing the aging models is to accurately estimate the required guard bands in which the reliability can be sustained for the entire circuit lifetime. Once the long-term reliability of the circuit is estimated through simulation, the results can be compared with predetermined reliability specifications or limits. If the predicted reliability does not satisfy the requirements, appropriate design modifications will be carried out to improve.

To simulate the aging effect of transistors in the circuit functionality, the transistor-level aging effects can be characterized with some additional circuit elements in the SPICE model. For example, [39] use the voltage-controlled voltage source (VCVS) to characterize the V_{th} change due to the HCI effect, as illustrated in Fig. 12. The output voltage of the VCVS will become larger as the HCI effect intensifies. A voltage-controlled current source (VCCS) is used to characterize the decrease of I_{ds} caused by the HCI effect. Essentially, SPICE simulation is no more than solving a group of transistor-model equations to predict the interactions of all these transistors upon external stimuli. Therefore, circuit degradation can be viewed as the result that transistor-level aging effects express themselves at the circuit level by changing their model structures. As long as the change of transistor model structures can be correctly modeled with the inclusion of additional circuit elements, and the relations between these additional elements and the time-dependent aging parameters can be built and calibrated with simple testing work, then it is foreseeable that circuit-reliability simulation will become a natural and simple step of the overall circuit functional simulation.

Further, in the aspect of predicting the lifetime degradation of circuits, the aging models are developed independently from the transistor models, thus needing to be embedded into circuit simulation. The typical flow for circuit aging

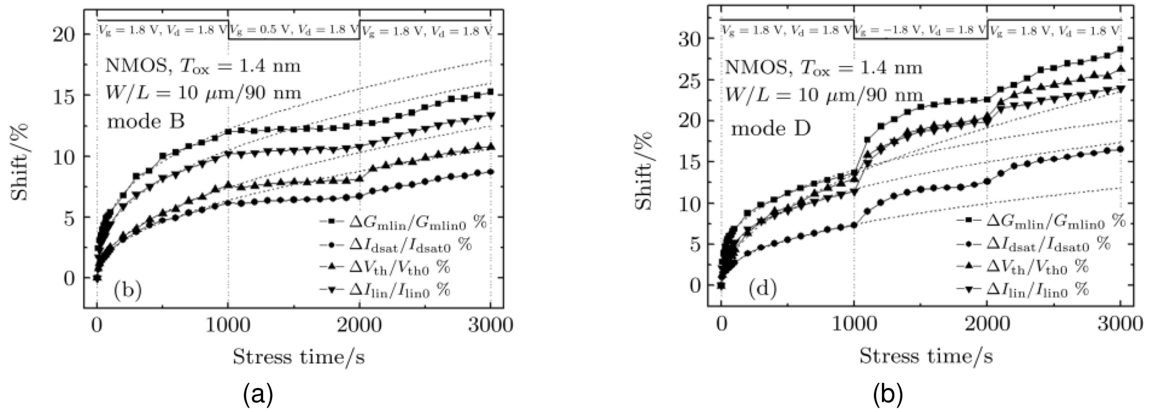

FIGURE 9. Parameters degradation under dynamic HCI stresses in [45]. (a) The stress of latter cycle is low voltage. (b) The stress of latter cycle is high voltage.

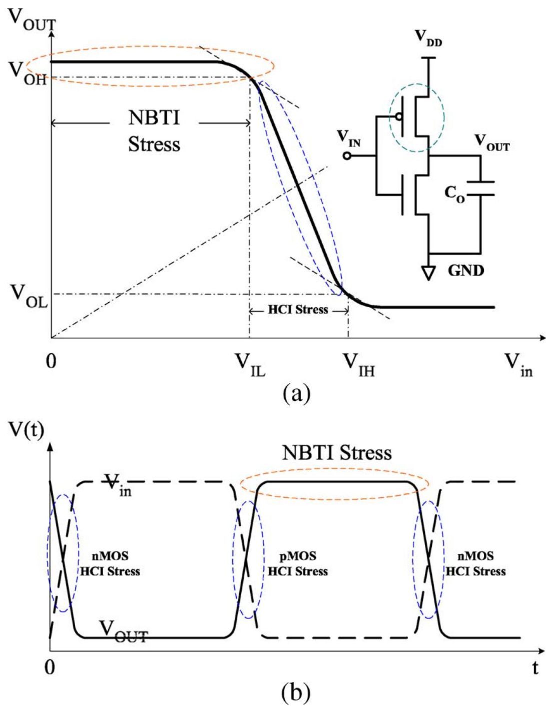

FIGURE 10. Different stress-time windows of HCI and NBTI for an inverter in [43]. (a) Voltage transfer curve plot. (b) Input–output waveform plot.

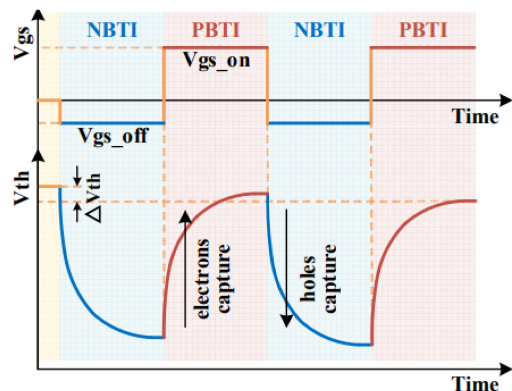

FIGURE 11. Two types of BTI effect under DOV stress.

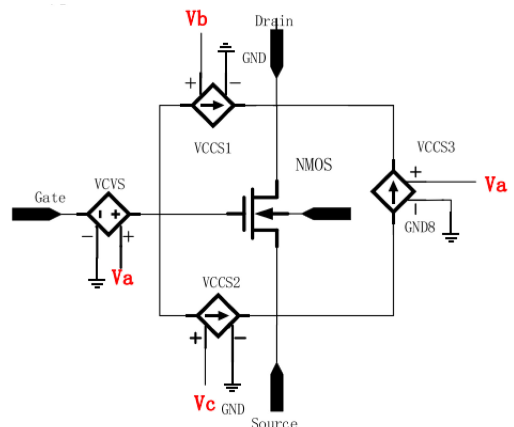

FIGURE 12. The equivalent circuit model of the HCI effect in [39].

simulators includes three steps. First, the investigated circuit is simulated without any aging, namely the fresh SPICE simulation. For each transistor, the state of the operation points it runs through are recorded. With the obtained information, the degradation values of the transistor parameters are calculated. This step is achieved through the Verilog-A module [58] as illustrated in Fig. 13(a). Then, the model parameters of the transistor are correspondingly changed. Finally, the circuit can be simulated again with newly adapted (aged) transistor model parameters, as illustrated in Fig. 13(b). This allows us to extract circuit performance under transistor degradation and identify the key issues at end of life. At each time step, the parameters of all transistors are updated and the corresponding new circuit conditions are used for the next iteration.

Based on these steps, in [44], [59], a simulation framework for studying the NBTI-induced delay degradation in circuits was discussed. As shown in Fig. 14, the lifetime is divided into N time periods, and the V_{th} degradation is calculated at the end of each time interval. The process continues till

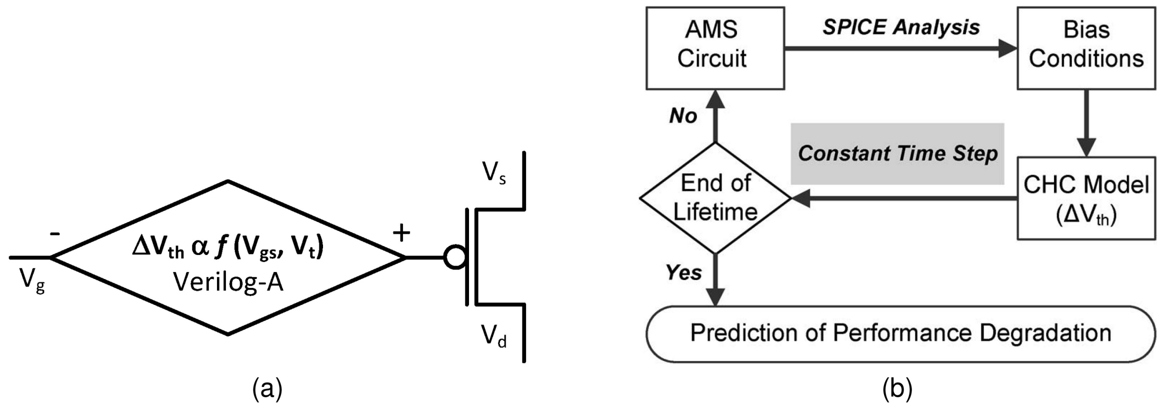

FIGURE 13. The calculation of circuit performance parameters after degradation in [58]. (a) The degradation value of transistor parameters are calculated based on Verilog-A module. (b) Circuit simulation based on the aging effect models of transistors.

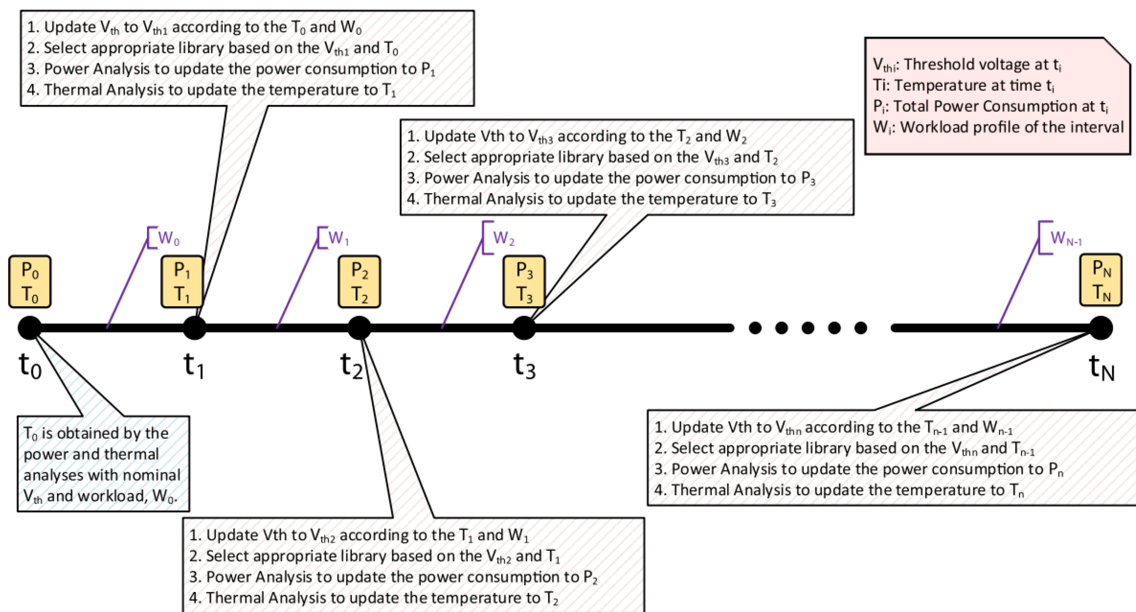

FIGURE 14. Flow of the proposed circuit simulation framework in [44].

reaching the end of the simulation time (10 years in this study). The timing degradation for the circuit is obtained at the end of the simulation. Reference [60] thoroughly investigated the influence of the BTI-induced transistor degradation on the dynamic write performance of a 20 nm bulk CMOS SRAM. As shown in Fig. 15, the aging model is also used to monitor the impact of mixed-mode stress on real circuits [61].

Nonetheless, the process variations (PVs) in manufacture and workload are also more and more important to the reliability evaluation of circuit. It could be too optimistic for circuit degradation without considering these factors. Thus, [41] proposed a new framework for analyzing the impact of BTI and PVs on large-scale digital logic circuits, reducing the complexity of circuit-level analysis and making it possible to handle large-scale circuits. A new V_{th} drift model was proposed and analysis the delay and subthreshold current of the circuit under the synergistic effect of BTI effect and PVs [62]. Besides, a framework considering interwoven effects of the workload and aging effect was proposed in [44], which studies the NBTI-induced delay degradation in digital circuits. The simulation setup for BTI degradation dynamically based on the workload during the simulation was introduced in [48], as shown in Fig. 16. The simulation setup consists of the transistor model which is combined with the model of BTI effect, and the V_{th} values of each transistor are dynamically updated during the simulation depending on the workload and time. The circuit simulations are conducted through SPICE or Spectre to get the circuit performance (i.e., delay).

At present, circuit reliability evaluation is mainly based on equivalent circuits or establishing the SPICE model of aging effect to update the model parameters of transistor after degradation. The degradation of transistor strongly depends on the ‘stress history,’ which is decided by its actual

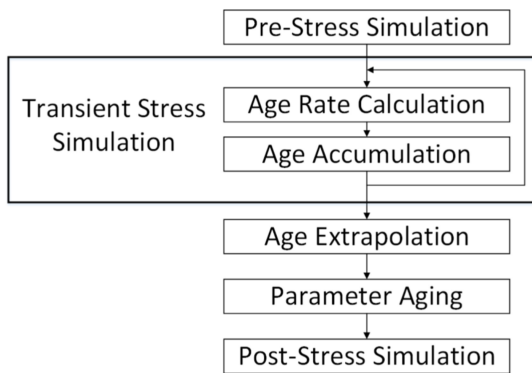

FIGURE 15. The flow diagram of aging simulation using Spectre in [61].

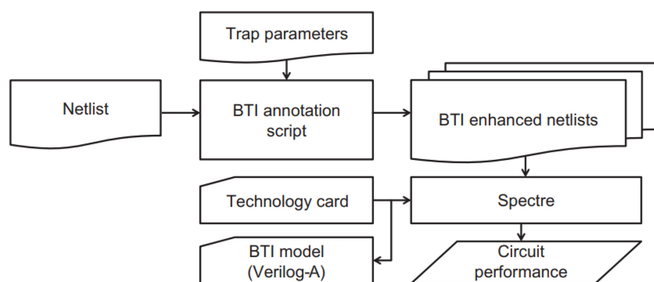

FIGURE 16. Simulation setup for the BTI degradation dynamically based on the workload in [48].

operation in the circuit. For circuit aging simulation, the degradation-, recovery- and variability-behavior have to be modeled as accurately as possible. Degradation can become permanent or compensated, depending on the order that the aging effects are activated during the circuit operation [63]. Thus, lifetime prediction procedures must take the aging mechanism interdependency into account.

The HCI and NBTI effects of transistors are tested using an efficient aging test method [29]. According to the I_{ds} degradation of different channel lengths, we found that there is no obvious channel length dependence for the degradation induced by NBTI. In addition, the degradation of I_{ds} caused by HCI decreases with increasing device size. In the long-channel transistor, the degradation of I_{ds} is small and can be ignored. Therefore, we test the I_{ds} degradation of 0.5 μm transistor by applying both voltage stress to the gate and drain (the conditions for the NBTI and HCI effects can be met). Likewise, we test the I_{ds} degradation of 0.18 μm transistor. In order to get the degradation of I_{ds} only induced by HCI, we subtract the I_{ds} degradation of 0.5 μm transistor from the I_{ds} degradation of 0.18 μm transistor. This is a way of decoupling aging effects. However, it is necessary to consider how to apply the decoupling method to the circuit reliability simulation.

V. SUMMARY AND CHALLENGE

The above-mentioned literatures show that the degradation of transistor performance can be calculated by the aging model under SOV or DOV. Then the degradation values can be converted into SPICE model parameters or equivalent circuit models to perform the reliability analysis of the circuit. For digital circuits, the transistor degradation model is used for timing analysis after aging. For analog circuits, the transistor degradation model is used for analyzing critical parameters (such as gain, bandwidth) after aging. However, transistor aging simulations are either too much work for the entire system, or the model accuracy is hard to guarantee due to the coupled aging effect at the design stage of the system. As channel geometries scale down, the physical mechanisms of these aging effects become more stochastic. Hence, a tendency is that the degradation model for the state-of-art technologies combines with the machine-learning models to make the model more general.

In view of this, the following problems still need to be solved urgently, which will be the focus of our future research:

1) Lack of accurate combined effect model of HCI and BTI under dynamic stress voltage;

2) It is difficult to use aging models to describe the degradation of multiple transistor parameters (I_{ds}, V_{th} and G_m) in the circuit at the same time;

3) Lack of reliability models that take the off-state degradation into account makes it difficult to accurately evaluate the circuit lifetime;

4) In order to provide a practical basis for the reliable design and optimization of the circuit, it is necessary to quickly locate the sensitive transistors in the circuit.

In addition, the challenge for the future is to establish reliability models with only a few parameters, analyzing the degradation of transistors on mixed digital and analog circuits, which can correctly describe the circuit's degradation under different operation voltage conditions as described above. At present, the simulation tools available also do not include important dynamic effects (such as recovery). Thus, there is still a lot to do to find a satisfactory solution to analyze the interdependency of these degradation effects, and perform accurate circuit reliability analysis.

REFERENCES

[1] S. Mishra et al., "A simulation study of NBTI impact on 14-nm node FinFET technology for logic applications: Device degradation to circuit-level interaction," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 271–278, Jan. 2019.

[2] L. Li, L. Xiao, H. Liu, and Z. Mao, "Synergistic effect of BTI and process variations on the soft error rate estimation in digital circuits," *IEEE Access*, vol. 10, pp. 64161–64171, 2022, doi: 10.1109/ACCESS.2022.3183137.

[3] B. Ullmann, "Impact of mixed negative bias temperature instability and hot carrier stress on MOSFET characteristics—Part I: Experimental," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 232–240, Jan. 2019.

[4] Z. Wu et al., "Investigation of the impact of hot-carrier-induced interface state generation on carrier mobility in nMOSFET," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3246–3253, Jul. 2021, doi: 10.1109/TED.2021.3080657.

[5] P. Duhan, V. R. Rao, and N. R. Mohapatra, "Effect of device dimensions, layout and pre-gate carbon implant on hot carrier induced degradation in HKMG nMOS transistors," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 3, pp. 555–561, Sep. 2020, doi: 10.1109/TDMR.2020.3007553.

[6] Z. Sun et al., "Investigation on the lateral trap distributions in nanoscale MOSFETs during hot carrier stress," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 490–493, Apr. 2019, doi: 10.1109/LED.2019.2897728.

[7] X. Guo and M. R. Stan, *Circuit Techniques for BTI and EM Accelerated and Active Recovery*. Cham, Switzerland: Springer, 2020, pp. 79–120, doi: 10.1007/978-3-030-20051-0_4.

[8] A. Kerber, T. Nigam, P. Paliwoda, and F. Guarin, "Reliability characterization of ring oscillator circuits for advanced CMOS technologies," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 2, pp. 230–241, Jun. 2020, doi: 10.1109/TDMR.2020.2981010.

[9] K.-U. Giering, "NBTI degradation and recovery in analog circuits: Accurate and efficient circuit-level modeling," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1662–1668, Apr. 2019, doi: 10.1109/TED.2019.2901907.

[10] C. Schluender, K. Puschkarsky, G. A. Rott, W. Gustin, and H. Reisinger, "NBTI: Experimental investigation, physical modelling, circuit aging simulations and verification," *Microelectron. Rel.*, vol. 82, pp. 1–10, Mar. 2018.

[11] M. Miura-Mattausch et al., "Compact modeling of dynamic trap density evolution for predicting circuit-performance aging," *Microelectron. Rel.*. vol. 80, pp. 164–175, Jan. 2018, doi: 10.1016/j.microrel.2017.12.003.

[12] R. Rodriguez et al., "Experimental monitoring of aging in CMOS RF linear power amplifiers: Correlation between device and circuit degradation," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2020, pp. 1–7, doi: 10.1109/IRPS45951.2020.9129301.

[13] G.-B. Lee and Y.-K. Choi, "Extraction of interface trap density through synchronized optical charge pumping in gate-all-around MOSFETs," *IEEE Electron Device Lett.*, vol. 41, no. 11, pp. 1629–1632, Nov. 2020, doi: 10.1109/LED.2020.3022025.

[14] G. Hiblot, "New charge pumping current model assuming exponential tails in the trap energy distribution," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1489–1492, Oct. 2018, doi: 10.1109/LED.2018.2863729.

[15] J. L. Wang et al., "Trap analysis based on low-frequency noise for SiC power MOSFETs under repetitive short-circuit stress," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 145–151, 2020, doi: 10.1109/JEDS.2020.2971245.

[16] C.-C. Lu, K.-S. Chang-Liao, F.-H. Tsai, C.-C. Li, and T.-K. Wang, "Detection of stress-induced interface trap generation on high-*k* gated nMOSFETs in real time by stress-and-sense charge pumping technique," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1405–1410, May 2015, doi: 10.1109/TED.2015.2409477.

[17] M. Cho et al., "Interface trap characterization of a 5.8-rm AA EOT p-MOSFET using high-frequency on-chip ring oscillator charge pumping technique," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3342–3349, Oct. 2011, doi: 10.1109/TED.2011.2162336.

[18] Y. Ding, C. Yan, Y. Qu, and Y. Zhao, "Re-examination of hot carrier degradation mechanism in ultra-scaled nFinFETs," *IEEE Electron Device Lett.*, vol. 43, no. 11, pp. 1802–1805, Nov. 2022, doi: 10.1109/LED.2022.3204429.

[19] N. Parihar, N. Goel, S. Mukhopadhyay, and S. Mahapatra, "BTI analysis tool—Modeling of NBTI DC, AC stress and recovery time kinetics, nitrogen impact, and EOL estimation," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 392–403, Feb. 2018, doi: 10.1109/TED.2017.2780083.

[20] A. Bravaix, V. Huard, F. Cacho, X. Federspiel, and D. Roy, *Hot-Carrier Degradation in Decananometer CMOS Nodes: From an Energy-Driven to a Unified Current Degradation Modeling by a Multiple-Carrier Degradation Process*. Cham, Switzerland: Springer, Oct. 2015, pp. 57–103, doi: 10.1007/978-3-319-08994-2_3.

[21] A. Gupta, C. Gupta, H. S. Jatana, and A. Dixit, "Investigation of hot-carrier degradation in 0.18 um MOSFETs for the evaluation of device lifetime and digital circuit performance," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 4, pp. 609–614, Dec. 2019.

[22] P. Sharma, "Hot-carrier degradation modeling of decananometer nMOSFETs using the drift-diffusion approach," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 160–163, Feb. 2017, doi: 10.1109/LED.2016.2645901.

[23] L. Atzeni and M. Rossetti, "Effect of reverse body bias on hot carrier induced degradation of n-MOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 1, pp. 80–85, Mar. 2018, doi: 10.1109/TDMR.2017.2789021.

[24] S. Mahapatra and N. Parihar, "Modeling of NBTI using BAT framework: DC-AC stress-recovery kinetics, material, and process dependence," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 1, pp. 4–23, Mar. 2020, doi: 10.1109/TDMR.2020.2967696.

[25] N. Haque, S. Dalai, B. Chatterjee, and S. Chakravorti, "Investigations on charge trapping and de-trapping properties of polymeric insulators through discharge current measurements," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 24, no. 1, pp. 583–591, Feb. 2017.

[26] A. Guo and J. A. del Alamo, "Unified mechanism for positive- and negative-bias temperature instability in GaN MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2142–2147, May 2017.

[27] P. Paliwoda, "Self-heating effects on hot carrier degradation and its impact on logic circuit reliability," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 2, pp. 249–254, Jun. 2019.

[28] S.-Y. Kim et al., "A comparative study on hot-carrier injection in 5-story vertically integrated inversion-mode and junctionless-mode gate-all-around MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 4–7, Jan. 2018, doi: 10.1109/LED.2017.2772871.

[29] Y. Xinhuan, S. Qianqian, Z. Jianyu, W. Chuanzheng, Y. Mingyan, and Z. Yuanfu, "A high-efffciency aging measurement with new data processing method for semiconductor device," *Microelectron. Rel.*, to be published.

[30] G. Torrente, "Investigation of degradation mechanisms and related performance concerns in 40nm NOR Flash memories," Ph.D. dissertation, Dept. Nano Electron. Nano Technol, Univ. Grenoble Alpes, Grenoble, France, 2018.

[31] F. A. Herrera, M. Miura-Mattausch, T. Iizuka, H. Kikuchihara, H. J. Mattausch, and H. Takatsuka, "Universal feature of trap-density increase in aged MOSFET and its compact modeling," in *Proc. Int. Conf. Simulat. Semicond. Processes Devices (SISPAD)*, 2020, pp. 109–112, doi: 10.23919/SISPAD49475.2020.9241674.

[32] S. Salamin, V. M. Van Santen, H. Amrouch, N. Parihar, S. Mahapatra, and J. Henkel, "Modeling the interdependences between voltage fluctuation and BTI aging," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 7, pp. 1652–1665, Jul. 2019, doi: 10.1109/TVLSI.2019.2899890.

[33] R. Kishida, T. Asuke, J. Furuta, and K. Kobayashi, "Extracting voltage dependence of BTI-induced degradation without temporal factors by using BTI-sensitive and BTI-insensitive ring oscillators," *IEEE Trans. Semicond. Manuf.*, vol. 33, no. 2, pp. 174–179, May 2020, doi: 10.1109/TSM.2020.2983060.

[34] H. Eslahi, S. A. Albahrani, D. Mahajan, and S. Khandelwal, "An analytical model for hot carrier induced long-term degradation in power amplifiers," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 39, no. 10, pp. 2000–2005, Oct. 2020, doi: 10.1109/TCAD.2019.2952554.

[35] W.-T. K. Chien, J. X. Luo, and M. Zhang, "The competing aging effects on SRAM operating life tests," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 2, pp. 416–425, Jun. 2019, doi: 10.1109/TDMR.2019.2916481.

[36] M. M. Mahmoud, N. Soin, and H. A. H. Fahmy, "Design framework to overcome aging degradation of the 16 nm VLSI technology circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 5, pp. 691–703, May 2014, doi: 10.1109/TCAD.2014.2299713.

[37] K. B. Sutaria, A. Mohanty, R. Wang, R. Huang, and Y. Cao, "Accelerated aging in analog and digital circuits with feedback," *IEEE Trans. Device Mater. Rel.*, vol. 15, no. 3, pp. 384–393, Sep. 2015, doi: 10.1109/TDMR.2015.2456893.

[38] J. B. Velamala et al., "Compact modeling of statistical BTI under trapping/detrapping," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3645–3654, Nov. 2013, doi: 10.1109/TED.2013.2281986.

[39] J.-A. Zhang et al., "An equivalent circuit model of HCI effect for short-channel N-MOSFET," in *Microelectron. Rel.*, vol. 136, Sep. 2022, Art. no. 114626, doi: 10.1016/j.microrel.2022.114626.

[40] V. B. Kleeberger, M. Barke, C. Werner, D. Schmitt-Landsiedel, and U. Schlichtmann, "A compact model for NBTI degradation and recovery under use-profile variations and its application to aging analysis of digital integrated circuits," *Microelectron. Rel.*, vol. 54, nos. 6–7, pp. 1083–1089, 2014.

[41] J. Fang and S. S. Sapatnekar, "The impact of BTI variations on timing in digital logic circuits," *IEEE Trans. Device Mater. Rel.*, vol. 13, no. 1, pp. 277–286, Mar. 2013, doi: 10.1109/TDMR.2013.2237910.

[42] A. Thirunavukkarasu et al., "Device to circuit framework for activity-dependent NBTI aging in digital circuits," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 316–323, Jan. 2019, doi: 10.1109/TED.2018.2882229.

[43] C.-C. Chen, S. Cha, T. Liu, and L. Milor, "System-level modeling of microprocessor reliability degradation due to BTI and HCI," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2014, pp. CA.8.1–CA.8.9, doi: 10.1109/IRPS.2014.6861125.

[44] B. Eghbalkhah, M. Kamal, H. Afzali-Kusha, A. Afzali-Kusha, M. B. Ghaznavi-Ghoushchi, and M. Pedram, "Workload and temperature dependent evaluation of BTI-induced lifetime degradation in digital circuits," in *Microelectron. Rel.*, vol. 55, no. 8, pp. 1152–1162, 2015.

[45] M. Xiao-Hua, C. Yan-Rong, H. Yue, and Z. Yue, "Hot carrier injection degradation under dynamic stress," *Chin. Phys. B*, vol. 20, no. 3, 2011, Art. no. 37305, doi: 10.1088/1674-1056/20/3/037305.

[46] A. Doukkali, I. Lahbib, P. Gamand, P. Martin, D. Lesenechal, and P. Descamps, "Reliability analysis of low noise amplifiers for wireless applications under high RF power stressing," in *Proc. Int. Conf. Adv. Technol. Commun. (ATC)*, 2017, pp. 132–135, doi: 10.1109/ATC.2017.8167602.

[47] D. P. Ioannou et al., "Hot carrier effects on the RF performance degradation of nanoscale LNA SOI nFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2018, pp. P-TX.2-1–P-TX.2-3, doi: 10.1109/IRPS.2018.8353697.

[48] G. I. Wirth, R. Da Silva, and B. Kaczer, "Statistical model for MOSFET bias temperature instability component due to charge trapping," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2743–2751, Aug. 2011, doi: 10.1109/TED.2011.2157828.

[49] X. Zhong, H. Jiang, L. Tang, X. Qi, P. Jiang, and L. Ran, "Gate stress polarity dependence of AC bias temperature instability in silicon carbide MOSFETs," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3328–3333, Jun. 2022, doi: 10.1109/TED.2022.3164641.

[50] H. Kuekner et al., "Impact of duty factor, stress stimuli, gate and drive strength on gate delay degradation with an atomistic trap-based BTI model," *Microprocess. Microsyst.*, vol. 37, no. 8, pp. 792–800, 2013, doi: 10.1016/j.micpro.2013.04.009.

[51] E. Acurio, F. Crupi, P. Magnone, L. Trojman, G. Meneghesso, and F. Iucolano, "On recoverable behavior of PBTI in AlGaN/GaN MOS-HEMT," *Solid-State Electron.*, vol. 132, pp. 49–56, Jun. 2017, doi: 10.1016/j.sse.2017.03.007.

[52] J. Kang, Q. Liu, H. Luo, H. Cao, Z.-H. Zhang, and Z. Xin, "Investigation of off-state stress induced degradation of SiC MOSFETs under short-circuit condition," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 5224–5234, May 2023, doi: 10.1109/TIE.2022.3189071.

[53] S.-G. Jung, S.-H. Lee, C.-K. Kim, M.-S. Yoo, and H.-Y. Yu, "Analysis of drain linear current turn-around effect in off-state stress mode in pMOSFET," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 804–807, Jun. 2020, doi: 10.1109/LED.2020.2989324.

[54] J. O. Gonzalez, M. Hedayati, S. Jahdi, B. H. Stark, and O. Alatise, "Dynamic characterization of SiC and GaN devices with BTI stresses," *Microelectron. Rel.*, vols. 100–101, Sep. 2019, Art. no. 113389, doi: 10.1016/j.microrel.2019.06.081.

[55] Z. Wu, S. Liang, G. Deng, and J. Wang, "Investigation on SiC MOSFETs with long time nitridation treatment under dynamic high temperature gate stress," in *Proc. IEEE Int. Power Electron. and Appl. Conf. Expo. (PEAC)*, 2022, pp. 1154–1158.

[56] Y. Zhao et al., "A unified physical BTI compact model in variability-aware DTCO Flow: Device characterization and circuit evaluation on reliability of scaling technology nodes," in *Proc. Symp. VLSI Technol.*, 2021, pp. 1–2.

[57] H. M. Abbas, B. Halak, and M. Zwolinski, "Learning-based BTI stress estimation and mitigation in multi-core processor systems," *Microprocess. Microsyst.*, vol. 81, no. 11, Mar. 2021, Art. no. 103713, doi: 10.1016/j.micpro.2020.103713.

[58] Y. Su et al., "Dynamic time evolutionary aging analysis for device-circuit lifetime estimation of thin-film transistors," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1439–1442, Sep. 2019, doi: 10.1109/LED.2019.2927519.

[59] Z. Zhang et al., "Aging-aware gate-level modeling for circuit reliability analysis," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4201–4207, Sep. 2021, doi: 10.1109/TED.2021.3096171.

[60] J. Ding, D. Reid, P. Asenov, C. Millar, and A. Asenov, "Influence of transistors with BTI-induced aging on SRAM write performance," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3133–3138, Oct. 2015, doi: 10.1109/TED.2015.2462319.

[61] B. R. Wier, K. Green, J. Kim, D. T. Zweidinger, and J. D. Cressler, "A Physics-based circuit aging model for mixed-mode degradation in SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 2987–2993, Aug. 2016, doi: 10.1109/TED.2016.2573263.

[62] L. Li, L. Xiao, J. Li, H. Liu, and Z. Mao, "Synergistic effect of BTI and process variations on impact and monitoring of combination circuit," in *Proc. IEEE 13th Int. Conf. ASIC (ASICON)*, Chongqing, China, 2019, pp. 1–4, doi: 10.1109/ASICON47005.2019.8983690.

[63] A. Crespo-Yepes et al., "CMOS inverter performance degradation and its correlation with BTI, HCI and OFF state MOSFETs aging," *Solid-State Electron.*, vol. 191, May 2022, Art. no. 108264, doi: 10.1016/j.sse.2022.108264.