Design for EMI/ESD Immunity for Flexible and Wearable Electronics

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ABSTRACT Proliferation of flexible, wearable and portable electronics come with new challenges of system reliability. Particularly, flexible and wearable electronics cause more frequent and are more susceptible to electromagnetic interference (EMI) effects and electrostatic discharge (ESD) failures, and have unique requirements for design-for-reliability (DfR) associated with EMI and ESD immunity to achieve electromagnetic compatibility (EMC) compliance. This paper outlines the key challenges in design for EMI and ESD immunity for wearable microsystems and discusses potential design for EMI/ESD immunity solutions.

INDEX TERMS EMI, ESD, EMC, flexible, wearable, design-for-reliability, immunity, WDUT.

I. INTRODUCTION

Advances in microelectronics technologies, from aggressive CMOS scaling to thin-film transistor (TFT) to flexible integrated circuit (IC) to low-power IC to heterogeneous integration (HI), make it possible to design and fabricate non-traditional ICs and microsystems, which inspires countless new applications, among which flexible, portable and wearable electronics are now widely available in the market [1], [2], [3]. Obviously, performance and reliability are the two cornerstones for any microelectronics products. Continuous advances and proliferation of flexible and wearable electronics pose a new reliability challenge in IC designs, which is design-for-reliability associated with EMI immunity and ESD robustness for microelectronics chips and system products, such as large-area displays, foldable displays, medical implantable devices, portable electronics (e.g., smartphones, tablets), wearable gadgets (e.g., smartwatches, sports devices, wellbeing monitors, AR/VR goggles), smart manufacturing (e.g., robots, sensors), edge computing, and all kinds of Internet of Everything (IoET) devices [4], [5], [6], [7], [8], [9]. Such unique families of flexible, portable and wearable electronics necessitate research innovations to ensure reliability and unlock the ultimate potentials of flexible technologies, particularly for the trending chiplet-based heterogeneous integration technologies, which makes DfR for EMI/ESD immunity extremely challenging while enabling more applications. In general, EMC compliance must be considered in developing microelectronics system products, which requires thorough understanding of the system capability of functioning satisfactorily in an electromagnetic environment for which EMI and ESD are the two key concerns. Accurate EMI and ESD characterization, including test techniques, tools, procedures and standards, at device, circuit and system levels, plays a critical role in developing robust EMI/ESD design-for-reliability solutions, which is an emerging challenge for flexible and wearable electronics. This paper outlines key challenges in EMI/ESD immunity characterization and DfR development for flexible, portable and wearable electronics. Potential EMI/ESD DfR solutions are discussed.

II. EMERGING EMI/ESD IMMUNITY CHALLENGES
A. DESIGN FOR EMI IMMUNITY CONSIDERATIONS

EMI effects refer to system performance degradation, malfunction or failure due to electromagnetic disturbances (a.k.a. noises or interferers). In electronics applications, EMC describes system's ability to operate acceptably in presence of various EMI effects where unwanted electromagnetic field are concerned for its EM signal/energy/field generation, propagation (transmission or coupling) and reception by a system. EMC compliance requires an electronic product operates properly without interfering with other systems

in a shared EM environment. Therefore, EMC compliance must consider EM energy emission as a source, susceptibility/immunity to unwanted EMI signal/energy, and transmission/coupling of unwanted EM field. While EMC has been studied extensively for general electronics, EMI for new flexible and wearable devices is an emerging reliability topic that calls for research to address the following unique challenges. First, success of flexible and wearable technologies resulted in proliferation of sea volume of such devices, which creates more EM pollutions and stronger EMI effects that may critically affect other systems in the common electromagnetic environment, representing a big challenge in product designs and EMI controls. Second, due to the moving nature of portable and wearable electronics, EM pollution becomes ubiquitous that can occur anywhere anytime, unpredictably, hence making EMI immunity for wearable devices extreme challenging. Third, wearables are typically more sensitive to alien EMI disturbances due to sizes, circuits and scaled technologies. Fourth, the transient nature of ad hoc EMI effects adds more risks and uncertainties to wearables, possibly nullifying otherwise effective standard EMI controls established for freestanding systems. For example, a person with an implanted medical device passing by a stranger in street using a smartphone may suffer from sudden malfunction of the embedded device. Similarly, in a hospital, one patient wearing a medical-assisting device approaching to another in-bed patient tied up to a medical monitor may accidently shutdown it. In both cases, the EMI effects can be deadly. Fifth, new testing methods and standards are needed to accurately evaluate EMI emission, transmission and immunity associated with wearable devices, including identifying the EMI generation mechanisms and sources, measuring the EM disturbances, evaluating EMI signal propagation and coupling channels, and characterizing system degradation due to EMI. Last but more importantly, design for EMI immunity, particularly at chip level, shall play a vital role in developing any EMI-robust flexible and wearable microelectronics systems both to ensure EMC compliance (e.g., minimizing EMI emission as a source) and to fend off any incident EM interferers (i.e., as an EMI victim). Recently, significant efforts have been drawn to research on EMI reliability issues of flexible and wearable electronics. For example, [5] reports a new EMI test method for wearable bio-sensors to accurately measure unwanted common-mode voltage induced by an ESD spark. Reference [6] describes a combined EM field simulation and circuit analysis technique for characterizing unwanted differential signal between two electrodes induced by an interfering EM field when operating a wearable electro-cardiogram (ECG) monitor, hence, suggesting a way to minimize EMI effect by carefully balancing the impedances of the two sensing electrodes in design. Overall, EMI immunity for flexible and wearable electronics is a new challenge requiring research innovation in all related aspects, including EMI characterization techniques, EMI test standards and hardening systems against EMI by design. It is noted that design for EMI immunity at IC level

is vitally critical to ensuring EMI reliability of wearable electronics. Among all factors, EMI shielding plays a key role in DfR for EMI immunity where the two important tasks in IC designs are: 1) minimizing undesired EM generation (as a noise source) and emission (propagation and coupling via a medium), and 2) rejecting incident EMI noises (as a victim). Such root-level design for EMI immunity philosophy requires major research efforts in IC designs for flexible and wearable electronics. Inspiring design example will be discussed later.

B. DESIGN FOR ESD IMMUNITY CONSIDERATIONS

In general, an ESD event occurs when two subjects of different electrical potentials are brought together (in direct contact or in close proximity), ESD discharging is then triggered, causing static charges transferring in between, and the resulting transient voltage and current pulses can degrade or damage electronics [10]. EMC concerns about ESD phenomena in two aspects: the transient electrostatic field and the EM transient (EMI effect) induced by an ESD spark, both can lead to system degradation, malfunction or damage. Design for ESD immunity is typically achieved through on-chip ESD protection in IC designs. In principle, on-chip ESD protection relies on an ESD protection device connected at an IC pad, which will be swiftly turned on by an incident ESD pulse to form a low-R discharging path to shunt the large ESD current without overheating and to clamp the pad voltage to avoid voltage breakdown [10], [11]. It is important to understand the key difference between human body model (HBM) and charged device model (CDM) ESD events [12], [13]. Briefly, HBM is an external-oriented ESD event, where static charges stored inside a human body will be discharged into an IC when finger-touching the chip, hence being a from-External-to-Internal phenomenon (E⇒I). HBM ESD protection utilizes the classic pad-based ESD protection method where the ESD device at the pad serves as a "guard" to block external charges from entering into a core IC die, hence, providing on-chip ESD protection [10]. On the other hand, CDM ESD is an internal-oriented event where static charges induced inside an IC will be discharged into the electrical ground (GND) through a grounding pad, hence being a from-Internal-to-External phenomenon (I⇒E) [14]. Intuitively, when using the classic pad-based ESD protection approach for CDM ESD protection, the charges stored inside an IC die must route through unknown internal paths to reach to the GND for CDM ESD discharging [15]. Furthermore, compared with ESD phenomena associated freestanding systems, flexibles and wearables have many unique ESD features that are being extensively studied, making ESD protection design and characterization a very challenging new research task for wearable electronics. First, the close proximity makes human-device ESD effects much stronger for wearables. Second, proliferation of flexible and wearable technologies makes ESD a wide-spreading reliability concerns for wearables. Third, existing effective ESD controls become
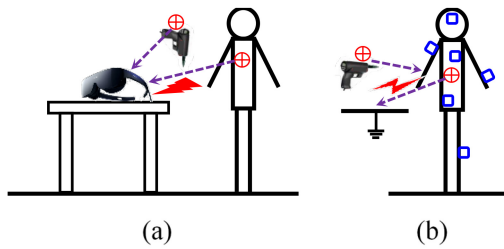
FIGURE 1. ESD phenomena for (a) freestanding systems per IEC/HMM and (b) wearable electronics are very different in ESD mechanisms.
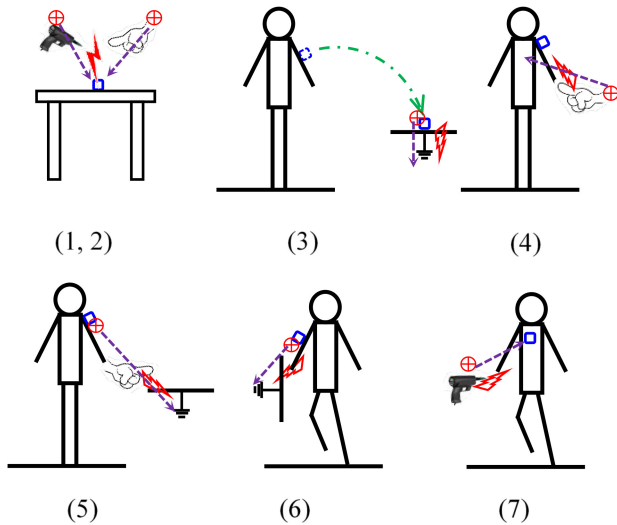

FIGURE 2. Different ESD scenarios for wearable electronics in applications.

impractical at the user end for portable and wearable devices. Fourth, since portable and wearable electronics move constantly, ESD events become ubiquitous and random (i.e., ad hoc in nature) that can occur anywhere anytime, making ESD immunity an urgent need for wearable devices. Fifth, wearables are more sensitive to ESD transient energy due to smaller sizes and scaled technologies used. Sixth, compared to freestanding systems, ESD phenomena for flexible and wearable electronics are far more complicated at application end, leading to high complexity in ESD protection designs and testing, which must be thoroughly investigated through research. In general, ESD phenomena can be rather different for freestanding systems and wearable electronics as depicted in Fig. 1, because the ESD events for wearables are very sensitive to where the device is mounted on a human body. Hence, ESD for wearables may be categorized into eight application scenarios as depicted in Fig. 2 and summarized in Table 1. In Scenario-1, a wearable device-under-test (WDUT) sitting on a table (i.e., WDUT-on-table) is picked up (touched directly) by a hand where static charges stored in a charged human body will be discharged into the WDUT, affecting its functions. This is an E⇒I charging stress to WDUT, which may likely cause ESD failure.

Scenario-1 ESD event may be characterized by the standard system level IEC61000-4-2 ESD testing method [16]. Scenario-2 describes a special Scenario-1 (General) case where a charged hand would touch directly a port of WDUT (i.e., linked to a pin/pad of the IC inside; a.k.a., via-Port). Clearly, Scenario-2 is a more severe ESD stressing case over Scenario-1 that is a general ESD stressing situation. Scenario-2 may be evaluated using the human-metal model (HMM) ESD testing standard, which is essentially the worst case of IEC61000-4-2 modeling when a charged human body holding a tool (e.g., an ESD zapping gun) to directly contact a port of WDUT, hence posing very high ESD risk to the WDUT (i.e., directly stressing the internal IC pads). In Scenario-3, a WDUT worn by a human body (i.e., WDUT-on-body) is taken off and then placed on GND (i.e., grounding), the charges stored inside the WDUT-on-body will discharge into GND, causing CDM-type ESD discharging and possible CDM ESD malfunction/failure. Scenario-3 is an I⇒E discharging stress to WDUT, which may be evaluated by the CDM ESD test standard [13]. However, caution must be given to the difference between system-level WDUT ESD events and component-level CDM ESD events, e.g., the typical CDM ESD energy storage capacitance of 6.8pF for a component is mostly too small for WDUT that is a wearable system device. It is also intuitive that IEC61000-4-2 and HMM test standards will not apply to Scenario-3. Scenario-4 describes a case where a wearable device mounted on a body (i.e., WDUT-on-body) is touched by a charged foreign hand/finger through the body finger (i.e., self-finger), ESD discharge from the charged foreign body will occur to zap the WDUT, causing ESD failure. This is an E⇒I charging stress to WDUT, which could be evaluated by IEC61000-4-2; however, the body effect will cause ESD complexity because the WDUT may be mounted to different positions of a body that cannot be accurately tested by IEC61000-4-2 model by either contact or air discharge approach. Scenario-5 describes a case where a wearable device mounted on a body (i.e., WDUT-on-body) is touched by a foreign GND object through a self-finger, the charges stored in the WDUT-on-body will discharge into GND through the self-finger. Scenario-5 is an I⇒E discharging stress to WDUT-on-body, which could be evaluated by the CDM ESD model; however, the body effect should also be included to address any deviation from the component-level CDM ESD testing procedure. The body effect (mounting locations) may effectively mitigate the ESD stressing intensity in Scenarios 4 and 5 compared to a case of directly touching WDUT. Scenarios-6 & 7 describe rather different ESD events unique to wearables, i.e., passing-by cases. In Scenario-6, when a human body wearing a WDUT-on-body passes by a GND object (e.g., a metal door knob), either in direct contact or in close proximity (i.e., air discharge), the charges stored inside the WDUT will discharge into the GND. This is an I⇒E discharging stress to WDUT, which will cause ESD malfunction/failure and could be evaluated by the CDM ESD test standard with the body effect being considered. Scenario-7 describes a passing-by

TABLE 1. Summary for various ESD event scenarios for wearable electronics systems.

No.	ESD Event Scenarios	Stress Type	ESD Nature	Test Model	Risk
1	WDUT-on-table touched/picked-up by a hand (General; Direct)	Charging	E⇒I	IEC61000-4-2	H
2	WDUT-on-table touched/picked-up by a hand (via Port, Direct)	Charging	E⇒I	HMM	VH
3	WDUT-on-body being taken-off and placed on GND (General, Direct)	Discharging	I⇒E	CDM (>6.8pF)	H/M
4	WDUT-on-body being touched by a charged foreign finger via self-finger (General; Indirect; via-Port not option)	Charging	E⇒I	~IEC61000-4-2 (body effect)	M/L
5	WDUT-on-body being touched by a foreign GND tip via self-finger (General; Indirect; via-Port not option)	Discharging	I⇒E	~CDM (body effect)	M/L
6	WDUT-on-body directly approaches GND (Direct; Random/Moving, Sensitive to body position; low chance via-port)	Discharging	I⇒E	~CDM (body effect)	VH
7	WDUT-on-body directly approaches a charged object (Direct; Random/Moving, Sensitive to body position; low chance via-port)	Charging	E⇒I	~IEC (body effect)	VH
8	WDUT-on-body being touched by a self-finger (General)	No	e-Equilibrium	N/A	N/A

WDUT: Wearable device (system) under test, broadly including equipment under test (EUT) in this paper
GND: Electrical ground
General: General ways to contact/approach WDUT
via-Port: A worst case way to contact/approach WDUT thorough a port that is connected to an internal IC pad/pin
Direct: Direct charging/discharging methods to WDUT
Indirect: Indirect charging/discharging methods to WDUT, through a human body
E⇒I: from-External-to-Internal; I⇒E: from-Internal-to-External
ESD stress intensity: Very high (VH), High (H), Medium (M), Low (L)
Body effect: Wearable device charging/discharging is sensitive to device position on body due to impedance
Typical component level CDM energy storage capacitance ~6.8pF (small) per CDM test standard

case similar to Scenario-6, however, the WDUT-on-body approaches a charged object. Hence, this is an E⇒I charging stress to WDUT-on-body, which may result in ESD failure to the WDUT and could be evaluated by IEC61000-4-2, again, with the body effect being included. Both Scenarios 6 and 7 are Direct ESD discharging/charging events, which are considered the worst cases among all WDUT ESD phenomena in terms of ESD risks. Furthermore, the passing-by nature of Scenarios-6 & 7 suggest higher complexity in the ESD phenomena because the WDUT-on-body is moving and the brush-by ESD interactions with the foreign GND or charging object are random, and the ESD charging/discharging effects are also very sensitive to the mounting position of the WDUT on a body due to the body effect (impedance related to the body geometry at the mounting point, e.g., hand, wrist, arm, waist, chest and head, and its distance to the touching point). Hence, substantial modification is expected when using IEC61000-4-2 and CDM ESD test standards in such scenarios. Lastly, Scenario-8 concerns a human body wearing a WDUT and a self-finger touches the WDUT-on-body (e.g., operating the device). In such a case, the first-order approximation is that the human body is roughly in electrical equilibrium, hence, no significant ESD charging/discharging is concerned with the WDUT-on-body. In summary, it is clear that ESD phenomena for wearable electronics is much more complicated ESD category compared to that for its freestanding counterparts, hence requires more research to understand the details and to develop more suitable and reliable ESD test procedures and standards for accurate ESD characterization and robust ESD protection designs. Potential ESD protection examples for wearable electronics are given below for inspiring thinking.

III. DESIGN FOR EMI IMMUNITY EXAMPLE

The boom in flexible and wearable electronics has led to substantial research to investigate related EMI reliability problems, from testing methods [5], [6] to EMI designs, particularly on design for EMI immunity of wearables [17], [18]. For example, [17] reports circuit routing technique in designing flexible printed circuit board for LCD panels where current return paths and decoupling capacitors were optimized to suppress EMI effects. Reference [18]
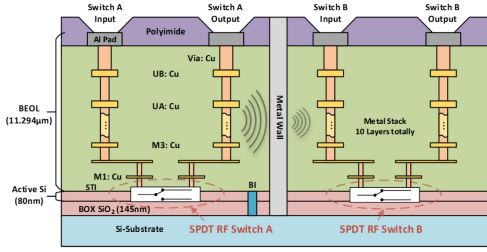
FIGURE 3. X-section of in-BEOL metal wall isolation structure uses to isolate global flying crosstalk between SPDT circuits in a SOI CMOS technology.

FIGURE 4. Measurement comparison for SPDT circuit splits, with and without metal cage isolation, and with unfilled air trench and using standard buried isolation (BI ring), shows that the new in-BEOL metal wall structure is very efficient in EMI suppression.

describes the benefits of using flexible thin films made of graphene multi-walled carbon nanotube (MWCNT) as RF shield layers for enhanced EMI shielding efficiency, which can be applied to various flexible and wearable electronics. Obviously, system-level design for EMI immunity may benefit the most from solving the EMI problem at its root, i.e., at device and IC levels, where EM shielding plays a critical role. In IC designs, global noise coupling remains a major EMI problem. Techniques to prevent in-substrate RF noise coupling, resistive and/or capacitive, in analog and mixed-signal (AMX) and RF ICs have been well developed, including using guard rings, high-R substrate, cavity, etc. On the other hand, it was found that global flying noises, i.e., RF interferences (a.k.a., noises or crosstalk) through the complex metal interconnects in the back end of line (BEOL) on a chip, becomes the dominant noise coupling cause that must be effectively suppressed [19]. We devised a novel in-BEOL metal wall flying noise isolation structure in CMOS as a potential EMI immunity solution, depicted in Fig. 3, where a fine-pitched deep trench is created around the concerned circuit, which is filled with synthesized nano metal powders to form a metal cage that serves as an EMI shield [20]. The novel design concept was validated experimentally. In the prototype design, SPDT RF antenna switches for smartphones (1710-2155 MHz) were designed in a foundry 45nm SOI technology, shielded by the metal wall isolation structures where the deep trench was etched by FIB and filled with silver nano powder (99.99%, 80~100nm in sizes) to form an EMI enclosure. Testing shows that the flying crosstalk from Switch A to Switch B was successfully reduced by ~18.5 dB (~98.6% in linear scale), confirming that the in-BEOL metal cage structure can be an efficient EMI shielding solution at chip level, as shown in Fig. 4. We believe that the in-BEOL and nano power filling features are suitable for EMI shielding in flexible ICs, hence a potential solution for design for EMI immunity for wearable electronics.

IV. DESIGN FOR ESD PROTECTION EXAMPLE

Two ESD design examples are discussed below addressing the unique challenges of design for ESD immunity for flexible and wearable electronics.
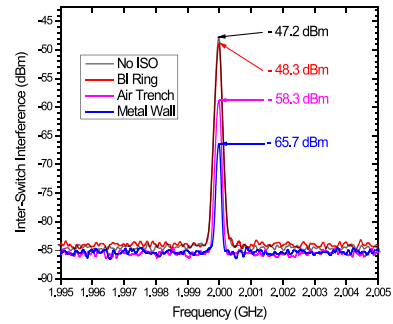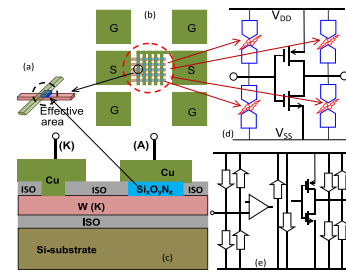

FIGURE 5. Above-IC nano crossbar array ESD protection structure: (a) Single-node device, (b) 5 × 5 array, (c) X-section, (d) new on-chip ESD circuit scheme, and (e) traditional ESD protection using PN-based ESD devices.

A. NANO CROSSBAR ARRAY ESD PROTECTION

Traditional ESD protection relies on in-Si PN-based active devices for ESD discharging, which however suffers from significant ESD design overhead (e.g., ESD induced parasitic capacitance, noise and leakage, as well as chip area consumed by large number of ESD devices and ESD layout difficulty). To overcome this fundamental ESD protection challenge, we devised a novel above-IC phase-changing-based nano crossbar array ESD protection mechanism and device structure [21], [22], [23]. Depicted in Fig. 5, the nano crossbar array ESD structure consists of an array of nano crossbar nodes with each node being a two-terminal (2T) device comprising two electrodes (anode, A and cathode, K) separated by a phase-changing insulator layer. The nano crossbar ESD array structures are made in CMOS BEOL, hence, being above-IC. The ESD node device remains Off during normal IC operations. When an incident ESD pulse appears at a pad, the ESD device will be triggered into ON state, through phase changing in the insulator, to form a low-R ESD discharging path for ESD protection. After the ESD pulse is over, the ESD device will return to OFF state. The prototype nano crossbar ESD array structures were fabricated in a CMOS-compatible process. Fig. 6 depicts the measured ESD discharging I-V curve by transmission-line pulse (TLP) ESD testing, which readily shows a desired dual-directional ESD discharging behavior [23]. The phase changing mechanism ensures ultrafast ESD triggering speed,
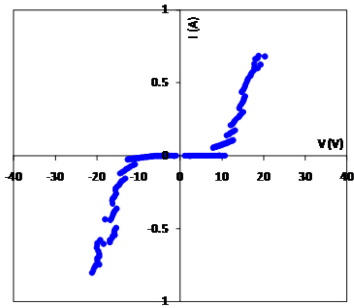
FIGURE 6. ESD discharging I-V characteristics for a 5X5 array nano crossbar ESD protection structure (5μm × 5μm node) by TLP measurement.
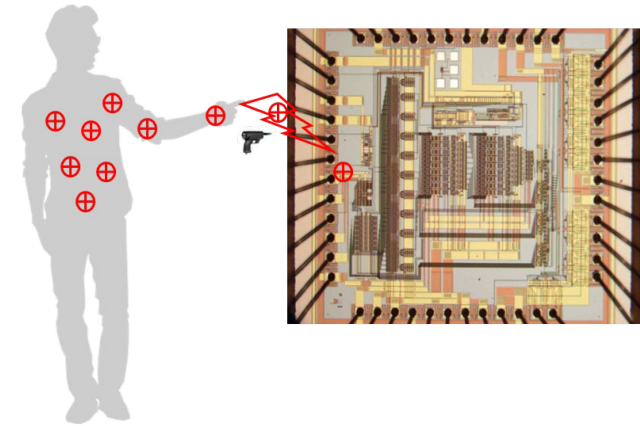

FIGURE 7. Illustration of external-oriented from-External-to-Internal ESD discharging phenomena associated with HBM, IEC and HMM ESD test standards.

FIGURE 8. Illustration of internal-oriented from-Internal-to-External ESD discharging phenomena associated with CDM ESD test standard.

FIGURE 9. Illustration of the classic pad-based ESD protection scheme for E⇒I ESD stressing cases. ⬆ represents an ESD protection device.

FIGURE 10. Using pad-based CDM ESD protection approach cannot avoid random internal CDM ESD failures induced by internal ESD discharge current routing. (✳ indicates possible internal CDM ESD failure points)

down to 100ps. Due to its above-IC device structure without any in-Si PN junctions, the new nano crossbar ESD array has negligible leakage (<2pA) and consumes no extra Si area. Very high ESD protection capability was achieved for a 5x5 prototype device (∼8.11A), which, in combination of its dual-directional ESD discharging feature, translates into dramatic reduction in chip area needed for an ESD protection network. All these unique features are highly desirable for advanced on-chip ESD protection to achieve robust ESD protection with minimized ESD design overhead. The unique above-IC nano crossbar ESD array structure seems to be suitable for design for ESD immunity for wearable and flexible electronics systems.

B. INTERNAL-DISTRIBUTED CDM ESD PROTECTION

As discussed earlier, HBM, IEC and HMM ESD phenomena are external-oriented E⇒I ESD discharge events, which can be effectively handled by the classic pad-based ESD protection approach, as depicted in Fig. 7. On the other hand, a CDM ESD event is internal-oriented I⇒E discharge stressing phenomenon, depicted in Fig. 8, which could not be effectively protected by the traditional bad-based ESD protection method. Fig. 9 depicts the classic pad-based ESD protection scheme widely applied to HBM, IEC and HMM ESD
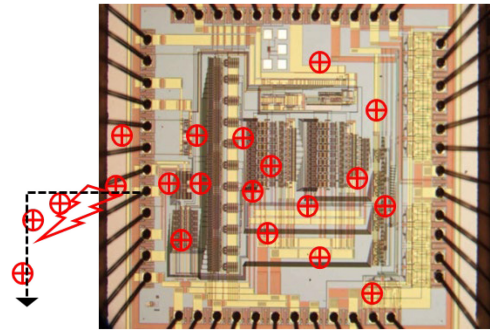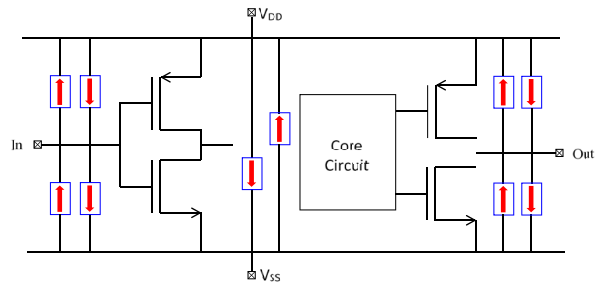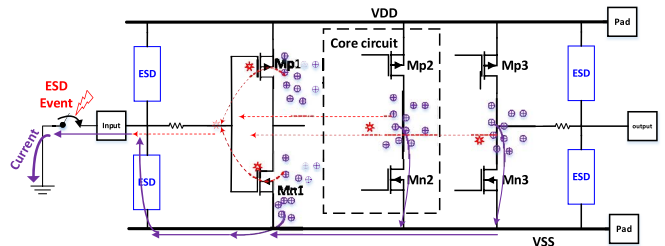
events [10]. Fig. 10 shows that if traditional pad-based ESD protection is used for CDM ESD event, unexpected internal CDM ESD failure may occur randomly when the charges stored arbitrarily inside a chip route internally *en route* to discharge at a GND pad [14]. Therefore, a novel concept of non-pad-based internal-distributed CDM ESD protection method was proposed to thoroughly protect ICs against CDM ESD stresses, as depicted in Fig. 11, where a set of ESD devices of smaller sizes are purposely placed at selected internal circuit nodes, per a smart partitioning technique [15]. The concept works in that, as the internal charges start to accumulate locally to a pre-set potential level, the local ESD device will be turned on to swiftly discharge the charges through a local GND *in situ*, without routing to an external GND pad, hence avoiding random internal routing of charges that could lead to unpredictable internal CDM ESD failures,
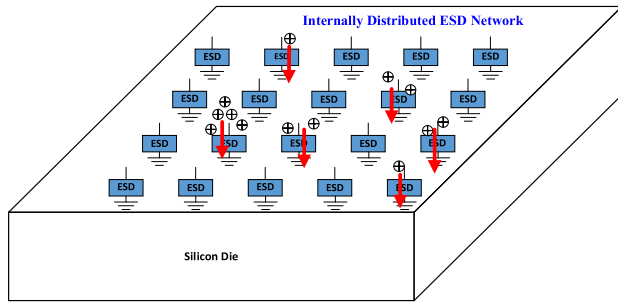
FIGURE 11. Illustration of the new internal-distributed CDM ESD protection method using a non-pad-based internal ESD device mesh on a chip.
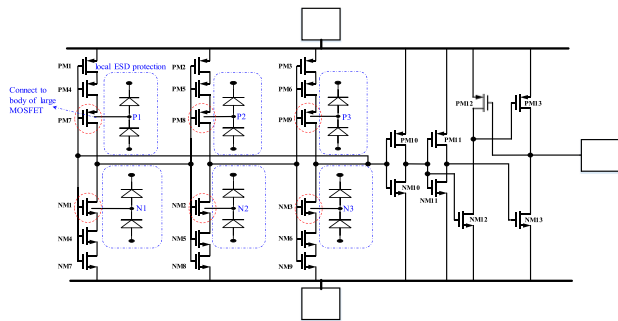

FIGURE 12. The new non-pad-based internal-distributed CDM ESD protection concept was validated using a 3-stage oscillator IC implemented in a foundry 45nm SOI CMOS where a set of diode ESD devices were placed at critical internal circuit nodes for local ESD discharging internally.

which is a major ESD reliability problem for advanced ICs. Understanding this CDM ESD protection problem is critical to wearable electronics, because, as discussed before, ESD phenomena for flexible and wearable devices are very complex, i.e., the same wearable device may suffer from HBM, IEC, HMM or CDM ESD stressing cases randomly during field application, all depending upon its application scenarios and where/how it is mounted on a human body. The situation is further complicated by the fact that no single existing ESD test standard was developed to cover the complexity of wearable ESD phenomena as discussed earlier. Nevertheless, the new internal-distributed CDM ESD protection method must be further studied as a potential CDM ESD protection solution for wearable electronics. The new non-pad-based internal-distributed CDM ESD protection concept has been validated by simulation and experimentally in an IC designed and fabricated in a 45nm SOI process, shown in Fig. 12 [15]. We believe that further research on internally distributed CDM ESD protection is important to design for ESD immunity for wearable electronics.

V. CONCLUSION

Advances in IC technologies led to proliferation of flexible, portable and wearable electronics, leading to emerging challenges of design for EMI/ESD immunity for such devices.

Due to the unique natures of flexible and wearable electronics, the EMI and ESD reliability problems are more ubiquitous, significant and complicated for wearable electronics, which calls for urgent research efforts to thoroughly understand all details including EMI/ESD fundamentals, characterization techniques, testing standards, and design for EMI/ESD immunity solutions, which are summarized in this paper. It is important to note that, typically, the EMI/ESD phenomena for freestanding systems are generally stable and EMI/ESD control measures can be efficient for EMI/ESD immunity solutions; however, EMI/ESD DfR for wearable/flexible electronics is much more complicated and involving because EMI/ESD phenomena are more ubiquitous and random that occur anywhere and anytime, the devices are more troublesome as EMI sources and more vulnerable as EMI/ESD victims, and "standing" EMI/ESD controls are not suitable for small and moving electronics. Therefore, DfR for EMI/ESD immunity for wearable/flexible electronics is an emerging area of R&D efforts. Several novel EMI and ESD reliability design examples are discussed aiming to inspire innovations to address the emerging reliability challenges of EMI and ESD immunity for flexible, portable and wearable electronics.

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