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Fast and Expandable ANN-Based Compact Model and Parameter Extraction for Emerging Transistors

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ABSTRACT In this paper, we present a fast and expandable artificial neural network (ANN)-based compact model and parameter extraction flow to replace the existing complicated compact model implementation and model parameter extraction (MPE) method. In addition to nanosheet FETs (NSFETs), our published ANN-based compact modeling framework is easily extended to negative capacitance NSFETs (NC-NSFETs), which are attracting attention as next-generation devices. Each device is designed using a technology computer-aided design (TCAD) simulator. Using device structure parameters, temperature, and channel doping depth as input variables, we construct a dataset of electrical properties used for machine learning (ML)-based modeling. The accuracy of predicting device electrical characteristics with the proposed ANN-based compact model is less than a 1% error compared to TCAD, and simulation results of digital and analog circuits using the proposed compact model show less than a 3% error. This allows the ANN-based modeling framework to achieve accurate DC, AC, and transient simulations without restrictions on device technology. In particular, temperature and process variables such as channel doping depth, which are not defined in the compact model parameters, are easily added to the previously presented five key parameters. Instead of conventional complex compact modeling and MPE work, we propose a method to create fast, accurate, flexible, and expandable ML-based Verilog-A SPICE models with design technology co-optimization (DTCO) capabilities.

INDEX TERMS Artificial neural network (ANN), machine learning (ML), compact model, model parameter extraction (MPE), nanosheet FET (NSFET), negative capacitance NSFET (NC-NSFET), SPICE.

I. INTRODUCTION

According to Moore's Law, integrated circuits have advanced rapidly over the past decades, and the structures and materials of transistors have also been changed to improve their power, performance, area (PPA) [1], [2]. With the development of such device technology, structural improvements have been made to nanosheet FETs (NSFETs) in order to improve gate controllability and increase current compared to the same area of the existing structure, such as a FinFET. According to the International Roadmap for Devices and Systems (IRDS) 2021, the negative capacitance NSFET (NC-NSFET) structure is expected to be adopted for ultra-low power applications at the 1.5 nm node around 2028 and beyond [2]. In order to analyze the performance of integrated circuits for which device design, high accuracy compact modeling as well as accurate model parameter extraction (MPE) are essential. Since it is very difficult to physically describe the characteristics of newly developed nanodevices, the typical compact model is very complex and takes years to develop. The traditional MPE flow is based on a physical

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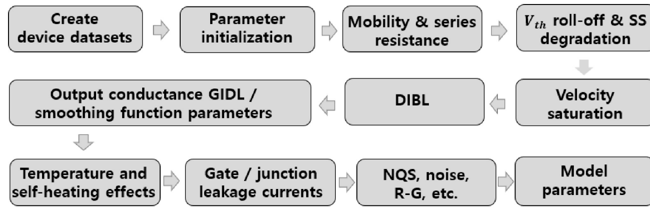

FIGURE 1. A conventional model parameter extraction flow [3], [4].

formula as $C-V$ (*Low* V_{ds}) $\rightarrow$ g_m, $I_{ds}-V_{gs}$ (*Low* V_{ds}) $\rightarrow$ g_m, $I_{ds}-V_{gs}$ (*High* V_{ds}) $\rightarrow$ g_{ds}, $I_{ds}-V_{ds}$ $\rightarrow$ $C-V$ (*High* V_{ds}) in the order, as shown in Fig. 1. It has a complex extraction process of 17-34 steps [3], [4]. Implementing the developed compact model in the MPE program is very difficult and time-consuming. In addition, it takes at least several weeks to extract accurate SPICE model parameters [5], [6]. This time-consuming MPE is another problem with the current design technology co-optimization (DTCO) flow. To solve these problems, studies on MPE using machine learning (ML) have been reported [6], [7], [8], [9], [10]. These studies suggest methods to estimate the dominant parameters, such as U_0 and V_{sat} at each step in the MPE process, which usually consists of dozens of steps. These algorithms are very convenient compared with the traditional MPE flow, as they enable MPE without adjusting the model parameters. However, these methods cannot be applied until the compact model of a new device is developed. Therefore, research on generating SPICE models based on ML has been reported, including our papers [11], [12], [13]. SPICE models must reflect changes in transistor size and temperature and accurately respond to circuit performance based on the DC, AC, and transient simulations. In this paper, following the previous study, we propose a fast ANN-based MPE replacement method that reproduces all the characteristics of the existing SPICE model and can further extend the device technology and process parameters. The contributions of this paper are as follows.

1) By adding the temperature and the channel doping depth (L_{CDD}) as variables to the ANN-based compact modeling framework, the predicted performance of the device can be changed accurately and quickly. In particular, it is expected that new process parameters such as L_{CDD}, which do not exist in the existing model parameter set, can be easily reflected.
2) By applying the proposed ANN model to both NSFETs and NC-NSFETs, I-V and C-V curves are predicted very accurately.
3) Based on the extracted ANN-based SPICE model, DC, AC, and transient simulations of digital and analog circuits are fast and accurate.

The overall flow of the proposed method is shown in Fig. 2. The structures and I-V curves of the NSFET and NC-NSFET in Phase 1 are shown in Figs. 3 and 4 in detail. The ANN model in Phase 2 is shown in Fig. 5. The flow is similar to the steps in our previous paper, but the smooth function and Gummel symmetry test (GST)

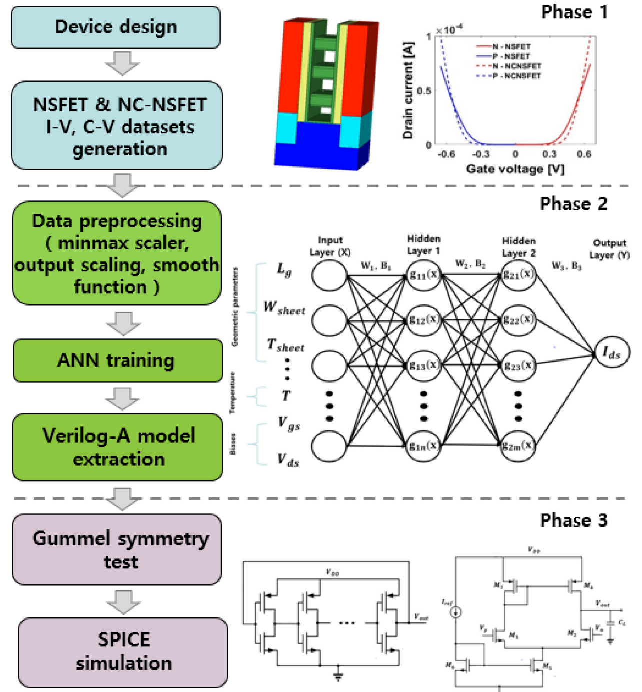

FIGURE 2. The proposed ANN-based model parameter extraction flow.

for next-generation device data and analog simulations are added. In Section II, we present the creation of the datasets for the NSFET and NC-NSFET. Section III describes the ANN-based MPE replacement method. Section IV shows the SPICE model extraction and SPICE simulation results for digital and analog circuits. Finally, Section V summarizes the paper and discusses future work.

II. DEVICE DESIGN AND DATASET GENERATION

The NSFETs and NC-NSFETs were designed and simulated using Synopsys Sentaurus TCAD [14]. The simulation conditions of the NSFET are similar to our previous paper [11]. First, we designed the NSFET device, and compared the electrical characteristics of the NSFET with published NSFET measurement data [15], and then design the NC-NSFET by replacing the ferroelectric (FE) material [16], [17], as shown in Fig. 3. The device structure parameters and HZO parameters are summarized in Table 1. Fig. 3 (c) shows the S curve to confirm the stable operating range of P_r (remnant polarization)-E_c (coercive field). A phase shift occurs between the hysteresis and the change in polarization direction, resulting in a negative capacitance effect, and the Landau-Khalatnikov (L-K) equation is used. If the L-K equation is drawn in the form of an S curve, the red curve in Fig. 3 (c) can be obtained. For the mobility calculation, a quasi-ballistic model according to the short channel length was used, and the Lombardi model and the inversion and accumulation layer model were used to reflect the scattering effect. The Slotboom bandgap narrowing model was used to consider the bandgap changes caused by doping [18]. Shockley-Read-Hall (SRH), Auger, and surface

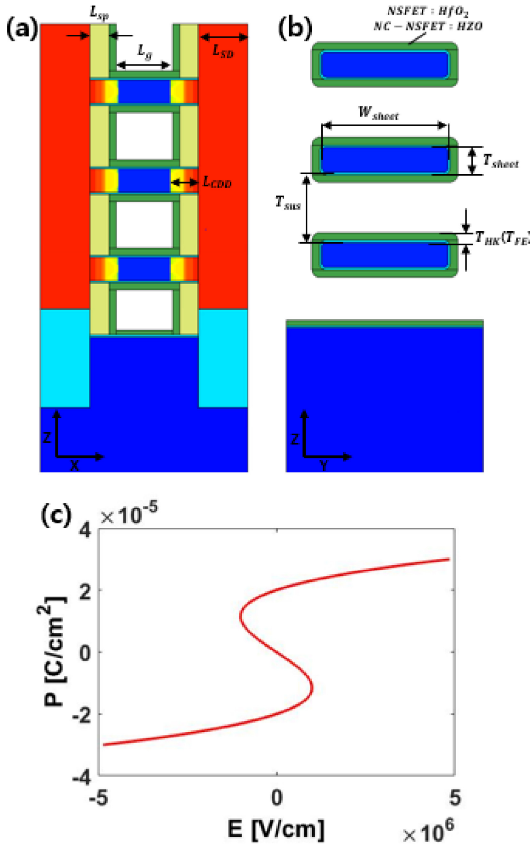

FIGURE 3. (a) The NSFET (NC-NSFET) Y-axis section, (b) the NSFET (NC-NSFET) X-axis section, (c) the NC-NSFET S curve.

TABLE 1. Device geometric parameters and HZO parameters.

Parameters [11]	Values	HZO parameters [16]	Values
L_g $[nm]$	12		
T_{sheet} $[nm]$	5		
W_{sheet} $[nm]$	20 to 50 (at 5 nm intervals)		
$T_{HK}(T_{FE})$ $[nm]$	1.5		
T_{sus} $[nm]$	10	α $[cm/F]$	-6.5e10
L_{SD} $[nm]$	10.5	β $[cm^5/FC^2]$	8.1e19
L_{CDD} $[nm]$	2, 4, 6	ϵ_{FE}	33
C_{Doping} $[cm^{-3}]$	N:1e16 / P:1e15		
SD_{Doping} $[cm^{-3}]$	N:6.5e20 / P:1e21		
T [°C]	-40, 27, 125		
V_{gs} [V]	0 to 0.65		
V_{ds} [V]	0 to 0.65		

SRH were used as recombination models, and the Band-to-Band Tunneling (BTBT) model was also used [19], [20]. To enhance the hole mobility of the P-type NSFET, we applied the stress effect and the silicon <110> direction [21]. For the stress effect calculation, the h-multivalley model [14] and the deformation potential model [22] were used, and the sub-band model was used among piezo models. For the NC-NSFET, the FE polarization model was additionally used to activate the Landau-Khalatnikov equation to calculate the behavior in the negative capacitance region of a FE material [14], [23]. In the case of NC-NSFETs, the electrical properties can be optimized through the FE thickness, FE thickness/DE (dielectric) thickness ratio, P_r, and E_c optimization [24], [25], [26].

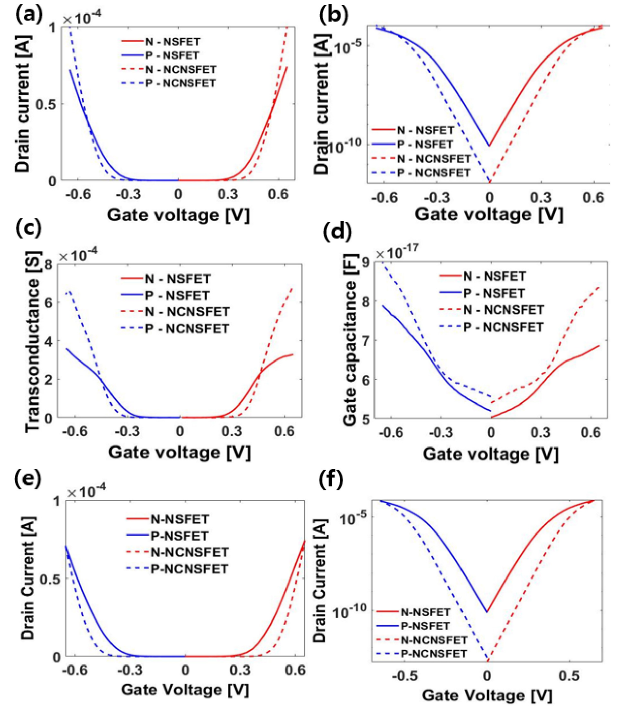

FIGURE 4. Device characteristics (a) I_{ds}-V_{gs}(V_{ds} = 0.65), (b) log scale I_{ds}-V_{gs}(V_{ds} = 0.65), (c) g_m-V_{gs}(V_{ds} = 0.65), (d) C_{gg}-V_{gs}(V_{ds} = 0.65), (e) on-current calibration I_{ds}-V_{gs}(V_{ds} = 0.65), (f) log scale on-current calibration I_{ds}-V_{gs}(V_{ds} = 0.65).

TABLE 2. Electrical characteristics of the NSFET and NC-NSFET.

	NSFET		NC-NSFET	
	N	P	N	P
V_{th} $[V]$	0.21	0.21	0.30	0.30
I_{on} $[A]$	7.4e-5	7.2e-5	1.0e-4	1.0e-4
I_{off} $[A]$	8.4e-11	8.6e-11	1.1e-12	1.6e-12
SS $[mV/dec]$	66	66.4	61.2	61.5
$g_{m,max}$ $[\mu S]$	324.8	348.5	688.5	639.2
R_{out} $[K\Omega]$	42.4	32.5	83.8	77.4

The device performances of the designed NSFET and NC-NSFET are summarized in Fig. 4 and Table 2. Compared to the NSFET, the NC-NSFET improved the on-current by more than 40% and the subthreshold swing (SS) by about 7%. In addition, the increase in transconductance according to the current amplification of the NC-NSFET compared to the NSFET shows that the voltage gain ($A_v = g_m/g_{ds}$) is improved [27]. For low power and improved reliability, the on-current of the NC-NSFET can be adjusted. There is a method of shifting the I-V curve by adjusting the work function, including the aforementioned NC-NSFET optimization method. Figs. 4 (e), (f) show the I-V curves of the presented NSFET and the calibrated NC-NSFET. In this paper, Figs. 4 (a), (b), (c), (d) were used as datasets for expanded modeling of NC-NSFET in NSFET and circuit performance analysis according to improved performance.

III. ANN-BASED MPE REPLACEMENT METHOD

Fig. 5 shows the structure of the ANN-based I-V and C-V models used to implement the proposed MPE method. The

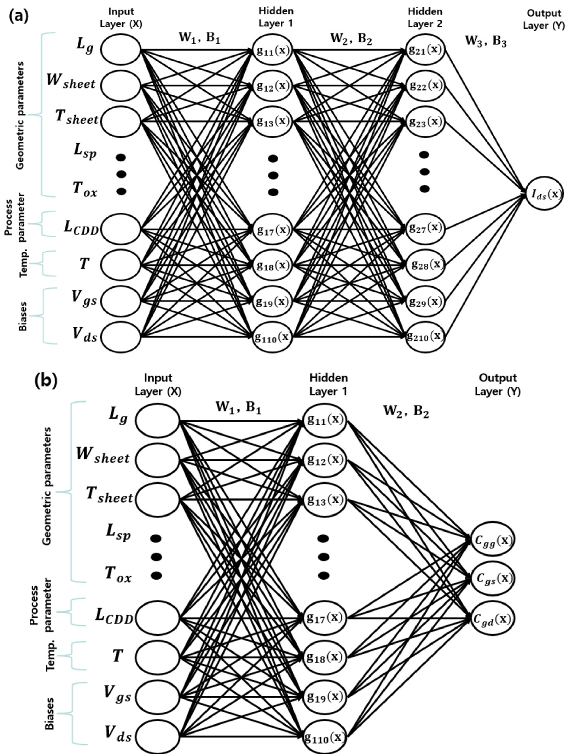

FIGURE 5. The ANN model architecture (a) $I-V$, (b) $C-V$.

input consists of five key geometric parameters (gate length, sheet width, sheet thickness, spacer length, oxide thickness), two terminal voltage biases (V_{gs}, V_{ds}), and the temperature variables. The output consists of electrical characteristics (i.e., the currents and capacitances). In addition, L_{CDD} was added to the input parameter set as a process variable to demonstrate the advantage of the expandability of the model, as shown in Fig. 3 (a). L_{CDD} is a variable representing the depth at which ions are implanted in the channel of the device. In general, the deeper the implantation, the lower the current value due to a decrease in the channel capacitance. For the temperature variable, the range of −40°C to 125°C was used [6]. The gate length, sheet thickness, spacer length, and oxide thickness were fixed to the values presented in Table 1. In addition, the sheet width was configured to be 20 to 50 nm (at 5 nm intervals) to adjust the transistor size. Temperature parameter values were −40, 27, and 125°C, and L_{CDD} values were 2, 4, and 6 nm. A total of 63 device datasets were used. Due to the property of the ANN model, only outputs within the trained range can be accurately predicted. In the datasets presented in this paper, the sheet width, temperature, and L_{CDD} can only be adjusted within specified variable ranges. However, the variable configuration can be freely changed, which was demonstrated in this paper. In the case of a digital circuit, accurate circuit simulation is possible even by training only the device performance according to bit values of 0 ($V_{ds} = 0.05$V) and 1 ($V_{ds} = 0.65$V). However, in the case of an analog circuit, it is possible to predict the performance according to the operating voltage of each transistor in the circuit. Analog circuits can be better modeled by adding more voltage bias data than digital circuits. For this reason, it is important to select a proper grid with appropriate voltage biases. In this paper, I_{ds}-V_{gs} ($V_{ds} = 0.05, 0.325, 0.65$V) and I_{ds}-V_{ds} ($V_{gs} = 0.05, 0.25, 0.325, 0.5, 0.65$V) data were used. For each device, the I-V and C-V curves consist of 30 points. Therefore, the proposed I-V model has 15,120 data samples, and the proposed C-V model has 11,340 data samples. The constructed datasets were divided into training data and test data in a 9:1 ratio. Common methods to reduce the complexity of the model are to measure the sensitivity via the gradients of the input and output [28] and to use principal component analysis (PCA) for dimension reduction [29]. However, in this study, the PCA process was omitted through the knowledge-based method, and only five inputs (in addition to the temperature, L_{CDD}, and voltage biases) that were the most dominant in device performance were selected, which significantly shortened the model training time. In the previous study, we selected only five geometric parameters that can represent more than 98% of the I-V and C-V characteristics of the device. A limitation of this knowledge-based method is that it cannot tune parameters other than the given input parameters. However, in this paper, this drawback can be overcome by easily adding new parameters such as temperature and L_{CDD}. In data preprocessing, a MinMax scaler was applied to the input and a logarithmic scale to the output. In addition, a smooth function suggested in a previous study was applied [13]. As an activation function, tanh is used. The I-V model consists of one input layer, two hidden layers composed of 10 hidden neurons, and one output layer. The C-V model consists of one input layer, one hidden layer composed of 10 hidden neurons, and one output layer. Adam was used as the optimizer for the model training, and a learning rate scheduler was used to gradually decrease the learning rate during epochs. An MSE-based physics-augmented loss function was used as presented in the previous study [11]. Fig. 10 shows the model accuracy according to the number of epochs. The increase in accuracy slows down above 100,000 epochs. In this paper, 200,000 epochs were performed to achieve a stable target error of less than 1%. In addition, early stopping was used to prevent overfitting due to larger epochs. Figs. 6 and 7 are the fitting results for the I-V and C-V curves of NC-NSFETs extracted through the TCAD datasets and the ANN model. Fig. 8 shows the fitting results for the device I-V curves according to the temperature. Fig. 9 shows the fitting results for the device C-V curves according to L_{CDD}. We used the NVIDIA Titan Xp graphics card to accelerate the training of the ANN model. Overall, high accuracy was achieved with less than a 1% error, and the training time took 15 minutes and 10 minutes for the I-V model and the C-V model, respectively. It is possible to produce a SPICE model within an hour, including the time to generate a Verilog-A model through the calculated weights and biases. This shows that significant time savings are possible compared to the very long processing time of the aforementioned traditional MPE. Also, as shown

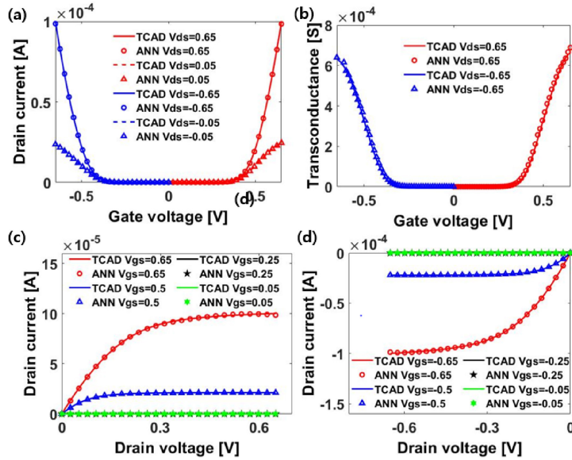

FIGURE 6. NC-NSFET I-V, g_m-V_{gs} fitting results (T = 27°C) (a) I_{ds}-V_{gs}, (b) g_m-V_{gs}, (c) N-type I_{ds}-V_{ds}, (d) P-type I_{ds}-V_{ds}.

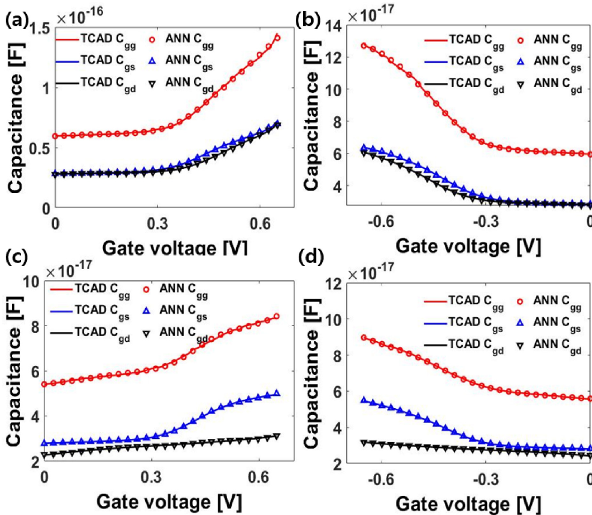

FIGURE 7. NC-NSFET C-V fitting results (T = 27°C) (a) N-type (V_{ds} = 0.05), (b) P-type (V_{ds} = 0.05), (c) N-type (V_{ds} = 0.65), (d) P-type (V_{ds} = 0.65).

in Fig. 11, it can be confirmed that the proposed ANN-based SPICE model has a trade-off relationship between model accuracy and SPICE simulation speed according to the number of layers and nodes. Therefore, it is necessary to adjust the appropriate number of layers and nodes according to the target accuracy and SPICE speed. Our previous study [11] demonstrated that the SPICE speed was faster than a state-of-the-art compact model. Unlike the previous work, which conducted model training through five structural parameters representing more than 98% of the device, in this paper, temperature and L_{CDD} variables were newly added and model training was conducted with seven parameters. Designers can easily add any parameters they want to tune to extract the desired ML-based SPICE model. In other words, if the user of the proposed framework has simple ML and python knowledge, it can be expanded to the desired ANN model within one day (excluding the dataset generation period).

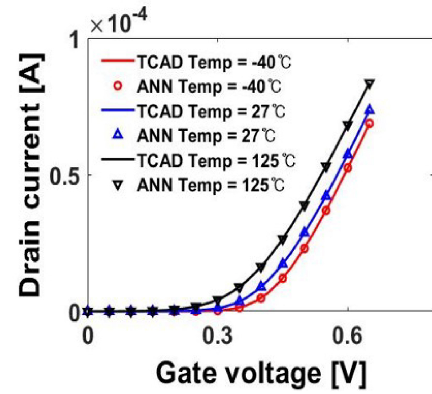

FIGURE 8. N-type NSFET I_{ds}-V_{gs} according to the temperature.

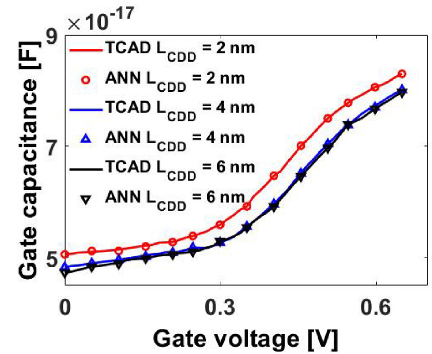

FIGURE 9. N-type NC-NSFET C_{gg}-V_{gs} according to the channel doping depth.

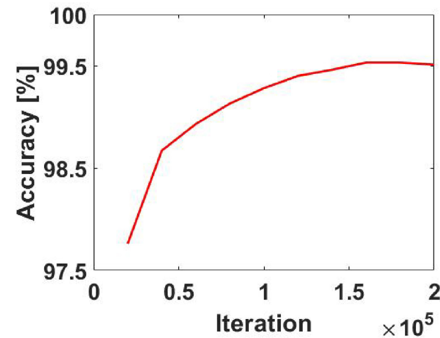

FIGURE 10. Model accuracy vs. the number of epochs.

IV. SPICE SIMULATION FOR DIGITAL AND ANALOG CIRCUITS

The ANN-based Verilog-A model proposed for SPICE simulation is constructed as shown in Fig. 12. In order to reflect the transistor sizing in the circuit, a variation of the sheet width of 20 to 50 nm (at 5 nm intervals) was applied to the datasets for training. In addition, the number of fins was set as a variable in the Verilog-A model parameters so that the I-V and C-V characteristics according to the number of fins were reflected. As shown in Fig. 12, the current and capacitance are calculated with the voltage biases given in SPICE. Also, even if a current source is given as an input, SPICE can internally convert it into an equivalent voltage

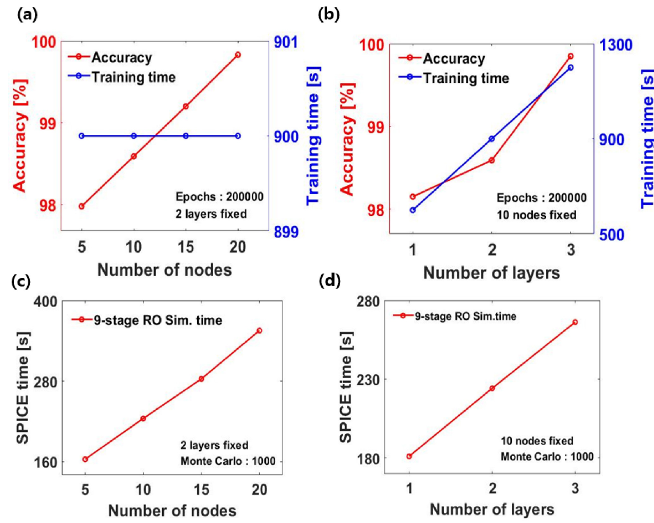

FIGURE 11. Performances of the ANN-model according to (a) the number of nodes, (b) the number of layers. SPICE simulation time according to (c) the number of nodes, (d) the number of layers.

1. Module(MOS) and terminal(D,G,S,B) definition

2. Extracted weights(W), biases(B) and hidden layer output(A) variable definition

3. Input(X), output(Y) and Number of FIN variable definition

4. ANN I-V model calculation
4.1 $Hidden\ layer1: A^1 = W^1 * X + B^1$
4.2 $Hidden\ layer1\ Activation\ function: tanh(A^1)$
4.3 $Hidden\ layer2: A^2 = W^2 * A^1 + B^2$
4.4 $Hidden\ layer2\ Activation\ function: tanh(A^2)$
4.5 $Output\ layer: Y = W^3 * A^2 + B^3$

5. ANN C-V model calculation
5.1 $Hidden\ layer1: A^1 = W^1 * X + B^1$
5.2 $Hidden\ layer1\ Activation\ function: tanh(A^1)$
5.3 $Output\ layer: Y_CV = W^2 * A^1 + B^2$

6. $C_{gg}, C_{gs}, C_{gd}, C_{gb}$ calculation
6.1 $C_{gg} = Number\ of\ FIN * Y_CV1$
6.2 $C_{gd} = Number\ of\ FIN * Y_CV2$
6.3 $C_{gs} = Number\ of\ FIN * Y_CV3$
6.4 $C_{gb} = C_{gg} - C_{gs} - C_{gd}$

7. $I_{ds}, I_{gd}, I_{gs}, I_{gb}$ calculation
7.1 $I_{ds} < +Number\ of\ FIN * (Y) * V(d,s)$
7.2 $I_{gd} < +C_{gd} * ddt(V(g,d))$
7.3 $I_{gs} < +C_{gs} * ddt(V(g,s))$
7.4 $I_{gb} < +C_{gb} * ddt(V(g,b))$

8. gm, gds calculation
8.1 gm = ddx(I(d,s), V(g,s))
8.2 gds = ddx(I(d,s), V(d,s))

9. END

FIGURE 12. The proposed ANN-based Verilog-A model.

bias. Therefore, if a current source is an input, simulation is possible without problems. Fig. 13 shows harmonic balance plots and the GST results up to the 4th derivative performed to evaluate the DC/AC symmetry of the ANN-based Verilog-A model [30]. The higher-order derivative of the GST means that the higher-order harmonic analysis is more accurate. Differentiation appeared up to the third order and the fourth order [12], [13], respectively. In this paper, the smooth function was used in the data preprocessing phase to improve the non-differentiation point as the order increased, and the accuracy of the model was verified through AC simulation of the analog circuit. As shown in Fig. 14, the

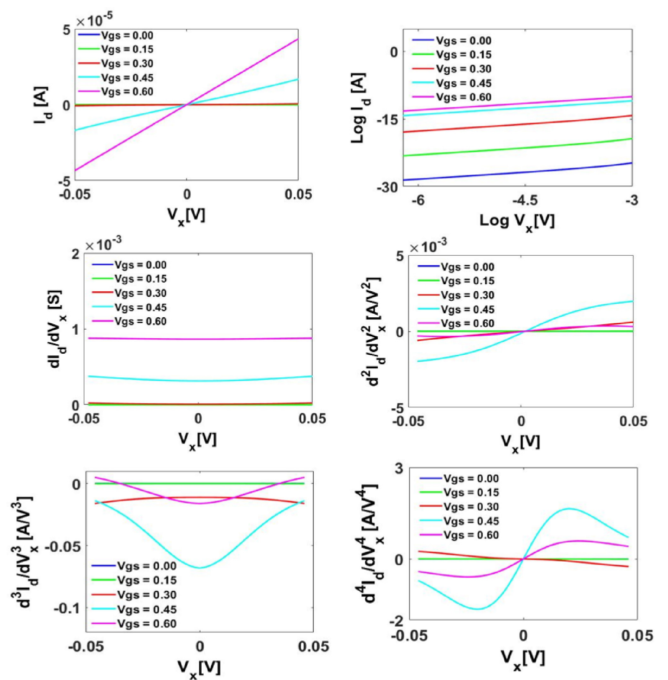

FIGURE 13. Gummel symmetry test results of the proposed ANN model.

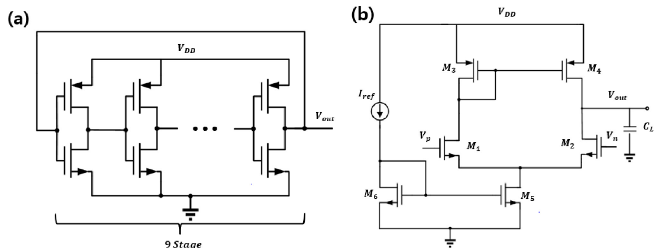

FIGURE 14. (a) 9-stage ring oscillator circuit, (b) 5-transistor OTA circuit.

simulation was performed by adopting a 9-stage ring oscillator (RO) as a digital circuit and a 5-transistor operational transconductance amplifier (OTA) as an analog circuit. To confirm the versatility in a large circuit, a 4-bit ALU circuit was adopted and the simulation was performed [31]. Also, to verify the accuracy of the circuit simulation, the error was compared with the BSIM-CMG 111.1 model. In case of the RO, transient simulation was performed from 0 to 300 ps. In case of the OTA, AC simulation was performed from 100 Hz to 1000 MHz in units of decades. Transistor sizing was adjusted in a ratio of $M_{1,2}$:$M_{3,4}$:M_5:M_6=5:10:2:1, and it was designed with a load capacitance of 100 fF and a reference current of 70 μA [27], [32]. In case of the 4-bit ALU, transient simulation was performed from 0 to 500 ps. We compared the delay of out[0:3] from a[0:3] under the condition of an adder input b[0:3] = [1, 0, 1, 1]. The delay of ALU in Tables 3 and 4 is the delay between a[1] and out[1].

Simulated waveforms for NSFET and NC-NSFET are shown in Fig. 15. Tables 3 and 4 compare circuit performance and accuracy of the proposed ANN model with

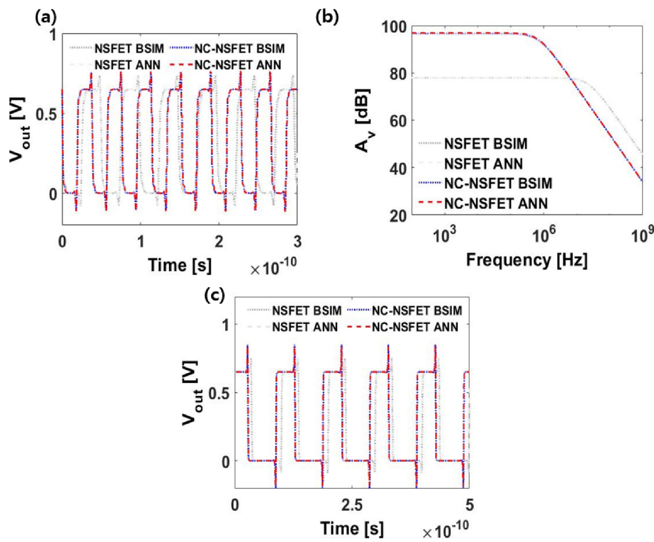

FIGURE 15. (a) 9-stage ring oscillator, (b) 5-transistor OTA, (c) 4-bit ALU waveform.

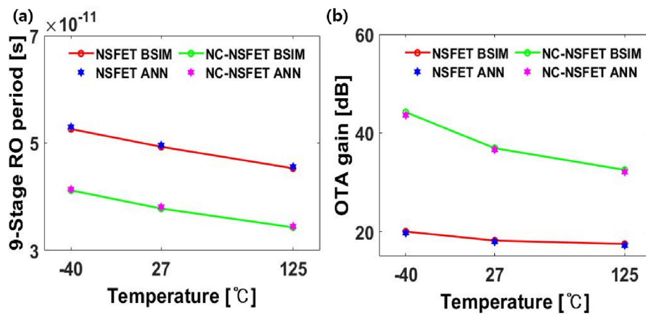

FIGURE 16. Performance changes according to the temperature. (a) 9-stage ring oscillator period, (b) 5-transistor OTA gain.

the BSIM-CMG model for NSFET and NC-NSFET at room temperature (T = 27°C). The proposed ANN model showed less than a 0.5% difference for the NSFET and less than a 1% difference for the NC-NSFET compared to the BSIM model of 9-stage RO circuit performance. The performance of the 5-transistor OTA circuit using the proposed ANN model for the NSFET and NC-NSFET showed less than a 3% difference compared to the BSIM model. The performance of the 4-bit ALU circuit using the proposed ANN model for the NSFET and NC-NSFET showed less than a 2.5% difference compared with the BSIM model. In both the BSIM model and the ANN model, the circuit speed of the NC-NSFET was 1.2 times faster than that of the NSFET with the 9-stage RO circuit, and the power was improved by about 30%. In the 5-transistor OTA circuit, the gain is improved by 1.2 times and the power was improved by about 10%. Even in the 4-bit ALU, circuit speed was improved by 1.5 times and the power was improved by about 10%. Fig. 16 shows the delay and gain of the circuits of the ANN model and the BSIM model according to the temperature value. The proposed ANN model showed less than a 1% difference in the 9-stage RO delay compared to the BSIM model according to the temperature change, and the 5-transistor OTA gain showed

TABLE 3. Comparison of the proposed ANN model and the BSIM-CMG model for the NSFET circuits.

		NSFET		
		BSIM	Proposed ANN	Diff. [%]
9-stage RO	T(period) [ps]	49.56	49.31	0.50
	Power [μW]	30.58	30.45	0.43
5-transistor OTA	Gain [db]	78.18	77.94	0.29
	Bandwidth [MHz]	23.70	24.20	2.06
	Power [μW]	52.46	52.58	0.23
4-bit ALU	Delay [ps]	63.59	62.25	2.11
	Power [μW]	63.77	63.55	0.34

TABLE 4. Comparison of the proposed ANN model and the BSIM-CMG model for the NC-NSFET circuits.

		NC-NSFET		
		BSIM	Proposed ANN	Diff. [%]
9-stage RO	T(period) [ps]	38.06	37.75	0.81
	Power [μW]	21.45	21.43	0.09
5-transistor OTA	Gain [db]	96.90	96.60	0.31
	Bandwidth [MHz]	0.74	0.76	2.63
	Power [μW]	46.73	46.85	0.25
4-bit ALU	Delay [ps]	40.74	39.95	1.94
	Power [μW]	56.85	56.80	0.09

less than a 2% difference. It was proved that the proposed method accurately represents the circuit performance according to the temperature change. It is known that a Verilog-A model is much slower than the BSIM-CMG model in simulation [13]. As shown in [11], a Verilog-A model is 5 to 6 times slower than the C-version model. Compared to the equivalent Verilog-A model, the ANN-based model is much simpler and faster than the BSIM-CMG model which is based on all the complex charge equations. If the ANN-based model is implemented in C language, it can be much faster than the BSIM-CMG SPICE model [11].

V. CONCLUSION

The existing MPE method has to go through a complicated fitting flow with more than a thousand model parameters as device scaling is accelerated. In this paper, we proposed a new ANN-based MPE replacement flow, by breaking away from the existing MPE flow, and demonstrated the ease of extended modeling for next-generation device technologies, such as the NSFET and NC-NSFET circuits, with less than a 1% error compared to TCAD. The application expandability of the digital and analog circuits was demonstrated by confirming the difference between the ANN-based model and the BSIM model within 1% for the digital circuit and within 3% for the analog circuit. In addition to the key device structural parameters, the temperature and channel doping depth variables were newly added and modeled. Then, the accuracies of circuit performance changes according to these variables were evaluated. The proposed MPE replacement flow is flexible enough to allow users to easily add or delete desired parameters for SPICE models.

In future research, we intend to conduct a study to analyze the statistical performance distribution of devices by reflecting the threshold voltage V_{th} mismatch according to various

process variations in the model. The statistical device and circuit analysis can be done by sampling the model parameters through the Monte Carlo method or improved methods [33]. ML techniques, such as the ANN proposed in this study, are expected to show considerable strength in process variation analysis and optimization compared to existing methods.

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