Received 28 October 2022; revised 12 December 2022 and 21 January 2023; accepted 26 January 2023. Date of publication 7 February 2023; date of current version 22 February 2023. The review of this article was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2023.3242968

Effect of Amorphous Layer at the Heterogeneous Interface on the Device Performance of β-Ga_2O_3/Si Schottky Barrier Diodes

ZHENYU QU [1,2], WENHUI XU [1] (Member, IEEE), TIANGUI YOU [1,2], ZHENGHAO SHEN [1,2], TIANCHENG ZHAO [1,2], KAI HUANG [1,2], AILUN YI [1], DAVID WEI ZHANG [3] (Member, IEEE), GENQUAN HAN [4] (Member, IEEE), XIN OU [1,2] (Senior Member, IEEE), AND YUE HAO [4] (Senior Member, IEEE)

1 State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
2 Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing 100049, China
3 School of Microelectronics, Fudan University, Shanghai 200433, China
4 State Key Discipline Laboratory of Wide Bandgap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, China

CORRESPONDING AUTHORS: T. YOU and X. OU (e-mail: t.you@mail.sim.ac.cn; ouxin@mail.sim.ac.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 62293520, Grant 62293521, Grant 62174167, and Grant 61874128; in part by the Shanghai Rising-Star Program under Grant 22QA1410700; in part by the Shanghai Basic Research Project under Grant 22JC1403300; in part by the Key Research Project of Zhejiang Laboratory under Grant 2021MD0AC01; and in part by the K. C. Wong Education Foundation under Grant GJTD-2019-11.

(Zhenyu Qu and Wenhui Xu contributed equally to this work.)

ABSTRACT Heterogeneous integration of β-Ga_2O_3 with Si substrate is considered as an effective and low-cost technology for the thermal management of β-Ga_2O_3 electrical devices. In this work, an isotype heterojunction of n-Ga_2O_3/n^+-Si (Ga_2O_3/Si) was fabricated by surface activated bonding in which an amorphous layer was induced by ion beam bombardment. The current density of Ga_2O_3/Si Schottky barrier diodes (SBDs) are about two orders of magnitude lower than that of Ga_2O_3 bulk SBDs at 2.8 V due to the influence of amorphous layer. The results are consistent with the simulation results when β-Ga_2O_3 Mole Fraction (MF = n(β-Ga_2O_3)/[n(β-Ga_2O_3) + n(SiO_2)]) and thickness of amorphous layers (T_{ox}) are set at 0.83 and 3 nm, respectively. Furthermore, devices with different MF and T_{ox} were simulated based on the nonlocal tunneling model by Sentaurus TCAD. The decrease of β-Ga_2O_3 Mole Fraction and increase of amorphous layers thickness in the hetero-interface of Ga_2O_3/Si SBDs lead to a dramatic degeneration of current density and specific on-resistance in Ga_2O_3/Si SBDs. These results may provide some guidance for improvement of vertical heterogeneous integration β-Ga_2O_3 devices performance.

INDEX TERMS β-Ga_2O_3, Schottky barrier diode, hetero-interface, TCAD simulation.

I. INTRODUCTION

As a promising semiconductor material, β-Ga_2O_3 has attracted extensive attentions because of its ultra-wide band gap of 4.8 eV and ultra-high breakdown field strength of 8 MV/cm. Baliga's figure-of-merit (BFOM) of β-Ga_2O_3 is far superior to that of Si and surpasses its counterparts as SiC and GaN [1], [2], [3]. It means that β-Ga_2O_3 devices are especially suitable for the high-power applications with low power dissipation. Furthermore, large-size β-Ga_2O_3 single crystals can be fabricated by the melt-grown method as the case of Si [4], which could reduce the fabrication cost of β-Ga_2O_3 wafers and improve the upper limit of its crystallization quality. Thanks to the excellent electrical properties of β-Ga_2O_3, MOSFETs [5], [6], [7], [8], [9], [10] and Schottky barrier diodes (SBDs) [11], [12], [13], [14], [15] with breakdown voltage of several kV class have been fabricated which demonstrate the great potential of β-Ga_2O_3 in the field of power electronics. However, the natural low thermal conductivity of β-Ga_2O_3, which is 0.1∼0.3 W/cm·K (only about 1/8 of that of Si) [2], [3], results in severe

self-heating effect of β-Ga_2O_3 high-power devices. The heat dissipation is a key hindrance to the large-scale applications of β-Ga_2O_3 power devices. One of the prospective solutions is to integrate β-Ga_2O_3 thin films onto a foreign substrate with high thermal conductivity [16], such as Si. On the other hand, with the heterogeneous integration of β-Ga_2O_3 and Si, Ga_2O_3/Si cascade structure can be realized similar to the case of GaN/Si cascade [17], which is used to achieve the normally off devices avoiding the dilemma in the fabrication of p-type β-Ga_2O_3 [18]. Nevertheless, it is difficult to integrate high-quality β-Ga_2O_3 thin films onto Si substrate by using hetero-epitaxial method because of the large mismatch in the lattice constant and the coefficient of thermal expansion. In the previous work, the integration of single-crystal β-Ga_2O_3 films onto Si substrates were successfully achieved by ion-cutting technique [19], [20]. However, due to the limit of surface activation bonding, there was an amorphous layer at the interface of Ga_2O_3/Si hetero-structure induced by Ar bombardment during the bonding process [20], [21], [22], which degraded the device performance of vertical Ga_2O_3/Si power device [20]. Although the amorphous layer can be eliminated by high temperature annealing [21], the interdiffusion of elements at the heterogeneous interface of Ga_2O_3/Si is very serious at high temperature as mentioned in Liang's work [23], which is inevitable in the fabrication process of heterogeneous vertical β-Ga_2O_3-based power device. In addition, the thickness of the amorphous layer is apparently an important parameter which can influence the electrical transport properties of Ga_2O_3/Si hetero-structure. Therefore, it is necessary to investigate effect of elemental composition and thickness of amorphous layer on the electrical transport of Ga_2O_3/Si hetero-structure.

In this work, Ga_2O_3/Si SBDs and Ga_2O_3 bulk SBDs were fabricated by surface activated bonding (SAB) technique and wafer thinning. High resolution transmission electron microscope (HRTEM) was used to characterize the interface quality of Ga_2O_3/Si, and the element interdiffusion at the Ga_2O_3/Si interface with a temperature of 900 °C was confirmed by scanning transmission electron microscope (STEM) energy dispersive spectroscopy (EDS). The device performance of Ga_2O_3/Si SBDs and Ga_2O_3 bulk SBDs were measured by Keiythley ACS 4200 and the experimental results were compared with the simulation results to clarify the reliability of the simulation. Finally, to further investigate the effect of the amorphous layer on the Ga_2O_3/Si SBDs, Sentaurus TCAD was used to compare the device performance of Ga_2O_3/Si SBDs with different amorphous layer properties, including the thickness (T_{ox}) and the elemental composition which is represented by β-Ga_2O_3 Mole Fraction (MF = n(β-Ga_2O_3)/[n(β-Ga_2O_3) + n(SiO_2)]).

II. DEVICE FABRICATION AND SIMULATION METHODOLOGY

The fabrication process flow of the Ga_2O_3/Si SBDs is schematically illustrated in Fig. 1(a). The doping concentrations of 650 μm (-201) β-Ga_2O_3 wafers purchased from

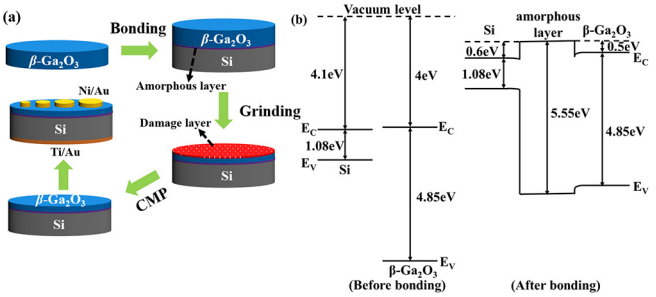

FIGURE 1. (a) Process flow of Ga_2O_3/Si SBDs. (b) Schematic band diagram of Ga_2O_3/Si SBDs before bonding and after bonding.

TABLE 1. Material parameters used for simulation.

Material	β-Ga_2O_3	Si	SiO_2
Band gap(eV)	4.85	1.08	9
Electron affinity (eV)	4	4.10	0.9
Relative dielectric constant	10	11.7	3.9
Effective electron mass	0.28	1.09	0.42
Room-temperature electron mobility($cm^2/V{\cdot}s$)	115	1417	-
Saturation electron velocity (cm/s)	2×10^7	1.07×10^7	-

Novel Crystal Technology and 500 μm Si wafers were 2×10^{17} cm^{-3} and 5×10^{19} cm^{-3}, respectively. Prior to wafer bonding, the β-Ga_2O_3 wafer and the Si wafer were both cleaned by alcohol and acetone solutions. After that, the β-Ga_2O_3 and Si wafers were activated by Ar ion beam source with a voltage of 1.0 kV and current of 100 mA. The SiO_2 naturally formed on the surface of the Si wafer was also removed during this process. After surface activation, the β-Ga_2O_3 and Si wafers were bonded at room temperature with a pressure of ~2.5MPa. More details of SAB process can be found in [22] and [24]. The bonded β-Ga_2O_3 wafer of the Ga_2O_3/Si hetero-structure was thinned to 35 μm by FD3803 Grinding equipment and a following chemical mechanical polishing (CMP) was used to remove the damaged region induced by grinding. After CMP, the Ga_2O_3/Si hetero-structure was obtained with a β-Ga_2O_3 layer thickness of 30 μm. For comparison, β-Ga_2O_3 wafer without wafer bonding was thinned to 30 μm by the same thinning process to fabricate Ga_2O_3 bulk SBDs. For both Ga_2O_3/Si and thinned Ga_2O_3 bulk wafer, Ni/Au (30/100 nm) electrodes with diameters of 200 μm were deposited by electron beam evaporation on the β-Ga_2O_3 surface to form Schottky contacts. Ti/Au (50/100 nm) Ohmic electrodes were deposited on the Si surface and thinned Ga_2O_3 bulk back surface by magnetron sputtering.

Sentaurus TCAD was used to simulate the device performance of SBDs on Ga_2O_3/Si and thinned Ga_2O_3 bulk. The electron affinity and band gap of β-Ga_2O_3 were adjusted to be 4 eV [25] and 4.85 eV, respectively. Furthermore, the electron mobility of β-Ga_2O_3 was set at 115 $cm^2/V{\cdot}s$ [26]. Material parameters used for simulation are summarized in Table 1. The doping concentrations of

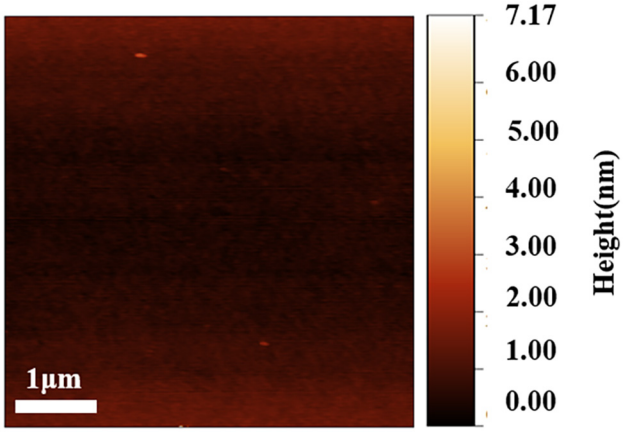

FIGURE 2. **AFM images of Ga_2O_3/Si surface topography after the grinding and CMP processes.**

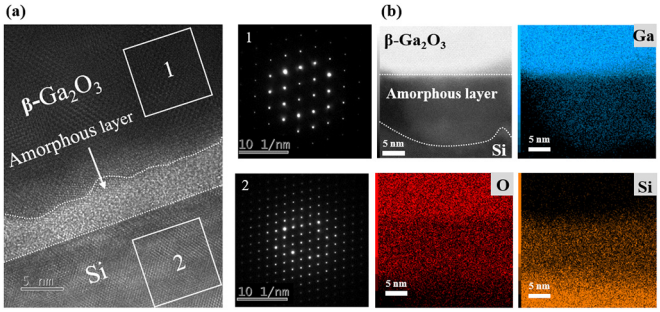

FIGURE 3. **(a) Cross-sectional TEM micrograph of the Ga_2O_3/Si interface. The inset 1, 2 represent the selected area electron diffraction patterns of Ga_2O_3 region and Si region. (b) EDS spectrum of Ga, O, Si at the Ga_2O_3/Si interface at 900 °C for 30 min.**

β-Ga_2O_3 and Si were defined as 2×10^{17} and 5×10^{19} cm^{-3}, respectively, which were consistent with that used in the experiments. Furthermore, the dopants were assumed to be completely ionized. Fermi-Dirac model, Shockley-Read-Hall (SRH) recombination model, Auger recombination model and doping dependent mobility model were used to improve the accuracy of simulation. High field saturation model was used to describe the carrier drift velocity saturation in high electric field [27]. Heterogeneous interface model used in the simulation can introduce double points at the heterointerfaces in the case of abrupt heterojunctions to avoid a large barrier error [28]. Besides, the nonlocal tunneling model was used to study the tunneling mechanism at the interface between β-Ga_2O_3 and Ni/Au Schottky electrode as well as the Ga_2O_3/Si interface [28]. Schematic band diagram of Ga_2O_3/Si SBDs before bonding and after bonding are illustrated in Fig. 1 (b), in which the MF and T_{ox} were 0.83 and 3 nm at zero bias, respectively. Considering the electron affinity of β-Ga_2O_3 and Si used in the simulation, the band offset at the bottom of the conduction band is 0.1 eV in the ideal case. However, with an amorphous layer inserted at the Ga_2O_3/Si interface, the barrier for electrons in Si to move through the amorphous layer is higher, which is about 0.6 eV.

III. RESULTS AND DISCUSSION

To characterize the quality of Ga_2O_3/Si hetero-structure, SBDs on Ga_2O_3/Si and Ga_2O_3 bulk were fabricated and characterized. Atomic force microscope (AFM) images of Ga_2O_3/Si surface topography can be found in Fig. 2. After grinding and following CMP, the root mean square roughness of Ga_2O_3/Si surface was 1.2 nm, which is flat enough for the device fabrication. A cross-sectional transmission electron microscope (TEM) micrograph and selected area electron diffraction (SAED) patterns of the β-Ga_2O_3/Si interface after annealing at 470 °C for 3 min are shown in Fig. 3 (a). No obvious crack or void was observed at the β-Ga_2O_3/Si interface, indicating that β-Ga_2O_3 and Si were well bonded. In addition, an amorphous layer with a thickness of ~4 nm at the interface is induced by Ar ion bombardment, which is consistent with previous reports [20], [21], [22]. The inset 1, 2 illustrate selected area electron diffraction patterns of Ga_2O_3 region and Si region respectively, which are marked in Fig. 3 (a). The bright and regular patterns in the inset 1 and 2 indicate the single crystal quality of Ga_2O_3 and Si. However, the crystal quality of Ga_2O_3/Si interface was aggravated after annealing at high temperature. To confirm the effect of high temperature annealing on the Ga_2O_3/Si interface, EDS was conducted at the Ga_2O_3/Si interface at high temperature of 900 °C for 30 min and the EDS spectrum of Ga, O, Si is shown in Fig. 3 (b). The interdiffusion of Ga, Si elements into the Ga_2O_3/Si interface occurred at high temperature which leads to a thicker amorphous layer in Fig. 3 (b) than that of Fig. 3 (a) annealed at 475°C for 3 min [23]. It indicates the potential of optimizing the amorphous layer at the hetero-interface by varying the annealing conditions.

The J-V characteristics of the Ga_2O_3/Si and Ga_2O_3 bulk SBDs are measured and used to calibrate the simulation, as shown in Fig. 4 (a) and (b). The E in the label represents the experiment results while S represents the simulation results. The current density of Ga_2O_3 bulk SBDs exceed the measurement limit of the instrument after the forward voltage is higher than 2.8 V in Fig. 4 (a). It is found that the measured J-V are basically consistent with simulated J-V characteristics of the Ga_2O_3/Si SBDs when T_{ox} and MF of the simulated Ga_2O_3/Si SBDs are 3 nm and 0.83, respectively. Compared with Ga_2O_3 bulk SBDs, the current density of Ga_2O_3/Si SBDs are much smaller which is verified in experimental and simulation results as shown in Fig. 4 (c). To understand the reason for the decrease of current density, the specific on-resistance extracted by dV/dJ ($R_{on,sp,d}$) of Ga_2O_3 bulk SBDs and Ga_2O_3/Si SBDs were compared in Fig. 4 (d). It can be easily accepted that the $R_{on,sp,d}$ of Ga_2O_3/Si SBDs is the sum of the thinned Ga_2O_3 layer resistance, the Si substrate resistance, the Ga_2O_3/Si interface resistance and the contact resistance, whereas the $R_{on,sp,d}$ of Ga_2O_3 bulk SBDs is only the sum of the thinned Ga_2O_3 layer resistance and the contact resistance. According to the resistivity of Si [29],

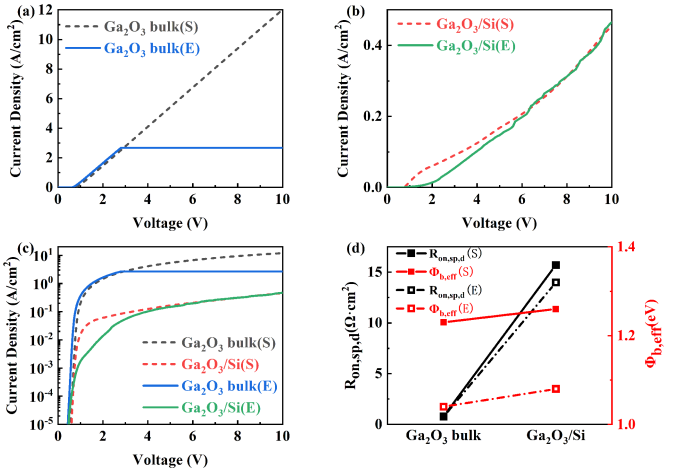

FIGURE 4. Simulated and measured (a) linear J-V curve of Ga_2O_3 bulk SBDs, the current reached the compliance limit after 2.8 V in the experiment. (b) linear J-V curve of Ga_2O_3/Si SBDs. (c) semi logarithmic J-V curve Ga_2O_3 bulk SBDs and Ga_2O_3/Si SBDs. (d) $R_{on,sp,d}$ and effective barrier height of Ga_2O_3 bulk SBDs and Ga_2O_3/Si SBDs.

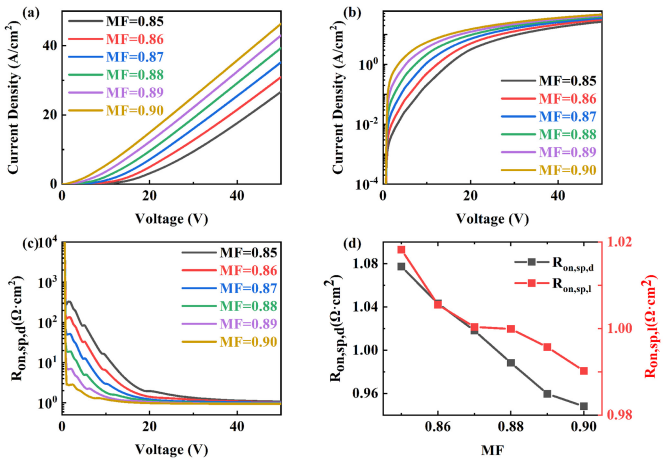

FIGURE 5. (a) Linear J-V curves, (b) semi-logarithmic J-V curves, (c) $R_{on,sp,d}$-V curves, and (d) comparison of $R_{on,sp,d}$ and $R_{on,sp,I}$ of Ga_2O_3/Si SBDs with different MF.

its specific on resistance is only about 7×10^{-5} Ω·cm^2, which is several orders of magnitude lower than the total $R_{on,sp,d}$ of the Ga_2O_3/Si SBDs. Thus, the influence of the Si substrate on $R_{on,sp,d}$ can be ignored. The $R_{on,sp,d}$ of Ga_2O_3 bulk SBDs is extracted to be about 0.8 Ω·cm^2, which is only about 6% of that of Ga_2O_3/Si SBDs at 10 V. Therefore, the $R_{on,sp,d}$ of Ga_2O_3/Si SBDs is dominated by the Ga_2O_3/Si interface resistance instead of the thinned Ga_2O_3 layer resistance and contact resistance at 10 V.

The most important factor is the Ga_2O_3/Si interface. Owing to the difference between the work function of highly doped Si substrate and Ga_2O_3 layer, an electron barrier is formed at the Ga_2O_3/Si interface that prevents electrons transporting from Si substrate to β-Ga_2O_3 layer, which was also reported by Wang et al. [20]. Ga_2O_3/Si SBD can be considered as a combination of β-Ga_2O_3 SBD and Ga_2O_3/Si isotype heterojunction. It increases the effective barrier height for electron to flow from Ti/Au Ohmic electrode to Ni/Au Schottky electrode in Ga_2O_3/Si SBDs and decreases the current density of Ga_2O_3/Si SBDs. Moreover, due to the existence of the amorphous layer at the Ga_2O_3/Si interface, the barrier height at Ga_2O_3/Si interface further increases to 0.6 eV, as shown in Fig. 1 (b), which lead to the increase of $R_{on,sp,d}$ and significant decrease of current density. The effective barrier height ($\Phi_{b,eff}$) of Ga_2O_3 bulk and Ga_2O_3/Si SBDs is calculated by (1):

$$\Phi_{b,eff} = \frac{kT}{q}\ln\left(\frac{A^*T^2}{J_0}\right) \tag{1}$$

where A* is the Richard constant, k is the Boltzmann constant, T is the absolute temperature, and J_0 is the reverse saturated current density extracted by the intercept of the linear region of fitted lnJ-V plot. The measured $\Phi_{b,eff}$ of SBDs are lower than that of simulated one. It may be caused by the high density of defects at the Schottky interface which increases the ideality factor and decreases the extracted $\Phi_{b,eff}$ [30]. The root mean square roughness larger than 1 nm extracted from AFM images after CMP also implies a high density of defects at the Schottky interface. Besides, the $\Phi_{b,eff}$ of Ga_2O_3/Si SBDs are slightly higher than that of Ga_2O_3 bulk SBDs due to the electron barrier at the Ga_2O_3/Si interface.

As the amorphous layer plays an important role in the device performance of Ga_2O_3/Si SBDs, the MF in the amorphous layer was used to study the effect of element composition changing of the amorphous layer on the device performance induced by the post-annealing process. In the simulation, the thickness of amorphous layer was fixed at 4 nm. The linear and semi logarithmic J-V characteristic curves of Ga_2O_3/Si SBDs with different MF are plotted in Fig. 5 (a) and (b), respectively. The current increases exponentially at low voltages and enter the linear region gradually at high voltages in ideal SBDs. However, an additional region where the current increases nonlinearly is observed before the linear region as the existence of the amorphous layer at Ga_2O_3/Si interface. The nonlinear region widens as the MF decreases, which is clearly shown in Fig. 5 (b). Besides, the current density of Ga_2O_3/Si SBDs increases with the increasing MF. It is caused by the diffusion of Ga element at the Ga_2O_3/Si interface resulting in the decrease of barrier height. According to the Wenzel-Kramers-Brillouin (WKB) approximation, the tunneling probability T at the interface barrier can be expressed by (2) [31]:

$$T \cong \exp\left(-\frac{2}{\hbar}\int_0^d |k(x)|dx\right) \tag{2}$$

where k(x) is the wave vector within the barrier and d is the width of the barrier. For a rectangular barrier with a barrier height of $q\Phi_B$ and a barrier width of d, (2) can be approximated as following [31]:

$$T \cong \exp\left(-\alpha d\sqrt{\Phi_B}\right) \tag{3}$$

where α is a constant. It is clear that the decrease of barrier height at the interface leads to the increase of tunneling probability, which increases the tunneling current through the heterogeneous-interface, and therefore increases the current density of Ga_2O_3/Si SBDs. The MF dependent $R_{on,sp,d}$ versus applied voltage is shown in Fig. 5 (c). The $R_{on,sp,d}$ keeps constant at high voltages, corresponding to the linear increase of current density. The Ga_2O_3/Si SBDs with low MF working in the linear region require a higher voltage than Ga_2O_3/Si SBDs with higher MF. To confirm the above specific on-resistance extracted by dV/dJ, which is labeled as $R_{on,sp,d}$ in Fig. 5 (d), a linear fitting method reported by Cheung and Cheung [32] is used to extracted the specific on-resistance as expressed by (4):

$$\frac{dV}{d(\ln J)} = R_{on,sp}J + \frac{nkT}{q} \tag{4}$$

where n is the ideality factor. The $R_{on,sp}$ can be derived from the slopes of the fitting curves, which is labeled as $R_{on,sp,l}$ in Fig. 5 (d). Both of $R_{on,sp,d}$ and $R_{on,sp,l}$ decrease with increasing MF, indicating that Ga diffusion is beneficial to improve SBDs performance. Ga elemental diffusion commonly occurs during high temperature annealing [22], [24], [33], which can alleviate the performance degradation induced by the amorphous layer. The $R_{on,sp,l}$ and $R_{on,sp,d}$ are all about 1 $\Omega{\cdot}cm^2$, which is 0.2 $\Omega{\cdot}cm^2$ higher than the $R_{on,sp,d}$ of Ga_2O_3 bulk SBDs, implying that the Ga_2O_3/Si interface resistance accounts for about 20% of the total resistance at a high voltage. The $\Phi_{b,eff}$ of Ga_2O_3/Si SBDs is constant around 1.26 $\pm$ 0.1 eV with MF varying from 0.85 to 0.90, which is consistent with that of the Ni/β-Ga_2O_3 [34]. It is noted that the extracted $\Phi_{b,eff}$ is dominated by the Schottky barrier, since the barrier height of the amorphous layer at heterogenous interfaces shown in Fig. 1 (b) is much lower than that of Schottky interface.

The thickness of the amorphous layer between heterogeneous interfaces varies with the activation parameters during the bonding process and post annealing conditions. Therefore, the effect of T_{ox} on the device performance of Ga_2O_3/Si SBD was investigated with MF = 0.9. Fig. 6 (a) and (b) show the J-V curves of Ga_2O_3/Si SBD with varying T_{ox} in linear scale and semi-logarithmic scale, respectively. It is clear that the current density of Ga_2O_3/Si SBDs decreases with the increasing T_{ox} from 0 nm to 5 nm. This can also be explained by (3). The increase of T_{ox} decreases the tunneling probability, consequently reducing the current density of Ga_2O_3/Si SBDs. It is noted that there is no significant difference between the J-V curves of T_{ox} = 0 nm, T_{ox} = 1 nm and T_{ox} = 2 nm, suggesting that the current degradation can be ignored when T_{ox} is less than 2 nm. Fig. 6 (c) shows that with the increasing T_{ox}, $R_{on,sp,d}$ increases and approaches to a constant at a higher voltage, suggesting that the device working in the linear region needs a higher voltage. It can be considered that the breakdown of amorphous layer occurs in the linear region and the breakdown voltage increases with the increase of the

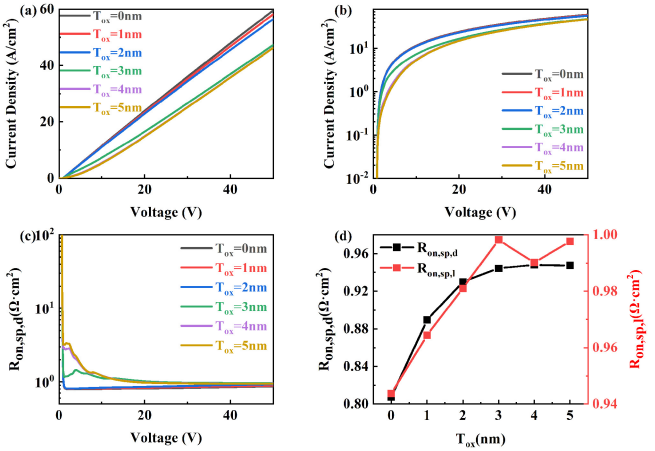

FIGURE 6. (a) Linear J-V curves, (b) semi-logarithmic J-V curves, (c) $R_{on,sp,d}$-V curves, and (d) comparison of $R_{on,sp,d}$ and $R_{on,sp,l}$ of Ga_2O_3/Si SBDs with different T_{ox}.

T_{ox} [35]. Therefore, the devices with a thicker amorphous layer require a higher voltage to work in the linear region. Besides, it can be seen that the widening of nonlinear region is limited when the T_{ox} < 2 nm. Fig. 6 (d) shows the $R_{on,sp,d}$ and $R_{on,sp,l}$ extracted by derivation method and linear fitting method. Overall, both of $R_{on,sp,d}$ and $R_{on,sp,l}$ increase with the increase of T_{ox} as a result of the increasing of Ga_2O_3/Si interface resistance. It is noted that the $R_{on,sp,l}$ of Ga_2O_3/Si SBDs without amorphous layer is 0.808 $\Omega{\cdot}cm^2$, which is very close to the $R_{on,sp,d}$ of Ga_2O_3 bulk SBDs, confirming that the Si substrate resistance can be ignored. The results above indicates that it is feasible to improve the device performance of Ga_2O_3/Si SBDs by optimizing bonding and annealing conditions.

IV. CONCLUSION

In conclusion, the effect of amorphous layer at the heterogeneous interface on device performance of Ga2O3/Si SBD was systematically investigated. HRTEM and SAED confirm the existence of amorphous layer at the Ga2O3/Si interface, which has a thickness of ~4 nm. The interdiffusion of Ga, Si and increase of Tox occurred at the hetero-interface after high temperature annealing. The current density of Ga2O3/Si SBDs are about two orders of magnitude lower than that of Ga2O3 bulk SBDs at 2.8V due to the existence of amorphous layer. The simulation results suggests that the device performance of the Ga2O3/Si SBDs gradually degrade with the decrease of MF and the increase of Tox. It means that the device performance can be recovered by appropriate annealing process with enhanced Ga diffusion and reduced Tox. This work highlights the importance of heterogeneous interface optimization for further β-Ga2O3 device designs on heterogeneous integration materials. High quality Ga2O3/Si SBDs with negligible performance degradation are expected to be fabricated when the MF and Tox can be further optimized by varying bonding and annealing conditions.

REFERENCES

[1] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3(010) substrates," *Appl. Phys. Lett.*, vol. 100, no. 1, Jan. 2012, Art. no. 13504.

[2] S. J. Pearton et al., "A review of Ga_2O_3 materials, processing, and devices," *Appl. Phys. Lett.*, vol. 5, no. 1, Jan. 2018, Art. no. 11301.

[3] S. J. Pearton, F. Ren, M. Tadjer, and J. Kim, "Perspective: Ga_2O_3 for ultra-high power rectifiers and MOSFETS," *J. Appl. Phys.*, vol. 124, no. 22, Dec. 2018, Art. no. 220901.

[4] Z. Galazka et al., "Czochralski growth and characterization of β-Ga_2O_3 single crystals," *Cryst. Res. Technol.*, vol. 45, no. 12, pp. 1229–1236, Dec. 2010, doi: 10.1002/crat.201000341.

[5] K. Tetzner et al., "Lateral 1.8 kV β-Ga_2O_3 MOSFET With 155 MW/cm^2 power figure of merit," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1503–1506, Sep. 2019, doi: 10.1109/LED.2019.2930189.

[6] S. Sharma, K. Zeng, S. Saha, and U. Singisetti, "Field-plated lateral Ga_2O_3 MOSFETs with polymer passivation and 8.03 kV breakdown voltage," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 836–839, Jun. 2020, doi: 10.1109/LED.2020.2991146.

[7] Z. Hu et al., "Enhancement-mode Ga_2O_3 vertical transistors with breakdown voltage >1 kV," *IEEE Electron Device Lett.*, vol. 39, no. 6, pp. 869–872, Jun. 2018, doi: 10.1109/LED.2018.2830184.

[8] K. Zeng, A. Vaidya, and U. Singisetti, "1.85 kV breakdown voltage in lateral field-plated Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 9, pp. 1385–1388, Sep. 2018, doi: 10.1109/LED.2018.2859049.

[9] K. Zeng, A. Vaidya, and U. Singisetti, "A field-plated Ga_2O_3 MOSFET with near 2-kV breakdown voltage and 520 mΩ·cm^2 on-resistance," *Appl. Phys. Exp.*, vol. 12, no. 8, Jul. 2019, Art. no. 81003.

[10] Y. Lv et al., "Lateral β-Ga_2O_3 MOSFETs with high power figure of merit of 277 MW/cm^2," *IEEE Electron Device Lett.*, vol. 41, no. 4, pp. 537–540, Apr. 2020, doi: 10.1109/LED.2020.2974515.

[11] N. Allen et al., "Vertical Ga_2O_3 Schottky barrier diodes with small-angle beveled field plates: A Baliga's figure-of-merit of 0.6 GW/cm^2," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1399–1402, Sep. 2019, doi: 10.1109/LED.2019.2931697.

[12] X. Huang et al., "3.4 kV breakdown voltage Ga_2O_3 trench Schottky diode with optimized trench corner radius," *ECS J. Solid-State Sci. Technol.*, vol. 9, no. 4, Apr. 2020, Art. no. 45012.

[13] K. Konishi et al., "1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes," *Appl. Phys. Lett.*, vol. 110, no. 10, Mar. 2017, Art. no. 103506.

[14] S. Kumar, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Vertical β-Ga_2O_3 Schottky barrier diodes with trench staircase field plate," *Appl. Phys. Exp.*, vol. 15, no. 5, Apr. 2022, Art. no. 54001.

[15] J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, "2300V reverse breakdown voltage Ga_2O_3 Schottky rectifiers," *ECS J. Solid-State Sci. Technol.*, vol. 7, no. 5, pp. Q92–Q96, May 2018, doi: 10.1149/2.0241805jss.

[16] W. Xu et al., "First demonstration of waferscale heterogeneous integration of Ga_2O_3 MOSFETs on SiC and Si substrates by ion-cutting process," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2019, pp. 1–4.

[17] Y. Wei, M. M. Hossain, and A. Mantooth, "Evaluation of the high performance 650 V cascode GaN FET under low temperature," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Redondo Beach, CA, USA, 2021, pp. 236–241.

[18] A. Kyrtsos, M. Matsubara, and E. Bellotti, "On the feasibility of p-type Ga_2O_3," *Appl. Phys. Lett.*, vol. 112, no. 3, Jan. 2018, Art. no. 32108.

[19] Y. Wang et al., "β-Ga_2O_3 MOSFETs on the Si substrate fabricated by the ion-cutting process," *Sci. China Phys. Mech.*, vol. 63, no. 7, Apr. 2020, Art. no. 277311.

[20] Z. Wang, D. Takatsuki, J. Liang, T. Kitada, N. Shigekawa, and M. Higashiwaki, "Fabrication of n-Si/n-Ga_2O_3 heterojunctions by surface-activated bonding and their device performance," *J. Appl. Phys.*, vol. 131, no. 7, Feb. 2022, Art. no. 74501.

[21] W. Xu et al., "Efficient thermal dissipation in wafer-scale heterogeneous integration of single-crystalline β-Ga_2O_3 thin film on SiC," *Fundam. Res.*, vol. 1, no. 6, pp. 691–696, Nov. 2021, doi: 10.1016/j.fmre.2021.11.003.

[22] Y. Xu, F. Mu, Y. Wang, D. Chen, X. Ou, and T. Suga, "Direct wafer bonding of Ga_2O_3–SiC at room temperature," *Ceram. Int.*, vol. 45, no. 5, pp. 6552–6555, Apr. 2019, doi: 10.1016/j.ceramint.2018.11.220.

[23] J. Liang et al., "Fabrication of β-Ga_2O_3/Si heterointerface and characterization of interfacial structures for high-power device applications," *Jpn. J. Appl. Phys.*, vol. 61, Mar. 2022, Art. no. SF1001.

[24] F. Mu et al., "A comparison study: Direct wafer bonding of SiC–SiC by standard surface-activated bonding and modified surface-activated bonding with Si-containing Ar ion beam," *Appl. Phys. Exp.*, vol. 9, no. 8, Jul. 2016, Art. no. 81302.

[25] M. Mohamed, K. Irmscher, C. Janowitz, Z. Galazka, R. Manzke, and R. Fornari, "Schottky barrier height of Au on the transparent semiconducting oxide β-Ga_2O_3," *Appl. Phys. Lett.*, vol. 101, no. 13, Sep. 2012, Art. no. 132106.

[26] A. Parisini, and R. Fornari, "Analysis of the scattering mechanisms controlling electron mobility in β-Ga_2O_3 crystals," *Semicond. Sci. Technol.*, vol. 31, no. 3, Feb. 2016, Art. no. 35023.

[27] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Trans. Electron Devices*, vol. ED-22, no. 11, pp. 1045–1047, Nov. 1975, doi: 10.1109/T-ED.1975.18267.

[28] *Sentaurus Device User Guide, Version O-2018.06*, Synopsys Inc., Mountain View, CA, USA, 2018.

[29] C. Bulucea, "Recalculation of Irvin's resistivity curves for diffused layers in silicon using updated bulk resistivity data," *Solid-State Electron.*, vol. 36, no. 4, pp. 489–493, Apr. 1993, doi: 10.1016/0038-1101(93)90257-Q.

[30] S. Ahn, F. Ren, L. Yuan, S. J. Pearton, and A. Kuramata, "Temperature-dependent characteristics of Ni/Au and Pt/Au Schottky diodes on β-Ga_2O_3," *ECS J. Solid-State Sci. Technol.*, vol. 6, no. 1, pp. P68–P72, Jan. 2017, doi: 10.1149/2.0291701jss.

[31] A. M. Kiefer, D. M. Paskiewicz, A. M. Clausen, W. R. Buchwald, R. A. Soref, and M. G. Lagally, "Si/Ge junctions formed by nanomembrane bonding," *ACS Nano*, vol. 5, no. 2, pp. 1179–1189, Jan. 2011, doi: 10.1021/nn103149c.

[32] S. K. Cheung and N. W. Cheung, "Extraction of Schottky diode parameters from forward current-voltage characteristics," *Appl. Phys. Lett.*, vol. 49, no. 2, pp. 85–87, Jul. 1986, doi: 10.1063/1.97359.

[33] H. N. Masten, J. D. Phillips, and R. L. Peterson, "Effects of high temperature annealing on the atomic layer deposited HfO_2/β-Ga_2O_3(010) interface," *J. Appl. Phys.*, vol. 131, no. 3, Jan. 2022, Art. no. 35106.

[34] L. A. M. Lyle et al., "Effect of metal contacts on (100) β-Ga_2O_3 Schottky barriers," *J. Vac. Sci. Technol. A*, vol. 39, no. 3, Mar. 2021, Art. no. 33202.

[35] D. J. Dumin, "Oxide wearout, breakdown, and reliability," *Int. J. High Speed Electron. Syst.*, vol. 11, no. 3, pp. 617–718, 2001, doi: 10.1142/S0129156401000988.