Received 3 December 2022; revised 4 January 2023; accepted 4 January 2023. Date of publication 17 January 2023;
date of current version 21 February 2023. The review of this article was arranged by Editor M. Chan.

Digital Object Identifier 10.1109/JEDS.2023.3237386

Floating Fin Shaped Stacked Nanosheet MOSFET for Low Power Logic Application

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This work was supported by Inha University Research Grant.

ABSTRACT In this paper, floating fin structured vertically stacked nanosheet gate-all-around (GAA) metal oxide semiconductor field-effect transistor (FNS) is proposed for low power logic device applications. To verify the electrical performance of the proposed device, three-dimensional (3-D) technology computer-aided design (TCAD) device/circuit simulations are performed with calibrated device model parameters. As a result, it is found that gate propagation delay (τ_{delay}) and dynamic power (P_{dyn}) are improved by 8% and 19%. respectively as compared to conventional vertically stacked lateral nanosheet (LNS). Through the rigorous analysis on the resistance and capacitance components of FNS and LNS, it is clearly revealed that the τ_{delay} and P_{dyn} are improved at the same P_{dyn} (50 μW) and τ_{delay} (187 GHz) by the reduced effective capacitance which results from the diminished gate-to-sorece/drain overlap area. Based on the TCAD simulation studies, it is expected that the FNS is suitable for next generation logic digital applications.

INDEX TERMS GAA MOSFET, parasitic capacitance, inverter propagation delay, dynamic power, area scaling.

I. INTRODUCTION

The scaling of complementary metal-oxide-semiconductor (CMOS) has been investigated since the emergence of semiconductor integrated circuits [1]. There are several options to sustain the scaling-down for future semiconductor devices. Among various devices after Fin field-effect transistor (FinFET) technology, gate-all-around (GAA) MOSFETs have been considered as one of the most promising devices [2], [3]. Thanks to two main reasons. The first is excellent gate controllability and the second is compatibility with the FinFET process [4], [5]. However, single GAA MOSFETs with a circular-shaped channel have the disadvantage that the current per unit area is lower than FinFETs.

To overcome this challenge, vertically stacked GAA-MOSFETs with lateral nanosheet (NS)-shaped channels (LNS) have been extensively studied to enhance the current per unit area [5], [6], [7]. However, unfortunately, LNS has the disadvantage that the effective capacitance is significantly increased by the overlap capacitance between source/drain (S/D) and channel to-channel space (T_{sp}) [7] with the enhancement of the current drivability per unit area as contrast to conventional FinFETs.

Thus, the gate propagation delay (τ_{delay}) is degraded by the increased effective capacitance and the dynamic power (P_{dyn}) is also more consumed although the τ delay is maintained. To mitigate the degradation of the device performances, the process to introduce the inner spacers between the channels has been considered [5]. However, there is a disadvantage in terms of fabrication cost since the formation of the inner spacers requires additional process steps. Also, it is hard to form the inner spacers with ideal rectangular

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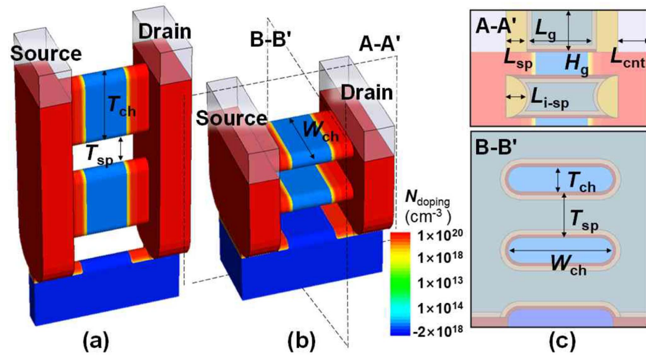

FIGURE 1. (a) Three dimensional (3-D) structure of the proposed fin shaped NS device (FNS). (b) Structure of the conventional lateral NS MOSFETs (LNS). (c) Cross-section view of the LNS and the definition of the parameters representing each dimensions.

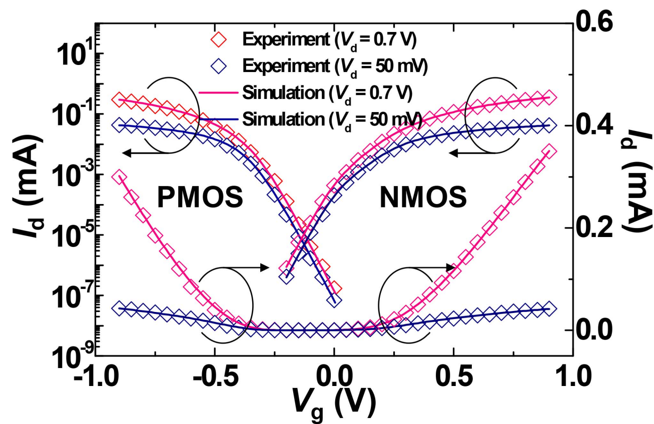

FIGURE 2. Drain current (I_d) – gate voltage (V_g) [drain voltage (V_d) = 0.7 V and 50 mV for n-MOSFET (NMOS) and V_d = −0.7 V and −50 mV for p-MOSFET (PMOS)] are represented for experimental and simulation data calibration [9].

shape [8]. Unexpectedly, a semicircular shape is formed by selectively etching the SiGe used as a sacrificial layer, which halves the effects of the overlap capacitance reduction.

In this paper, a novel fin-shaped vertically stacked NS device (FNS) is proposed to improve power, performance and area (PPA) as shown in Fig. 1(a). In order to confirm the feasibility of FNS, the process flow, which improves the structural weak point of LNS, is demonstrated. Furthermore, to verify the device/circuit-level performances, the gains of the τ_{delay} and the P_{dyn} are extracted from inverter characteristics with geometric parameters of Fig. 1(c) and the origin of the performance improvement is rigorously investigated by analyzing the capacitance and resistance components of FNS and LNS.

II. DEVICE INFORMATION AND CALIBRATION CONDITION

A. CALIBRATION CONDITIONS

For accurate technology computer-aided design (TCAD) simulations, model parameters are calibrated by referring the experimental data with two channels stacked on top of bulk Si where the stacked nanowires are modeled based on the transmission electron microscope (TEM) images [9]. Then, drift-diffusion approximation is applied under 0.7 V of supplied voltage (V_{dd}) condition to calibrate drain current (I_d)-gate voltage (V_g) characteristics as shown in Fig. 2. Shockley-Read-Hall (SRH) and Lombardi models are calibrated to reflect generation-recombination and mobility of carriers, respectively [10]. Also, quantum confinement is considered owing to thin channel thickness (T_{ch}) and threshold voltage (V_{th}) is tuned by adjusting the work-function of metal. Based on the calibrated models for the short channel nanowire devices with high-κ/metal gate structure [11], (100)<110> mobility (LNS) and (110)<110> mobility (FNS) are reflected using Lombardi auto-orientation model depending on the channel orientation of each device. A contact resistivity of $\rho_C = 1 \times 10^{-10}$ Ω-cm^2 is used in LNS and FNS to evaluate advanced technology nodes, and the resistivity value referred from the experimental results of previous studies. [12], [13]. Here, it should be noted that two stacked channels are utilized for the simulations of FNS and LNS. Recently, there was the report that the number of channel stacks is limited in terms of power and performance. At the same V_{dd}, speed gain can be maximized up to 4 stacks and it starts to decrease with the number of stacks larger than 4. Also, the speed gain at the same power continuously decreases as the number of stacks increases. These phenomena can be explained by noticing that the increase of the current tends to be diminished with the increasing number of stacks due to the increase of series resistance [14]. Thus, 2 or 3 stacks have been considered as an optimal number and thereby FNS and LNS with 2-stacked channels are evaluated by considering the complexity and feasibility of the fabrication process.

TABLE 1. Device parameters for evaluation.

Parameters	LNS	FNS	Parameters	LNS	FNS
Number of Stacks	2		Effective Width (W_{eff})	116 nm	
Gate Height (H_g)	20 nm		Effective Gate Length (L_{eff})	13 nm	
Channel Width (W_{ch})	25 nm	7 nm	Channel space (T_{sp})	15 nm	
Channel Thickness (T_{ch})	7 nm	25 nm	Spacer Length (L_{sp})	5.5 nm	
Bottom Fin Height (H_{fin})	3 nm		Inner Spacer Length ($L_{i\text{-}sp}$)	5.5 nm	
HfO_2 Thickness (T_{hk})	15 Å		S/D Doping ($N_{S/D}$)	1×10^{21} cm^{-3}	
SiO_2 Thickness (T_{ox})	7 Å		Channel Doping (N_{CH})	5×10^{17} cm^{-3}	

B. DEVICE STRUCTURE

The device parameters of LNS and FNS with the vertically stacked two NSs based on the 3-nm node of the international roadmap for devices and systems (IRDS) 2018 [15] are shown in Table 1. LNS has channel width (W_{ch}) of 25 nm and T_{ch} of 7 nm whereas W_{ch} of 7 nm and T_{ch} of 25 nm are applied to FNS. Accordingly, both the devices have the same effective width (W_{eff}) of 116 nm by the formula $[W_{ch} \times \pi + (T_{ch} - W_{ch}) \times 2] \times 2$ and $[T_{ch} \times \pi + (W_{ch} - T_{ch}) \times 2] \times 2$, respectively. For both LNS and FNS, gate length (L_g) of 15 nm and effective gate length (L_{eff}) of 13 nm are used where L_{eff} is defined by L_g without overlap length. NS-to-NS space (T_{sp}) is 15 nm, inner

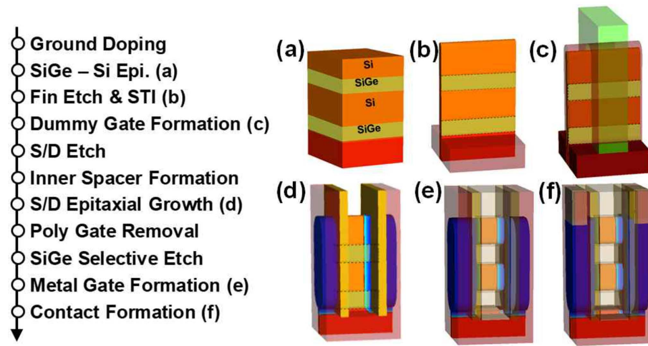

FIGURE 3. Process flow for fabricating the FNS device.

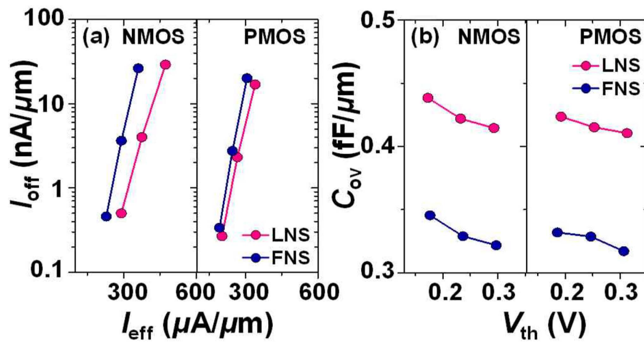

FIGURE 4. (a) Effective current (I_{eff}) and off current (I_{off}) correlation plot of FNS and LNS for NMOS and PMOS. (b) Correlation plot of threshold voltage (V_{th}) and Overlap capacitance (C_{ov}) for NMOS and PMOS. C_{ov} is extracted by applying a frequency of 1 MHz.

spacer length ($L_{i\text{-}sp}$) is 5.5 nm, spacer thickness (L_{sp}) is 5.5 nm, channel doping concentration (N_{CH}) of 5×10^{17} and S/D doping concentration ($N_{S/D}$) of 1×10^{21} cm^{-3} are applied.

C. PROCESS FLOW

The fabrication process flow of the FNS is highly compatible with LNS as shown in Fig. 3. Although FNS has the disadvantages in terms of increasing the number of stacks since fins should be vertically stacked, FNS is applicable through the improvement of the current channel stacking process in the case of stacking 2 or 3 channels which has been considered as an optimal number in terms of power and performance.

The most remarkable difference from the LNS is that the thicker epitaxial growth of Si (T_{Si}) is required than that of SiGe (T_{SiGe}) for the formation of the channels [Fig. 3(a)] where the T_{Si} and T_{SiGe} determine the T_{ch} and the T_{sp}, respectively. After fins are patterned [Fig. 3(b)], dummy poly gate [Fig. 3(c)] and S/D with inner spacers [Fig. 3(d)] are formed sequentially. It should be noted that the metal gates and the S/D face each other with the gate dielectric and semicircle-shaped inner spacer in between after the metal gate formation process of Fig. 3(e). It means that the dielectric area (namely, multiplication of W_{ch} and T_{sp}) between the metal gates and the S/D serves as an undesired S/D overlap capacitance (C_{ov}) which is V_g-independent (constant capacitance). In this regard, the FNS can diminish the C_{ov} effectively by reducing the W_{ch} without the change of the W_{eff}.

Additionally, in FNS, the increase of width can be simply implemented by modulating the fin height for the enhanced current as contrast to LNS where it is difficult to increase the width of the nanosheet because it affects multi-V_{th} process margin by changing the space between nanosheets with different V_{th} or between NMOS and PMOS [16].

III. RESULTS AND DISCUSSION

A. BASIC ELECTRICAL CHARACTERISTICS

Effective current (I_{eff}) vs. off current (I_{off}) correlation plot are described in Fig. 4(a). The three different V_{th}s are implemented by changing the work function to evaluate the current drivability and capacitance. Compared to LNS, FNS has the degraded I_{eff} by 20% and 9% for n-MOSFET (NMOS) and p-MOSFET (PMOS), respectively (at fixed I_{off} of 1nA/μm) although other main electrical parameters such as V_{th} and subthreshold swing (SS) are not significantly different. For the NMOSs of LNS/ FNS, the V_{th}s are 236/232 mV and the SSs are 69.9/69.7 mV/dec, respectively.

In terms of capacitances, the V_{th}-C_{ov} correlation plot [Fig. 4(b)] shows that the C_{ov} of FNS is decreased by 22% (NMOS) and 25% (PMOS), respectively as compared to LNS. Based on the similar reduction amount of the C_{ov} for the entire V_{th} regions ($\sim$90 aF/μm), it can be noticed that the constant capacitance component of the C_{ov} is reduced. By evaluating the difference of the I_{eff}-I_{off} and V_{th}-C_{ov} characteristics between LNS and FNS, it is expected that geometry-dependent parasitic capacitance and resistance components might affect the electrical characteristics significantly.

B. CAPACITANCE ANALYSIS

To analyze the C_{ov} difference between LNS and FNS, it is necessary to define all the composition of effective capacitance (C_{eff}) including the C_{ov}. One-stage inverter capacitance can be defined as the total C_{eff}. Considering the operation of an inverter, the C_{eff} is divided into the C_{in} (capacitance from previous node), the C_{out} (that from output node), and the fan-out (FO). capacitance (C_{fo}) [17] as shown in Fig. 5 and equation (1).

$$C_{eff} = C_{in} + C_{out} + C_{fo} \quad (1)$$

Here, the C_{in} and C_{out} are composed of gate capacitance (C_{gg}), gate-to-drain capacitance (C_{gd}), and drain to body capacitance (C_{db}) [18]. The capacitance for the n-type device (C_{nmos}) and that for the p-type (C_{pmos}) are separately considered. Since the inverter oscillates between 0 V and V_{dd}, each capacitance component is also modulated between a depletion mode capacitance [$C_{(dep.)}$] and an inversion mode capacitance [$C_{(inv.)}$] depending on the inverter bias condition [19], [20], [21]. Thus, the C_{in} and the C_{out} can be expressed as below.

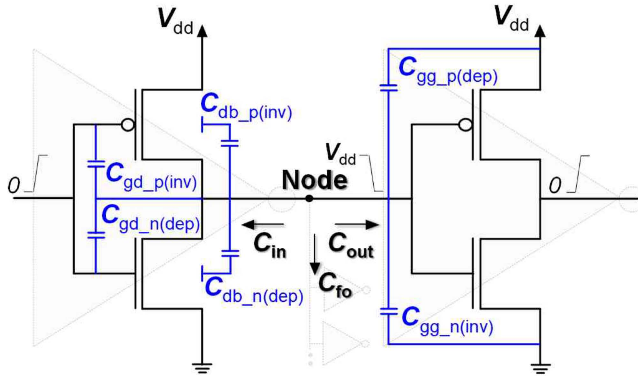

FIGURE 5. Capacitance modeling of two inverter chains when the signal is propagated through them. Input and output capacitance seen from the node (C_{in}), (C_{out}) and fan-out capacitance (C_{fo}) are defined from the specified node located between the inverters.

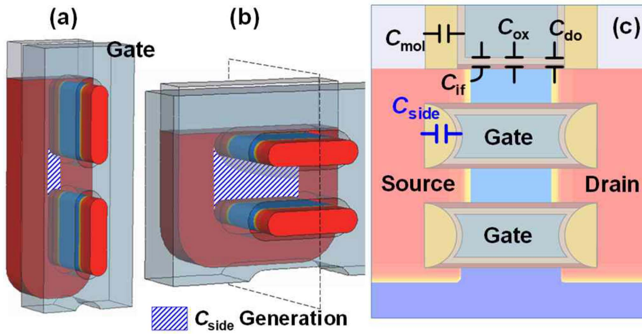

FIGURE 6. Area which contribute to gate to S/D capacitance through inner spacers (C_{side}) in (a) FNS and (b) LNS. (c) Definition of detailed capacitance parameters constituting C_{eff}.

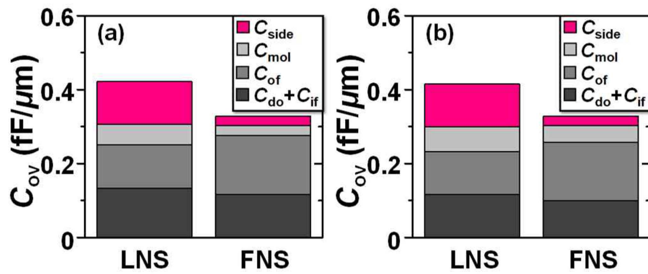

FIGURE 7. Stacked bar charts for capacitance component analysis of FNS and LNS. for (a) NMOS and (b) PMOS.

$$C_{in} = 2\left[C_{gd_{p(inv.)}} + C_{gd_{n(dep.)}}\right] + C_{db_p(inv.)} + C_{db_n(dep.)} \quad (2)$$

$$C_{out} = C_{gg_p(dep.)} + C_{gg_n(inv.)} \quad (3)$$

Furthermore, two representative capacitance components, equations (4) and (5), $C_{gg(inv.)}$ ($V_g = V_{dd}$, $V_d = 0$ V) and $C_{gg(dep.)}$ ($V_g = 0$ V, $V_d = 0$ V), consist of the gate to S/D fringing capacitance through spacers (C_{of}), the gate to S/D fringing capacitance across the channel (C_{if}), the gate to S/D overlap capacitance (C_{do}), the gate-to-channel capacitance (C_{ox}), and the parasitic capacitance between the gate and S/D contact metal (C_{mol}) as depicted in Fig. 6(c). Here, note that the C_{ov} is the half of the $C_{gg(dep.)}$. Considering the signal oscillation of ring oscillator, the summation of all these capacitances becomes the C_{eff} because the capacitances are connected in parallel at the node that located between two inverters.

$$C_{gg(inv.)} = C_{ox} + C_{do} + C_{of} + C_{side} + C_{mol} \quad (4)$$

$$C_{gg(dep.)} = C_{if} + C_{do} + C_{of} + C_{side} + C_{mol} \quad (5)$$

It should be noted that the constant gate-to-S/D capacitance through inner spacers (C_{side}) is inevitably added to both $C_{gg(dep.)}$ and $C_{gg(inv.)}$ by the metal gate formation process of LNS and FNS, which degrades the device performance [22]. However, it is clearly observed that the FNS has the reduced C_{side} [reduced shaded overlap area in Figs. 6(a) and (b)]. In order to investigate the effect of C_{side} on C_{ov}, each capacitance components are compared between FNS and LNS [Figs. 7(a) and (b)]. As a result, it is found that the C_{ov}s of FNS are decreased by 89 (NMOS) and 90 (PMOS) aF/μm compared to LNS due to the reduction of the C_{side}.

C. RESISTANCE ANALYSIS

Although FNS has the capacitance reduction, the degradation of the I_{eff} is accompanied. To reveal the origin of the I_{eff} degradation and to enhance the I_{dsat}, its resistance components are rigorously analyzed. In the stacked GAA-MOSFETs, over-drive linear resistance (R_{odlin}) can be divided into channel resistance (R_{ch}), extension resistance (R_{ext}) [23]. Equivalent resistance circuits for LNS and FNS can be described as shown in Figs. 8(a) and (b) where the R_{ch} and the R_{ext} of each layer are connected in series. Thus, the R_{odlin} can be expressed as following equation (6).

$$R_{odlin} = R_{ext} + R_{ch} \quad (6)$$

Importantly, Figs. 9(a) and (b) indicate the comparison of the R_{ext} and the R_{ch} between the LNS and FNS. The analysis on each resistance is performed using linear regression by applying the same over-drive voltage (V_{od}) which is 0.5 V for NMOS and –0.5 V for PMOS (from V_{th} of the devices). As shown in Fig. 9(a), the R_{ch} increased by 28 $\Omega\cdot\mu$m for NMOS and decreased by 37 $\Omega \cdot \mu$m for PMOS in FNS compared to LNS. This R_{ch} difference can be explained by that of mobility because FNS and LNS have the different channel orientations of (110)<110> and (100)<110>. In Fig. 9(b), R_{ext} of the FNS is increased (NMOS 134 $\Omega \cdot \mu$m, PMOS 140 $\Omega\cdot\mu$m) compared to the LNS by the due to the reduction of S/D contact area and the increase of S/D height. The current contributed by the bottom fin region is negligible for LNS and FNS since the region has the high doping concentration (namely, large resistance) by ground doping.

D. GATE DELAY AND DYNAMIC POWER ANALYSIS

To estimate the AC characteristics of the FNS, inverter performances are analyzed. Especially, τ_{delay} (7) and P_{dyn} (8), which are function of C_{eff}, inverter effective resistance (R_{eff})

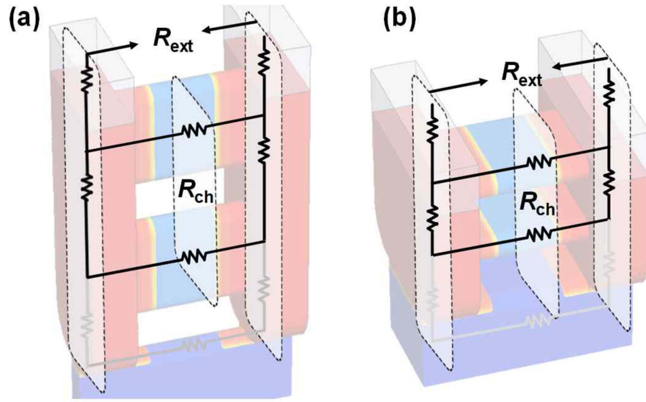

FIGURE 8. (a) Equivalent resistance circuits of the FNS and (b) the LNS device.

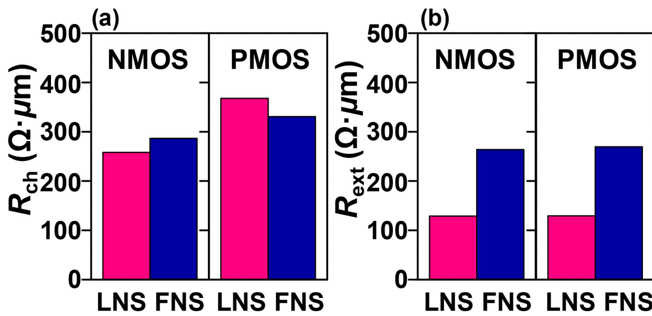

FIGURE 9. Bar chart for (a) channel resistance (R_{ch}) and (b) external resistance (R_{ext}) analysis. To compare and analyze the resistance components of FNS and LNS, each resistance component is extracted by extrapolation using over-drive linear current (I_{odlin}).

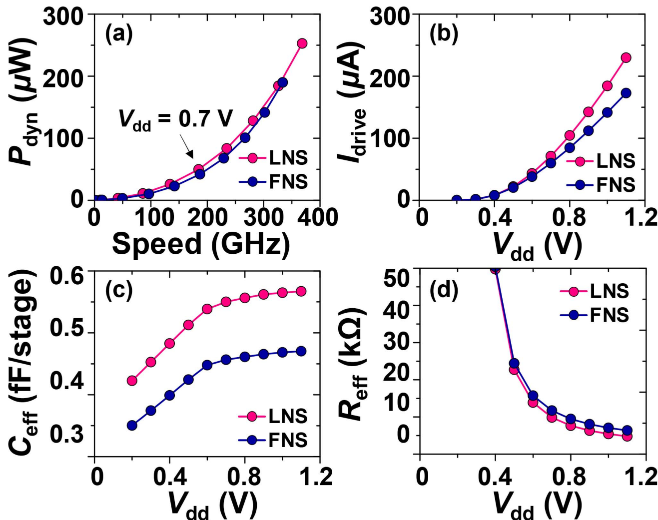

FIGURE 10. (a) Frequency – *P*dyn correlation plot of LNS and FNS. (b) *I*drive, (c) *C*eff, and (d) Inverter effective resistance (*R*eff) extracted by sweeping *V*dd from 0.2 V to 1.1 V.

and frequency (f), are analyzed because they are representative indexes for evaluating the AC performance of inverters.

$$\tau_{delay} = C_{eff} \times R_{eff} \tag{7}$$

$$P_{dynamic} = f \times C_{eff} \times V_{dd}^2 \tag{8}$$

For the accurate analysis of the device performance, V_{dd} is swept from 0.2 to 1.1 V and the device is evaluated with reasonable criteria in the correlation graph between P_{dyn} and frequency (namely, inverse of τ_{delay}). Fig. 10(a) demonstrates the P_{dyn} comparison with respect to the frequency between LNS and FNS. It is clearly seen that FNS has 19% P_{dyn} gain (9.4 μW) at the same frequency (187 GHz, FO1, V_{dd} = 0.7 V). In other words, the 8% gain of frequency (15.3 GHz) at the same P_{dyn} (50 μW, FO1, V_{dd} = 0.7 V) is achievable, meaning that FNS is suitable for low power operations. This can be understood by noticing that the C_{eff} of FNS is improved by 17% in all the V_{dd} range [Fig. 10(c)] although the inverter drive current (I_{drive}) becomes degraded with the V_{dd} increasing compared to LNS [Fig. 10(b)] due to the increase of the inverter resistance [Fig. 10(d)]. That is, the reduction of the C_{eff} overwhelms the I_{drvie} degradation and thereby the performance improvements are obtained. In addition, note that the R_{eff} and R_{ext} of FNS can be diminished without sacrificing C_{eff} gain by applying wrap-around-contact (WAC) [5].

Furthermore, the FO is added to consider inverter operations in complex circuits. It can be expected that the C_{eff} is increased by the number of C_{fo} because inverter FO is located between the input and output stages and the additional C_{fo} component serves as the capacitance component of the output node with $C_{gg(inv)}$ and $C_{gg(dep)}$ when one point of inverter oscillation is captured as follows.

$$C_{fo} = C_{gg_p(dep.)} + C_{gg_n(inv.)} \tag{9}$$

Fig. 11(a) shows that the C_{eff} difference between the LNS and the FNS becomes larger with the increasing number of FO. Also, as depicted in the frequency vs. P_{dyn} correlation with respect to the FO number [Fig. 11(b)], the P_{dyn} is decreased by 19% at the same frequency and the τ_{delay} is reduced by 8% at the same P_{dyn} even in the FO3 case. Thus, it is confirmed that the performance gain of FNS is still maintained despite of the addition of the FO, indicating the feasibility of FNS to the actual logic circuit.

In Table 2, the performance and electrical parameters of FNS are compared to those of LNS. It is clearly observed that FNS has the improved speed at same P_{dyn} and, in other words, the reduced P_{dyn} at same speed. Based on the comparisons, it is confirmed that the performance enhancement results from the capacitance reduction, and particularly the decrease in C_{side} is noticeable in both NMOS and PMOS.

IV. CONCLUSION

In this paper, FNS have been proposed for low power logic device applications because FNS can have the improved electrical characteristics than LNS although the process flow is highly compatible with those of FinFETs and LNSs. Through the TCAD device and circuit simulations, the device performance of FNS is rigorously investigated. As a result, it is found that the P_{dyn} at the same frequency (187 GHz) and

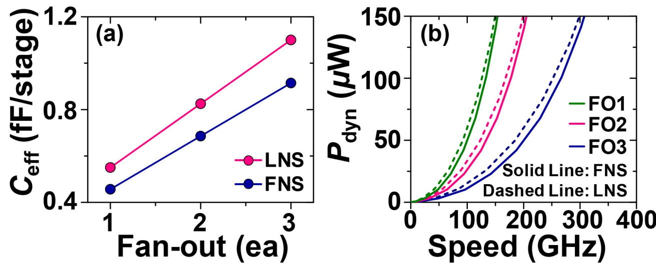

FIGURE 11. (a) FO effect on C_{eff} of LNS and FNS. (b) Frequency – P_{dyn} correlation plot with respect to the number of FO.

TABLE 2. Benchmark table for performance evaluation.

Parameters	Unit	LNS		FNS	
		NMOS	PMOS	NMOS	PMOS
Speed (at same P_{dyn})	GHz	92.3		99.9	
P_{dyn} (at same speed)	μW	49.8		40.5	
I_{eff} (at same I_{off})	µA/µm	320	245	255	225
V_{th}	V	0.232	0.253	0.237	0.247
C_{ov}	fF/μm	0.422	0.415	0.329	0.329
C_{gd}	fF/μm	0.408	0.401	0.322	0.322
C_{side}	fF/μm	0.116	0.115	0.027	0.026
C_{of}	fF/μm	0.117	0.117	0.159	0.158
C_{mol}	fF/μm	0.055	0.067	0.026	0.045
C_{do+if}	fF/μm	0.134	0.116	0.117	0.099
R_{ch}	Ω·μm	258	368	286	331
R_{ext}	Ω·μm	129	129	264	269
I_{off}	nA/μm	4.015	2.317	3.639	2.758

the τ_{delay} at the same P_{dyn} (50 μW) are reduced by 19% and 8% in the one-stage inverter, respectively. Even, the same amount of τ_{delay} reduction is achievable in the inverter with FO3.

To verify the origin of the performance improvements, the analysis on the resistance and capacitance components of LNS and the FNS is performed. It is clearly revealed that the R_{ext} is increased by the reduced S/D contact area and the extended floating fin height, and the C_{eff} is diminished due to the reduction of the C_{side}. Consequently, the τ_{delay} and the P_{dyn} are improved despite of the I_{eff} degradation because the C_{eff} reduction overwhelms the drivability degradation during the signal propagation through inverters.

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