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A Tall Gate Stem GaN HEMT With Improved Power Density and Efficiency at Ka-Band

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ABSTRACT In this letter, AlGaN/GaN HEMTs with tall-gate-stem structures were realized to improve the power performance of Ka-band devices, and a film thinning process is adopted in the fabrication process to reduce the parasitic capacitance caused by the thick silicon nitride film. According to the S-parameter measurement results, devices owning a tall-gate-stem structure and undergoing the film thinning process have higher cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) values with lower extracted parasitic capacitance. For the load-pull measurement result, the AlGaN/GaN HEMT with a tall gate stem has improved output power density (P_{out}) and power added efficiency (PAE) at Ka-band. The device with the elevated stem shows a steady-state current density of 883 mA/mm and a maximum transconductance of 323 mS/mm at 20 V bias, and it achieves f_T of 39.5 GHz, f_{max} of 112.9 GHz with the maximum PAE of 24.6% and the maximum P_{out} of 6.6 W/mm at 38 GHz.

INDEX TERMS AlGaN/GaN HEMT, tall-gate-stem structure, output power density, power added efficiency.

I. INTRODUCTION

GAN-Based high electron mobility transistors (HEMTs) have become popular microwave power devices in recent years. The GaN material has several remarkable properties, such as a wide bandgap of 3.4 eV, high breakdown electric field, high electron mobility, and high saturation electron drift velocity. These features enable GaN devices to provide high output power under high-frequency operation. With the development of fifth-generation communication (5G), which requires high-power devices for Ka-band, GaN material will be essential because it can operate at high frequency with excellent power performance [\[1\]](#page-6-0), [\[2\]](#page-6-1), [\[3\]](#page-6-2), [\[4\]](#page-6-3), [\[5\]](#page-6-4), [\[6\]](#page-6-5), [\[7\]](#page-6-6), [\[8\]](#page-6-7), [\[9\]](#page-6-8), [\[10\]](#page-6-9), [\[11\]](#page-6-10), [\[12\]](#page-6-11), [\[13\]](#page-6-12).

When operated at high frequency, device performances such as cut-off frequency (f_T) , maximum oscillation frequency (f_{max}) , output power density (P_{out}) , and poweradded efficiency (PAE) suffer from parasitic effects. The parasitic capacitance is mainly contributed by the gate-tosource capacitance (C_{gs}) and the gate-to-drain capacitance (C_{gd}) . To alleviate these effects, the tall-stem-gate structure is implemented in this study. Using simulations, it was found that reduction of C_{gs} and C_{gd} can be achieved by properly increasing the height of the gate stem [\[14\]](#page-6-13). The tall-stemgate structure increases the distance between the gate head and the channel, resulting in the reduction of the C_{gs} and C_{gd} due to the decrease of the head-to-channel capacitance.

The impact of height of gate stem on power performance has not been discussed in the literature; in this study, GaN HEMT devices with gate stem heights of 150 nm and 250 nm are fabricated and compared to investigate their difference in

FIGURE 1. Schematic of the parasitic capacitance of a *-***-gate AlGaN/GaN HEMT.**

FIGURE 2. Device structure and dimensions of the AlGaN/GaN HEMT. Lg is 100 nm, and Hstem values are 150 nm and 250 nm for group A and B respectively. Dgs and Dgmd are 800 nm. Lhead and Hhead are 350 nm.

power performance. Improved power gain, output power density, and efficiency of the device at Ka-band are observed in this study due to the adoption of the tall gate stem structure.

II. DEVICE DESIGN

As shown in Fig. [1,](#page-1-0) the Γ -gate structure of the AlGaN/GaN HEMT used in this study generates the head-to-channel capacitance (C_{hc}) and the stem-to-channel capacitance (C_{sc}) , which are parasitic capacitance contributing to C_{gs} and C_{gd} . According to [\[14\]](#page-6-13), the simulated C_{gs} and C_{gd} values of the elevated T-gate device were reduced because raising the stem height alleviates C_{hc} significantly with only a slight increase of C_{sc} . Similar to the T-gate device, the Γ -gate AlGaN/GaN HEMT with a higher head level will have a lower C_{gd} value; and modifying the gate architecture at the drain side will also influence the value of C_{gs} [\[15\]](#page-6-14). Therefore, for the contribution to C_{gs} , if the reduction of C_{hc} is more significant than the increase of C_{sc} , C_{gs} of the elevated Γ -gate device is expected to be reduced as well.

Based on the concept, two types of devices were designed, one with a 150nm-stem-height gate and the other with a 250nm-stem-height gate. The structure and dimensions of --gate AlGaN/GaN HEMTs in this study are shown in Fig. [2.](#page-1-1) With a higher gate stem, the device would have lower C_{gs} and C_{gd} values with better RF power performance.

On the other hand, different heights of gate stems are determined by the thickness of the first deposited silicon nitride (SiN) film in the fabrication process. Therefore, to minimize the parasitic capacitance difference caused by different thicknesses of the first deposited SiN film, a

TABLE 1. AlGan/Gan HEMTs in different groups.

FIGURE 3. Small-signal equivalent circuit model of the AlGaN/GaN HEMTs in this study.

film thinning process is adopted during the process. The film thinning process is also expected to improve the gain compression of devices during the load-pull measurement through the dispersion control. For the deposition of a SiN film, the 2-step PECVD was adopted. For the first step of the deposition, low-power plasma was used to form the first 50 nm of the SiN film thickness for better quality; for the second step of the deposition, the relatively high-power plasma was then used to accelerate the deposition rate till the target thickness. The SiN film formed by the relatively high-power plasma tends to have more defects and it leads to more significant dispersion [\[16\]](#page-6-15). The film thinning process removes the part formed by the relatively high-power plasma of the SiN film, and thus is expected to improve the dispersion characteristic. Therefore, an experiment on the 150nm-gate-stem-height devices with and without film thinning process is conducted to investigate its influence on RF power performance.

Overall, as shown in Table [1,](#page-1-2) 3 types of devices were prepared. One with a 150nm-stem-height gate and has undergone the film thinning process is labeled as group A, another with a 250nm-stem-height gate and has undergone the film thinning process is labeled as group B, and the other with a 150nm-stem-height gate and has not undergone the film thinning process is labeled as group C.

To investigate the relationship between device RF characteristics and parasitic capacitance, a small-signal equivalent circuit model of an AlGaN/GaN HEMT with parasitic ele-ments is provided in Fig. [3.](#page-1-3) Where C_{pgi} , C_{gdi} , C_{gdi} stand for the inter-electrode and crossover capacitance between gate, source, and drain. Then, the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) are introduced to explain the relationship between device RF characteristics and parasitic elements of the AlGaN/GaN HEMTs in this

FIGURE 4. Epitaxial layers of the AlGaN/GaN HEMT.

study. Equation [\(1\)](#page-2-0) and [\(2\)](#page-2-0) shows the general forms of f_T and f_{max} formulas:

$$
f_T = \frac{g_m/2\pi}{(C_{gs} + C_{gd}) \times [1 + (R_s + R_d)g_o] + g_m C_{gd}(R_s + R_d)}
$$

\n
$$
\approx \frac{g_m}{2\pi (C_{gs} + C_{gd})}
$$
 (1)

$$
f_{\text{max}} = \frac{f_T}{2\sqrt{g_o(R_g + R_s) + 2f_T C_{gd}R_g}}
$$
(2)

where R_s is the source resistance, R_d is the drain resistance, R_g is the gate resistance, and g_0 is the output conductance [\[17\]](#page-6-16), [\[18\]](#page-6-17). Based on the formulas, it can be observed that f_{T} and f_{max} have a negative correlation with parasitic capacitance C_{gs} and C_{gd} , which is roughly inversely proportional to $C_{gs} + C_{gd}$. Therefore, the reduction in C_{gs} and C_{gd} improves f_T and f_{max} significantly. Because the definition of fmax is the frequency that Mason's unilateral gain (G_U) becomes unity, the reduction of parasitic capacitance not only improves the RF characteristics but also benefits the power gain characteristic.

III. DEVICE FABRICATION

From bottom to top, the AlGaN/GaN HEMTs on SiC were composed of the following epitaxial layers: GaN buffer layer, GaN channel layer, AlN spacer layer, and AlGaN barrier layer as shown in Fig. [4.](#page-2-1)

The fabrication process for devices with film thinning can be divided into four main parts: Ohmic contact formation, isolation, gate formation, and metallization. For the Ohmic contact formation, the Ti/Al/Ni/Au Ohmic metal stack was deposited by the E-gun evaporator, followed by RTA at 835 ℃ in nitrogen ambient. Device isolation was performed using boron ion implantation. For the gate formation, the first SiN film was deposited using PECVD for device passivation, and its thickness is equal to the height of the gate stem. The first SiN film thickness of 150 nm and 250 nm were prepared for devices in group A and group B, respectively. Afterward, E-beam lithography was conducted twice to perform gate shift technology as shown in Fig. [5.](#page-2-2) The first E-beam lithography defined the region to be etched of the first SiN film, and the second E-beam lithography defined the area for gate metal deposition. The pattern of the second E-beam lithography was slightly shifted from the pattern of the first E-beam lithography, and the overlap equals the gate length, which is 100 nm. For the two-step E-beam lithography method, the as-deposited SiN film provides steady support for the tall stem structure, and the height of gate

FIGURE 5. Gate shift technology of the *-***-gate AlGaN/GaN HEMT.**

FIGURE 6. SiN film thinning process of the Γ **-gate AlGaN/GaN HEMT.**

stem can be accurately determined by the thickness control of the SiN film. After two steps of E-beam lithography, a gate metal stack of Ni/Au was deposited by the E-gun evaporator. Afterward, the device was covered with the second SiN film of 100 nm to protect the deposited gate metal and fill the etching vacancy left by the gate shift process. The overall SiN thickness of the 250nm-gate-stem-height device so far is 100 nm thicker than the 150nm-gate-stem-height device. A film thinning process, as shown in Fig. [6,](#page-2-3) was applied not only to minimize the parasitic capacitance difference caused by different first deposited SiN film thicknesses (150/250 nm) but also to improve the dispersion control for the devices in groups A and B. During the film thinning process, the deposited SiN film were directly etched by ICP-RIE, and the thickness was reduced to 50 nm. The deposition of second SiN film before film thinning is necessary; otherwise, the etching vacancy will lead to the collapse of the gate structure during directly etching. After the film thinning process, the devices in groups A and B were passivated by the third SiN film of 100 nm to protect the gate metal. That is, the devices in group C did not undergone the film thinning process and

FIGURE 7. (a) IDVG and (b) IDVD characteristics of the 4×25 um 150nm-gate-stem device with SiN film thinning process.

the deposition of the third SiN film. Finally, for the metallization, the via hole opening of the passivation film was performed by ICP-RIE and then thick Au metallization of 2 um was deposited.

IV. RESULTS AND DISCUSSION

The devices with different heights of gate stem (150/250 nm for group A/B) and devices with or without the film thinning process (group A and C) were fabricated and evaluated in this study. The evaluation of the device includes the DC characteristics, the S-parameters, and the RF power characteristics.

A. IMPACT OF SIN FILM THINNING ON ALGAN/GAN HEMTS

To investigate the impact of SiN film thinning on performance, devices with thinned (group A) and un-thinned (group C) first SiN film are compared. The overall thickness of SiN films for devices in groups A and C are 150 nm and 250 nm, respectively. The gate width of the device is 4×25 um and the height of the gate stem is 150 nm for each group.

The DC characteristics of the devices in group A and C are shown in Fig. [7](#page-3-0) and Fig. [8.](#page-3-1) The IDVG measurements were conducted under 20V drain bias voltage (V_{DS}) as shown in Fig. [7](#page-3-0) (a) and Fig. [8](#page-3-1) (a). For the device in group A, the steady-state current density (I_{dss}) was 863 mA/mm and

FIGURE 8. (a) IDVG and (b) IDVD characteristics of the 4×25 um 150nm-gate-stem device without SiN film thinning process.

the maximum transconductance $(g_{m,max})$ was 317 mS/mm. For the device in group C, the I_{dss} was 888 mA/mm and the $g_{m,max}$ was 322 mS/mm. The IDVD measurements were conducted under different gate bias voltages (V_{GS}) from 0 V to -5 V as shown in Fig. [7](#page-3-0) (b) and Fig. [8](#page-3-1) (b). Based on the measurement of DC characteristics, the SiN film thinning process does not cause obvious difference in DC performance.

The S-parameter measurement results of the devices in groups A and C with 4×25 um gate width are shown in Fig. [9](#page-4-0) (a) and (b). The bias condition is $V_{DS} = 20V$ and $V_{GS} = -2.7V$. The values of f_T can be obtained from the measured $|H21|$ gain results and the values of f_{max} can be obtained from the measured MSG/MAG results. For the device in group A, f_T was 32.7 GHz and f_{max} was 92.9 GHz; for the device in group C, f_T was 29.6 GHz and f_{max} was 87.6 GHz. Both f_T and f_{max} of the device in group A are higher than in group C. According to the results of S-parameter measurements, the values of the parasitic elements of the devices can be extracted referring to the approach proposed in $[19]$. The intrinsic elements C_{gs} and C_{gd} of devices in groups A and C are extracted under bias condition of $V_{DS} = 20V$ and $V_{GS} = -2.7V$. The values of the extracted Rg, Cgs and *C*gd of the AlGaN/GaN HEMTs in this study are listed in Table [2.](#page-4-1) The device in group A has a C_{gs} value of 78.2 fF and a C_{gd} value of 12.1 fF, while the

FIGURE 9. Measured |H21| and MSG/MAG of 150nm-gate-stem AlGaN/GaN devices (a) with and (b) without SiN film thinning process.

TABLE 2. Estimated maximum oscillation frequency and Rg, Cgs, and Cgd values of AlGaN/GaN HEMTs with 4x25 gate width in this study.

Group	\mathbf{I}_{max}	C_{gs}	C_{gd}	\mathbf{K}_{σ}
	92.9 (GHz)	78.2 (fF)	12.1 (fF)	4.2 (ohm)
В	112.9 (GHz)	59.7 (fF)	8.7(fF)	6.2 (ohm)
C	87.6 (GHz)	82.3 (fF)	13.7(fF)	4.0 (ohm)

device in group C has a C_{gs} value of 82.3 fF and a C_{gd} value of 13.7 fF. The film thinning process slightly reduces the parasitic capacitance of the AlGaN/GaN HEMTs. Since the film thinning process does not change the gate structure, the gate resistance of devices in groups A and C are similar. The extracted results are consistent with the formulas of f_T and f_{max} , which indicate that higher f_{T} and f_{max} values are due to lower parasitic capacitance. For the S-parameter result of devices in groups A and C, it can be concluded that the reduction of 100 nm in SiN film thickness causes the decrease in the parasitic capacitance, and therefore the RF performance is improved. This phenomenon is expected to be more significant on 250nm-gate-stem devices because the SiN thickness difference will be 200 nm between thinned and un-thinned devices.

The 38 GHz load-pull measurement results of devices in groups A and C with 4×25 um gate width are compared in Fig. [10.](#page-4-2) During the measurement, V_{GS} was set at class A and

FIGURE 10. Power performance at 38 GHz for 150nm-gate-stem AlGaN/GaN HEMTs with and without SiN film thinning in this study.

 V_{DS} was biased at 28 V for each device. The impedances of both the source port and the load port were matched for the maximum output power density. The device in group A achieved the maximum output power density $(P_{\text{out,max}})$ of 4.7 W/mm, the maximum power-added efficiency (PAE_{max}) of 14.7%, and the linear gain of 5.8 dB; the device in group C achieved $P_{\text{out,max}}$ of 4.1 W/mm, PAE_{max} of 10.2%, and the linear gain of 5.6 dB. Based on the load-pull measurement results, a more severe gain compression is found for the device in group C due to worse dispersion control. For device in group A, the film thinning process not only reduces the parasitic resistance, but also significantly improves the dispersion characteristic. Therefore, the SiN film thinning process is necessary to further improve the output power density and the power-added efficiency of the device; otherwise, the influence of dielectric thickness will be more significant on 250nm-gate-stem device.

B. ALGAN/GAN HEMTS WITH DIFFERENT HEIGHTS OF GATE STEM

To investigate the impact of height of gate stem, devices with gate stem height of 150 nm (group A) and 250 nm (group B) are compared. For each group, the gate width of device is 4×25 um and the thickness of first SiN film is thinned to 50 nm.

The DC characteristics of the devices in groups A and B are shown in Fig. [7](#page-3-0) and Fig. [11.](#page-5-0) The IDVG measurements were conducted under V_{DS} of 20 V as shown in Fig. [7](#page-3-0) (a) and Fig. [11](#page-5-0) (a). For the device in group A, the I_{dss} was 863 mA/mm and the $g_{m,max}$ was 317 mS/mm. For the device in group B, the I_{dss} was 883 mA/mm and the gm,max was 323 mS/mm. The IDVD measurements were conducted under different V_{GS} from 0 V to -5 V as shown in Fig. [7](#page-3-0) (b) and Fig. [11](#page-5-0) (b). Based on the measurement of DC characteristics, different gate stem heights in this study have only a minor impact on the DC performances of the devices.

FIGURE 11. (a) IDVG and (b) IDVD characteristics of the 4×25 um 250nm-gate-stem device with SiN film thinning process.

FIGURE 12. Measured |H21| and MSG/MAG of 250nm-gate-stem AlGaN/GaN device with SiN film thinning process.

The S-parameter measurement results of the devices in groups A and B with 4×25 um gate width are shown in Fig. [9](#page-4-0) (a) and Fig. [12.](#page-5-1) The bias condition is $V_{DS} = 20V$ and $V_{GS} = -2.7V$. For the device in group A, f_T was 32.7 GHz and fmax was 92.9 GHz; for the device in group B, f_T was 39.5 GHz and f_{max} was 112.9 GHz. Based on the results, both f_T and f_{max} of the device in group B are much improved. The intrinsic elements C_{gs} and C_{gd} of the device in group B are extracted under bias condition of V_{DS} = 20V and $V_{GS} = -2.7V$ as well. The device in group A has

FIGURE 13. Power performance at 38 GHz for 150nm- and 250nm-gate-stem AlGaN/GaN HEMTs with SiN film thinning in this study.

TABLE 3. Device power performance comparison at Ka-band.

Device	Freq.	$\mathbf{V_{DS}}$	$P_{out}(a) PAE_{max}$	PAE _{max}	$P_{\text{out,max}}$
Tall-Gate-Stem Device in this work	38GHz	28V	4.9W/mm	24.6%	6.6W/mm
[20]	30GHz	30V		38.0%	6.4W/mm
[21]	40GHz	15V	2.0W/mm	13.0%	
[22]	30GHz	20V	5.0W/mm	39.0%	6.0W/mm
[23]	40GHz	25V	2.7W/mm	12.5%	
[24]	40GHz	15V	2.2W/mm	18.0%	2.5W/mm
[25]	40GHz	20V	1.8W/mm	18.5%	2.1W/mm
[26]	40GHz	15V		20.1%	3.3W/mm
$[27]$	30GHz	10V	2.0W/mm	72.0%	
[28]	30GHz	15V	3.0W/mm	40.0%	5.0W/mm
[29]	30GHz	20V	3.5W/mm	39.0%	
[30]	30GHz	15V		47.0%	5.8W/mm

a C_{gs} value of 78.2 fF and a C_{gd} value of 12.1 fF, while the device in group B has a C_{gs} value of 59.7 fF and a C_{gd} value of 8.7 fF. This proves that appropriately raising the gate head can efficiently improve the parasitic capacitance. Although the tall-gate-stem structure causes an increase in R_g value, it is still worth applying the tall-gate-stem structure because the reduction in C_{gs} and C_{gd} is significant.

The 38 GHz load-pull measurement results of devices in group A and B with 4×25 um gate width are compared in Fig. 13 . During the measurement, V_{GS} was set at class A and V_{DS} was biased at 28 V for each device as well. Also, the impedances of both the source port and the load port were matched for the maximum output power density. The device in group A achieved $P_{\text{out,max}}$ of 4.7 W/mm, PAE_{max} of 14.7%, and the linear gain of 5.8 dB; the device in group B achieved $P_{\text{out,max}}$ of 6.6 W/mm, PAE_{max} of 24.6%, and the linear gain of 8.0 dB. It can be observed that the tall-gate-stem structure significantly improves P_{out} and PAE of the device at 38 GHz. Based on the load-pull measurement results and the extracted C_{gs} and C_{gd} values from

the S-parameter results, it is shown that the tall-gate-stem AlGaN/GaN HEMT with reduced parasitic capacitance not only has better f_T , f_{max} , and power gain characteristic, but its output power and power-added efficiency are also enhanced.

Table [3](#page-5-3) compares the device performances in this study with the reported data of the Ka-band device in the literature. It shows that the RF power performance of AlGaN/GaN HEMT with a tall gate stem is comparable with the data of the reported Ka-band devices in the literature.

V. CONCLUSION

The increase of the head-to-channel distance for a GaN HEMT device was realized by increasing the gate stem height. This leads to lower head-to-channel capacitance (C_{hc}) , which is included in the gate-to-source capacitance (C_{gs}) and the gate-to-drain capacitance (C_{gd}) . According to the experimental results, raising the gate stem mitigates the parasitic capacitance and enhances the RF power performance of the device under high-frequency operation. Based on the S-parameter measurement results, the device with a gate stem of 250 nm can achieve f_T of 39.5 GHz and f_{max} of 112.9 GHz, which are higher than the device with a gate stem of 150 nm. For the AlGaN/GaN HEMT with gate stem height of 250 nm, the load-pull measurement results at 38 GHz showed the maximum output power density ($P_{\text{out,max}}$) of 6.6 W/mm, the maximum power-added efficiency (PAE_{max}) of 24.6%, and the linear gain of 8.0 dB. The power performance of the 250nm-gate-stem device is much better than the 150nm-gate-stem device. Again, the results indicate that raising the gate head can alleviate the parasitic effects of C_{gs} and C_{gd} . Furthermore, the device demonstrates the RF power performance comparable to the data reported in the literature.

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