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Overview on Latch-Up Prevention in CMOS Integrated Circuits by Circuit Solutions

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ABSTRACT In CMOS chips, the wider layout rules were traditionally applied to overcome latch-up issues. However, the chip area with wider layout rules was often enlarged, and in turn the chip cost was also increased. To effectively improve latch-up immunity without enlarging the chip area, circuit methods were therefore invented. An overview on circuit methodology used to prevent latch-up issues in CMOS integrated circuits (ICs) is presented in this article. The circuit solutions, including reducing the I/O pad trigger current, sensing the trigger current to control the power supply, and restarting the power supply through an MOS switch to shut off the latch-up current, are overviewed.

INDEX TERMS Latch-up, latch-up prevention, silicon-controlled rectifier (SCR), guard ring, active guard ring, voltage regulator, over-current detector.

I. INTRODUCTION

The parasitic silicon-controlled-rectifier (SCR) structure in CMOS integrated circuits had been reported to cause serious latch-up failures [1], [2], [3], [4]. As shown in Fig. 1(a), the SCR structure is a 2-terminal device with a four-layer p-n-p-n path, which consists of two bipolar devices (Q_{PNP} and Q_{NPN}). The equivalent circuit of the latch-up (SCR) path between the anode and cathode is shown in Fig. 1(b) [5], [6]. Since the collector current of Q_{NPN} is also the base current of Q_{PNP}, if the trigger current Itn flows into the base of Q_{NPN} and causes Q_{NPN} to enter the amplification working zone, Q_{PNP} will further amplify the collector current of Q_{NPN}, which generates a positive-feedback regenerative mechanism to establish the latch-up state. Similarly, when the trigger current Itp flows into the base of Q_{PNP}, the latch-up path will be triggered into the latch-up state. When a latch-up path occurs, regardless of whether the trigger current Itn/Itp was removed, the latch-up path does not stop until the chip burns out. Thus, IC engineers had been advised to be mindful of latch-up failures during circuit design and chip layout.

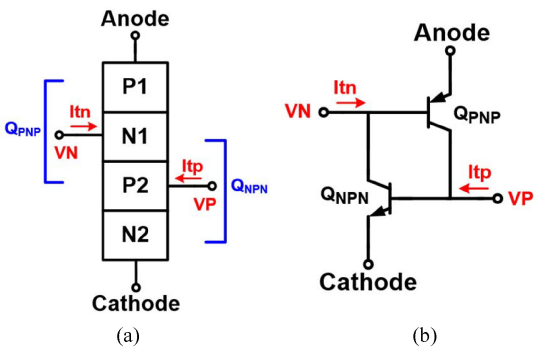

FIGURE 1. (a) Four-layer p-n-p-n structure, and (b) the equivalent circuit of the latch-up (SCR) path from anode to cathode.

The typical parasitic p-n-p-n path (P+/N-well/P-well/N+) in the layout of a CMOS inverter drawn with well taps (pickups) is shown in Fig. 2(a). With the source (P+ diffusion) of PMOS in an N-well connected to VDD, and the source (N+ diffusion) of NMOS in the p-well/p-substrate connected to VSS (GND), the p-n-p-n path forms the parasitic latch-up path from VDD to VSS, which is shown in Fig. 2(b). Moreover, the cross-sectional view of the parasitic p-n-p-n path inside a CMOS inverter and the equivalent circuit that causes latch-up issues are shown in Figs. 3(a) and 3(b), respectively. The typical I–V characteristic of the

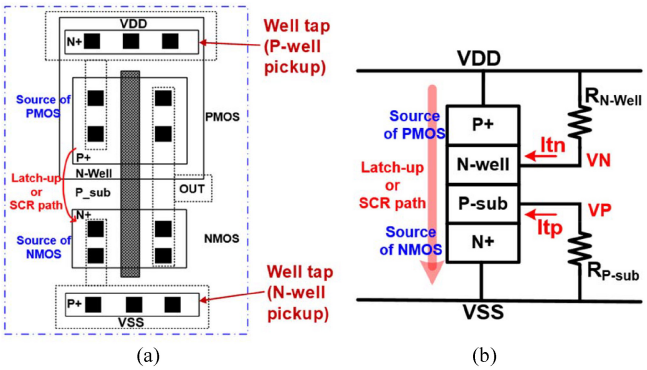

FIGURE 2. (a) Typical layout top view of CMOS inverter with well taps (pickups), and (b) the parasitic latch-up path in the CMOS inverter.

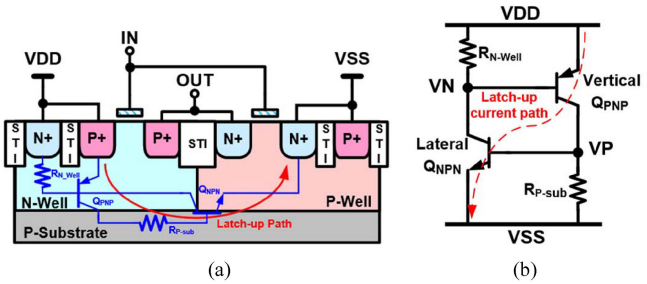

FIGURE 3. (a) Cross-sectional view of CMOS inverter, and (b) the equivalent circuit of the latch-up path from VDD to VSS.

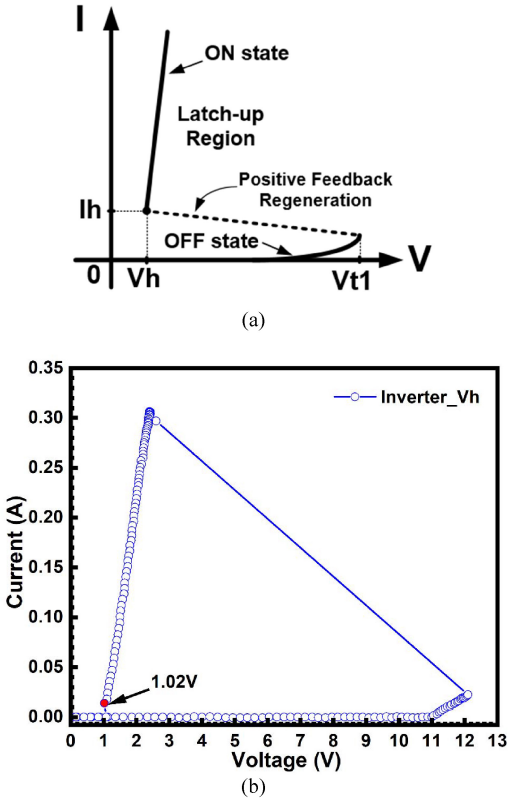

FIGURE 4. (a) The illustrated I-V characteristics of the parasitic latch-up path in a CMOS technology. (b) The measured DC I-V characteristics of the parasitic latch-up path in a CMOS inverter cell drawn with foundry's design rules and pickups, fabricated in a 0.18-μm bulk CMOS process.

parasitic latch-up path is illustrated in Fig. 4(a). The measured DC I-V characteristics of the parasitic latch-up path in a CMOS inverter cell drawn with foundry's design rules and pickups, fabricated in a 0.18-μm bulk CMOS process, is shown in Fig. 4(b). The holding voltage is only 1.02V measured at room temperature, even if the pickups (P+ diffusion in P-well, N+ diffusion in N-well) had been drawn inside the layout area the CMOS inverter. Once the parasitic latch-up path is triggered, the vertical Q_{PNP} and lateral Q_{NPN} transistors are kept on due to the positive-feedback regenerative mechanism. Typically, the SCR has a lower holding voltage (Vh) of ~1V in the bulk CMOS technologies, which was often smaller than the VDD of internal circuits. The triggered-on latch-up path will conduct a huge abnormal current flowing from the power supply (VDD) to GND, which often burns out the chip.

To verify the latch-up immunity of CMOS ICs, the JEDEC Standard for *IC Latch-Up Test* [7] has been widely used in the IC industry. The I/O cell under latch-up test with the applied positive or negative trigger current is illustrated in Fig. 5(a). An overshooting or undershooting trigger current of 100 mA is applied to each I/O pin to seek whether any latch-up event occurs in the chip, or not. In addition, the voltage fast transient on the VDD power supplies may induce latch-up occurrence in CMOS ICs. The latch-up test with the voltage-transient trigger applied to the VDD pins is illustrated in Fig. 5(b), where the overshooting peak voltage (Vp) is often 1.5 times of VDD voltage level. With the trigger current applied to the I/O pins, or the transient voltage applied to the power pins, the latch-up events may occur in the region of I/O cells, or even in the region of internal circuits [8], [9], [10], [11], [12], [13], [14], [15], [16].

To increase latch-up immunity of CMOS ICs, the typical layout skills include increasing the anode and cathode spacing, improving the width of the guard rings, and adjusting the spacing between guard rings. Also, some process optimizations in CMOS technology had been implemented [17], [18], [19], [20], [21], [22], which include trench isolation, SOI (Silicon on Insulator), retrograded well, and epitaxy (Epi) wafer, etc. Additional passive guard rings had also been applied [23], [24], [25], [26], [27]. However, even if high latch-up immunity can be achieved by implementing the aforementioned methods, they may increase the manufacturing cost or chip area. Therefore, to look for a cost-efficient solution for improving latch-up immunity has been strongly requested by the cost-sensitive consumer IC products. IC designers were required to save the fabrication cost without utilizing extra mask layers and/or process steps, to reduce the layout spacing between the PMOS and NMOS, and even to reduce the width of guard rings. Thus, some

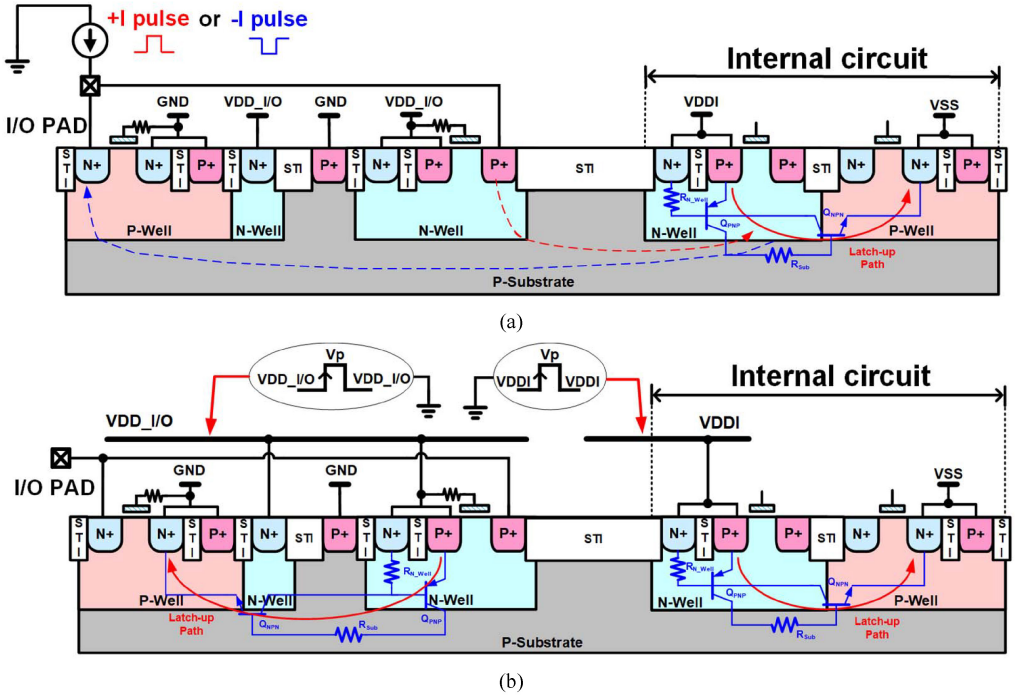

FIGURE 5. Latch-up test for a CMOS IC with (a) the overshooting or undershooting trigger current at the I/O pad, and (b) the voltage-transient trigger at the VDD pad.

circuit solutions are invented to effectively improve latch-up immunity of CMOS ICs, without enlarging the chip layout.

Without additional process modification, the passive guard rings in layout placement are universally applied for latch-up preventions. The devices located at the I/O pads must be surrounded by double guard rings, as specified by the design rules of foundry [27], to overcome the latch-up issues at the I/O pads. Thus, the latch-up event would not occur in the IO cells, when the I/O cell layout has been drawn with the suitable guard rings. However, in order to save layout area, the devices of the internal circuits would not be surrounded by guard rings. Only some pickups (P+ diffusion in P-well, N+ diffusion in N-well) are drawn inside the layout area of internal circuits to provide the correct biases to the P-well and N-well. Therefore, the internal circuits, with no guard rings surrounding, are still sensitive to latch-up issues. As shown in Fig. 5(a), the P+ drain/N-well (N+ drain/P-well) junction in the I/O PMOS (NMOS) device is forward-biased to conduct the positive (negative) trigger current into the substrate. Hence, the passive guard ring may not completely absorb the latch-up trigger current. Since a part of the trigger current is injected into the p-type substrate and flows towards the internal circuit blocks, the parasitic p-n-p-n path of the internal circuits can be fired to cause latch-up event [27]. As a result, the circuit methods of active guard ring were therefore reported to improve the latch-up immunity of CMOS ICs [28], [29], [30].

In this article, the active guard ring to improve latch-up immunity by circuit methodology is first reviewed in Section II. In Section III, a novel auto-detector circuit to sense the trigger current injecting from the I/O cells, and then to stop latch-up current in the internal circuits for latch-up prevention, is presented [31]. Moreover, TLU (transient-induced latch-up) is more easy to cause the latch-up occurrence located inside the internal circuit blocks of CMOS ICs [11], [12], [13], [14], [15], [16]. Thus, the power supply restart method with switching control circuit is used to interrupt the latch-up current path from the power line to the internal circuit blocks [32], [33], [34], [35], [36]. The power supply restart to stop the latch-up current by MOS switches is reviewed in Section IV. Comparisons among the circuit solutions to improve latch-up immunity are discussed in Section V, and an example of application with the auto-detector circuit in a digital IC is given in Section VI. Finally, a conclusion is given in Section VII.

II. ACTIVE GUARD RING

For the traditional latch-up prevention on the I/O cell with guard rings, the guard rings are drawn to fully surround the I/O or ESD (electrostatic discharge) devices in layout. Some design rules to specify the widths and spacings of guard rings were often given by the foundries. In addition, the spacing from the I/O cells to the blocks of internal circuits must be drawn wider ($\sim$ 50 μm, or even more) in layout to avoid the latch-up event occurrence in the internal circuits due to the trigger current applied to the I/O pads [27]. If the specification of latch-up immunity was requested higher, the aforementioned widths and spacings must be drawn further wider to result in a bigger chip layout. Thus, the concept

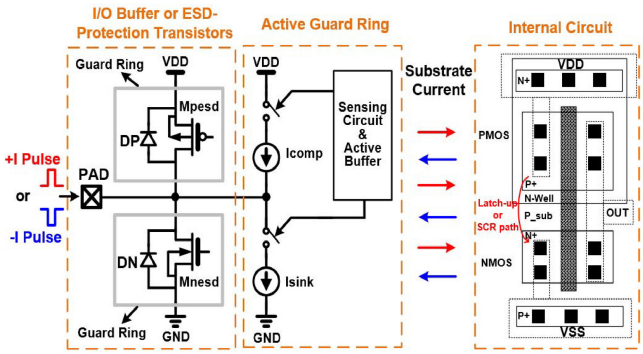

FIGURE 6. Concept of "active guard ring" designed to reduce the current injecting to the internal circuits during latch-up I-tests.

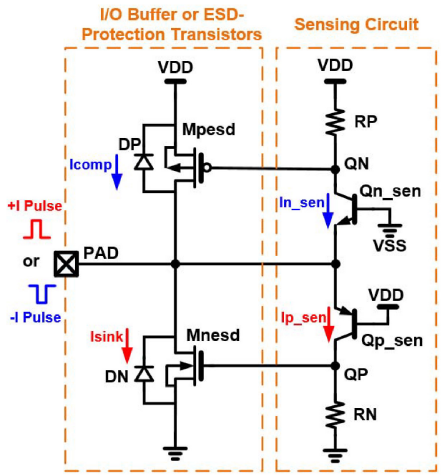

FIGURE 7. Circuit structure of the active guard ring implemented with BJT junctions [29].

of "active guard ring" realized by circuit methodology to effectively improve latch-up immunity without enlarging the layout spacings was reported [28], [29], [30].

The concept of "active guard ring" is illustrated in Fig. 6, where the sensing circuit is used to detect the current injecting from the I/O or ESD devices during the latch-up I-test with positive or negative trigger currents applied at the I/O pad. Then, some compensation currents (Isink or Icomp) are generated to "neutralize" the trigger current that applied to the I/O pad. Finally, the current injecting from the I/O or ESD devices toward the internal circuits can be dramatically reduced to avoid the latch-up occurrence in the internal circuits. By using such a circuit solution of "active guard ring", the latch-up immunity against latch-up I-test with trigger currents applied at the I/O pad can be significantly improved, without enlarging the layout spacing between the I/O cells and the internal circuits.

A. ACTIVE GUARD RING WITH BJT JUNCTION [29]

In Fig. 7, the circuit structure of the active guard ring is implemented by the additional junctions of bipolar junction transistors (BJTs). The active guard ring is composed of additional junctions of BJTs (Qn_sen and Qp_sen), a sensing circuit block, and two large-dimensional ESD protection transistors (Mpesd and Mnesd). The Qn_sen and Qp_sen are used to sense and monitor latch-up trigger current levels. The base terminal of Qn_sen is connected to VSS, the base terminal of Qp_sen is connected to VDD, and the emitter terminals of these two BJTs are connected to the I/O pad. The gate terminal of Mnesd is connected to the collector of Qp_sen, which is also connected to ground via a poly resistor RN. The gate terminal Mpesd is connected to the collector of Qn_sen, which is also connected to VDD via a poly resistor RP. During the normal circuit operating condition, the ESD protection transistors (Mpesd and Mnesd) are kept in the off state.

When a negative trigger current is applied at the I/O pad during the latch-up I-test, the Qn_sen detects the latch-up current perturbations and then pulls low the gate of the Mpesd. Qn_sen can be turned on and produce a sensing current (In_sen). When In_sen is sufficient to pull down the gate terminal (QN) of Mpesd, quite a large amount of compensating current (Icomp) can be produced from VDD to the I/O pad. So, with the source-to-drain current of Mpesd (Icomp) increased, the negative trigger current applied at the I/O pad can be neutralized. Thus, the substrate perturbation current from the I/O or ESD devices flowing toward the internal circuits can be decreased during the latch-up negative I-test.

On the contrary, when a positive trigger current is applied from an external source during the latch-up I-test, the pad voltage is pulled over the supply voltage VDD, and Qp_sen can be turned on to produce a sensing current (Ip_sen). When Ip_sen is sufficient to pull up the gate terminal (QP) of Mnesd, quite a large amount of extra sink current (Isink) can be produced by the Mnesd of large device dimension to neutralize the positive trigger current applied at the I/O pad. Thus, the latch-up immunity of the internal circuits against the latch-up I-test applied at the I/O pad can be significantly improved. The effectiveness of such a circuit implementation of active guard ring has been successfully verified in the silicon chip [29].

B. ACTIVE GUARD RING WITH ADDITIONAL MOS [30]

The circuit structure of active guard ring implemented with additional MOS transistors is shown in Fig. 8, which includes a sensing circuit block, two large-dimensional ESD protection transistors (Mpesd and Mnesd), and two resistors (RP and RN) in the sensing circuit. Under normal circuit operation, the gate voltage (VGP) of PMOS (MPS) is biased to VDD through RP, and the gate voltage (VGN) of NMOS (MNS) is biased to ground through RN. So, the ESD protection transistors (Mpesd and Mnesd), with VGP voltage level at VDD and VGN voltage level at ground, are kept in the off state.

Under the latch-up I-test with the positive trigger current applied to the I/O pad, the pad voltage (Vpad) will be raised higher than VDD. When the Vpad is larger than the gate

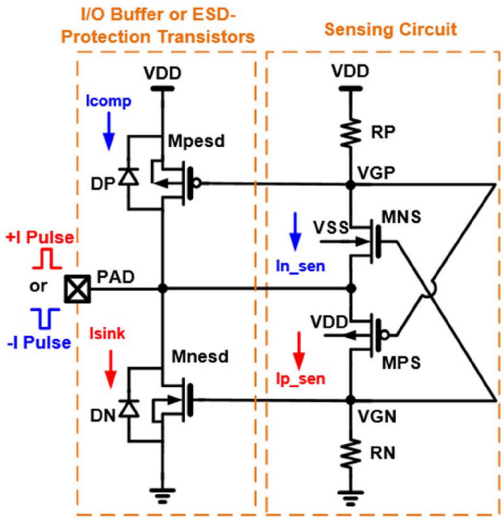

FIGURE 8. Circuit structure of active guard ring implemented with additional MOS transistors [30].

voltage (VGP) of MPS over a threshold voltage, MPS will be turned on. As a result, the gate voltage (VGN) of Mnsed will be pulled up by the channel current (Ip_sen) of MPS, and the large-dimensional Mnsed will be turned on to conduct the positive trigger current from the I/O pad to VSS. Thus, the latch-up risk is improved by injecting less current into the substrate.

Under the latch-up I-test with the negative trigger current applied to the I/O pad, Vpad will be pulled down to a low voltage level below VSS. The MNS will be turned on, once the Vpad is lower below a threshold voltage of VGN. The gate voltage (VGP) of Mpsed will be pulled down by the channel current (In_sen) of MNS. As a result, the large-dimensional Mpesd is turned on to conduct current from VDD to the I/O pad that compensates the negative trigger current applied at the I/O pad. Therefore, the latch-up trigger current injecting into the p-substrate toward the internal circuits can be significantly reduced, and the overall latch-up immunity can be effectively strengthened. The effectiveness of such a circuit implementation of active guard ring with additional MOS transistors has been already proven in the silicon chip [30].

III. AUTO-DETECTOR CIRCUIT TO STOP LATCH-UP

The concept of an auto-detector circuit is to sense the trigger current from the I/O pad to control the power supply [31]. Under the latch-up I-test, the latch-up trigger current injecting toward the internal circuits can be detected by adding a hole/electron detector between the I/O cells and the internal circuits. The output of the auto-detector circuit is utilized to turn off the LDO (low dropout regulator), which provides the power supply to the internal circuits. Thus, the latch-up occurrence in the internal circuits can be entirely stopped to prevent burned-out failures inside the chip.

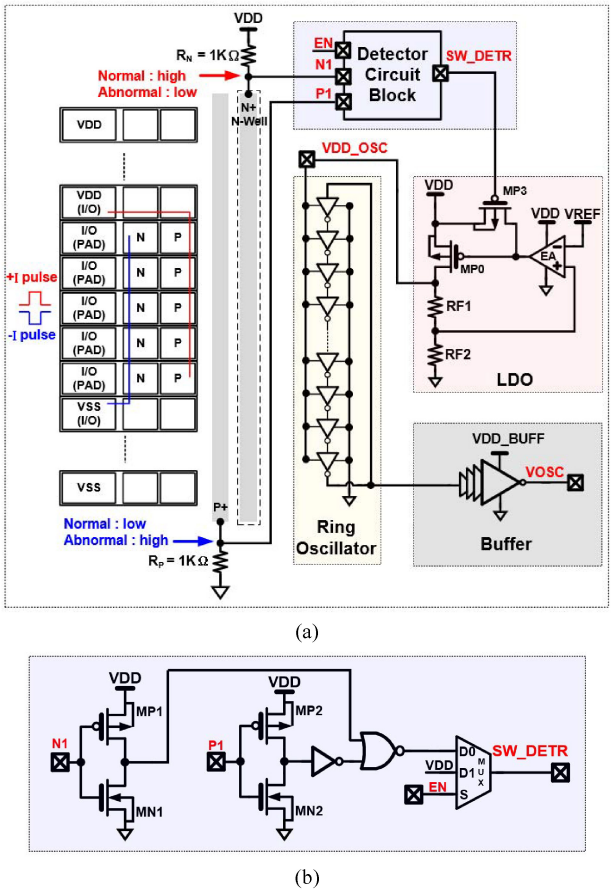

FIGURE 9. (a) The function block diagram of the auto-detector circuit to stop the latch-up current, and (b) the control logic in the detector circuit block [31].

The auto-detector circuit to stop the latch-up current for latch-up prevention is shown in Fig. 9(a). To detect the injecting holes (electrons) when a positive (negative) trigger current is applied to the I/O pad during the latch-up I-test, a long strip of P+ diffusion (N+/ N-well layer) is inserted between the I/O cells and the internal circuit blocks (accomplished by a ring oscillator). The signal at the P1 node is the output of the hole detector, which was constructed using the P+ diffusion and connected to VSS (GND) with a poly resistor R_P of 1 kΩ. The signal at the N1 node is the output of the electron detector, which was made by the N+ diffusion in the N-well and connected to VDD through a poly resistor R_N of 1 kΩ. The P1 and N1 signals are sent to the detector circuit block using the logic gates depicted in Fig. 9(b). The output signal of the detector circuit block (SW_DETR) is used to control the gate of a PMOS transistor (MP3) in the LDO circuit that provides the power supply (VDD_OSC) to the internal circuits (ring oscillators). To control the gate voltage of MP3 (SW_DETR), two inverters (MP1, MP2, MN1, and MN2) are used to detect the logic signals at nodes N1 and P1. The logic gate NOR is used to control the logic states N1 and P1, and the EN of MUX is used to select whether the auto-detector circuit is enabled

or not. To fully avoid latch-up issues between PMOS and NMOS in these circuit blocks, all of the devices utilized in the detector circuit and LDO are well surrounded by guard rings in the layout.

Under normal circuit operation conditions (no latch-up trigger current applied at the I/O pad), since the resistor R_P (R_N) is connected to GND (VDD), the voltage at node P1 (N1) is kept at GND (VDD). Thus, the SW_DETR is kept at VDD by the detector circuit, and the MP3 is kept off. The LDO will generate a stable regulated voltage to VDD_OSC, and the internal circuits (ring oscillator) will perform their normal circuit functions.

Under the latch-up I-test with positive trigger current applied to the I/O pad, the injecting holes (from the positive trigger current) towards the ring oscillator (internal circuits) are detected by the hole detector (a long strip of P+ diffusion placed between the I/O cells and internal circuits), which causes the voltage level at node P1 to be raised. When the state at P1 is changed from low to high, the state at SW_DETR (the output of the detector circuit) is switched to low. Then, the MP3 will be turned on, and the LDO will be turned off. Due to MP3 being turned on and MP0 being turned off, the LDO circuit stops to generate the power supply to the VDD_OSC of ring oscillator. Without any power supply to VDD_OSC, any current flowing through the latch-up paths in the internal circuits can be automatically stopped. After the latch-up I-test, no positive trigger current is applied to the I/O pad (no hole injecting towards the internal circuits), so the voltage level at node P1 returns to GND. The state of SW_DETR returns to high, and the LDO circuit restarts working normally to supply voltage to VDD_OSC. Finally, the internal circuits return to their normal circuit functions.

When a negative trigger current is applied to the I/O cell during the latch-up I-test, the injecting electrons (from the negative trigger current) towards the internal circuits are then detected by the electron detector (N+/ N-well placed between the I/O cells and internal circuits), which causes the voltage level at node N1 to be pulled down. When the state at N1 is changed from high to low, the state at SW_DETR (the output of the detector circuit) is switched to low, causing the MP3 to be turned on, and then the MP0 will be turned off. So, the LDO circuit will be turned off. Because there is no power supply to the VDD_OSC, any current flowing through the latch-up paths in the internal circuits can be automatically stopped. After the latch-up I-test, no negative trigger current is applied to the I/O pad (no hole injecting towards the internal circuits), so the voltage level at node N1 returns to VDD. The state of SW_DETR returns to high, and the LDO circuit restarts its normal operation to supply voltage to VDD_OSC. The internal circuits return to their normal circuit functions.

With such an innovative circuit solution, the latch-up immunity of CMOS ICs can be substantially increased, but with a short distance between the I/O cells and the blocks of internal circuits to save the chip layout area [31].

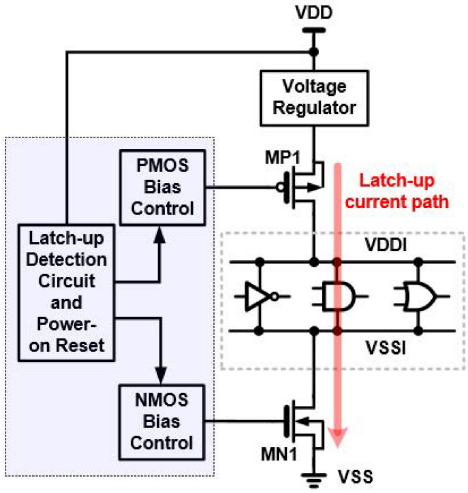

FIGURE 10. The latch-up current detection and recovery circuit [32].

IV. RESTART POWER SUPPLY TO STOP LATCH-UP CURRENT

Due to the parasitic latch-up paths in CMOS ICs, transient trigger noise appears not only in the I/O pad but also in the internal core circuits through the metal connections of the VDD/GND power lines. When the parasitic latch-up path is triggered, the huge current through the latch-up path can cause irreversible damage to the internal circuits. However, the latch-up state can be removed if the power supply is stopped. By switching the control circuit on power supply, the over-current detection circuits were invented to interrupt the current flow of the latch-up path [32], [33], [34], [35], [36], and therefore to stop the latch-up current.

A. LATCH-UP DETECTION AND RECOVERY CIRCUIT [32], [33]

The concept of latch-up current detection and recovery circuit is shown in Fig. 10 [32]. The circuit includes a power control switch MP1 (or MN1) and a latch-up detection circuit, which controls the gate of the switch MP1 (or MN1). The internal core power supply VDDI is generated from the voltage regulator. When the parasitic latch-up path of the core circuit block is triggered, an extensive dc-current will appear between the VDDI and VSSI. Thus, the large current will cause the power supply voltage (VDD) to drop significantly, which is detected by the latch-up detection circuit. Then, the switch MP1 (MN1) is turned off by the PMOS (NMOS) bias control to interrupt the latch-up current from the voltage regulator to the internal circuits, so the latch-up state can be removed. Finally, the power supply will be restarted to support the normal circuit operations in the internal circuits.

To realize such a circuit concept, the latch-up prevention circuit which composed of an intended function circuit and a latch-up detection circuit is shown in Fig. 11 [33]. A switch MN0 with a resistor R1 is connected between the ground

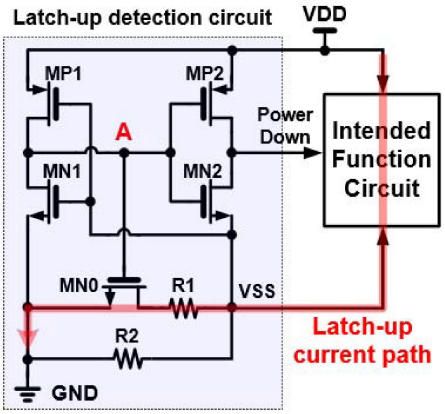

FIGURE 11. Realization of a latch-up prevention circuit [33].

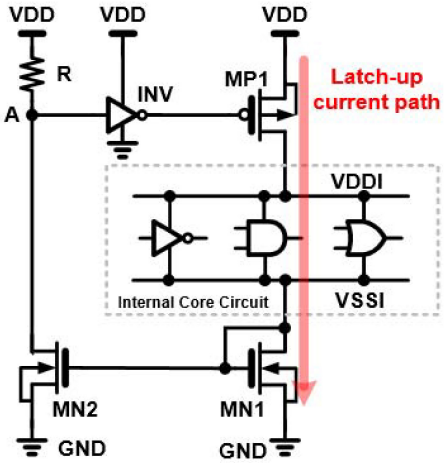

FIGURE 12. Latch-up current self-stop circuit [34].

terminal and the intended function circuit to prevent latch-up issues. The latch-up detection circuit, which is composed of two inverters (MP1, MP2, MN1, and MN2), MN0, R1, and R2, is used to turn the power on or off of the intended function circuit. The power-down control signal is the output of the latch-up detection circuit, and it decides whether the intended function circuitry is enabled or disabled. When the power-down signal has a low value (logical low), the power supply for the intended function circuitry operates normally. In a power-down state with a high value (logical high), the power supply for the intended function circuitry is removed to stop the latch-up event.

During normal circuit operations, the voltage difference between node VSS and the ground (GND) is small due to the R1 of lower resistance. Therefore, transistor MP1 is turned on, and the gates (node A) of the MP2 and MN2 are pulled to logic "High", which causes the MN2 to be turned on and to pull the power-down signal to a lower voltage level. So, the power-down signal is logical "Low", and the intended function circuitry is running normally.

When a latch-up issue occurs inside the intended function circuit, the huge latch-up current conducting through R1 will cause a greater voltage drop between node VSS and ground (GND). Because the voltage drop exceeds the threshold voltage of transistor MN1, the MN1 will be turned on to pull down the voltage level at node A, and then the gate of the MN0 will be turned off to stop the current flowing out from the intended function circuit. As transistor MN1 is turned on, node A is also pulled low, which causes the MP2 to be turned on and the MN2 to be turned off to pull the power-down signal to logical "High". The intended function circuitry will be in a power-down state, so the latch-up occurrence can be removed by stopping the current of the latch-up path.

After the latch-up condition ends, the voltage level at VSS node will be pulled low again due to the resistor R2 of some suitable resistance, and then the power-down signal goes back to a "low" state, and the intention circuit is turned back to its normal circuit operation.

B. LATCH-UP CURRENT SELF-STOP CIRCUIT [34]

The latch-up current self-stop circuit realized with a MOS switch and a current mirror detector is shown in Fig. 12 [34]. The circuit consists of a PMOS switch MP1, a diode-connected NMOS MN1 with its current mirror pair MN2, and the circuit (INV and R) used to bias the gate of MP1. The current extractor of the internal core circuit is made by using MN1 and MN2 NMOS transistors built as a current mirror. The resistor R between VDD and the inverter (INV) input node A is used for the current-voltage converter, which provides the feedback current signal to control the gate of switch MP1 via the INV inverter.

During the normal circuit operation, the voltage drop on the resistor R is minimal since the current flowing through it is relatively small. The input stage of inverter INV node A coupled to VDD by the resistor R is biased in the "high" state, which makes the gate of the MP1 transistor biased at a "low" state. So, the MP1 is turned on, and the power supply VDD is passed to the internal core circuit (VDDI). The internal core circuit can be generally operating to perform the intended circuit functions.

If the parasitic latch-up path inside the internal core circuit was triggered on, a large current will appear on the path from VDD to GND through MP1 and MN1. When a huge current is identified, it will be mapped to MN2 and the resistor R by the current mirror. The voltage drop across the resistor R is greatly increased by the mapped large current. This large voltage drop makes the state of the INV input node A changing from "high" to "low", and then the PMOS switch of MP1 is turned off. When the MP1 is turned off, the huge latch-up current flowing through the parasitic latch-up path in the internal core circuit can be stopped, and the latch-up occurrence is removed.

When the latch-up current is shut off, the voltage drop on the resistor R is decreased to zero, so that the output state of the inverter INV is changed into a "low" state, and then the switch MP1 is re-turned on. Thus, the internal core circuit is auto-reset and back to its normal circuit operation again.

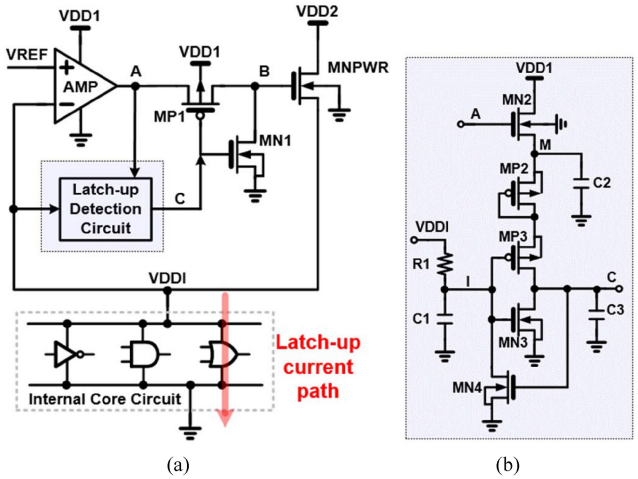

FIGURE 13. (a) The voltage regulation with latch-up prevention circuit, and (b) the corresponding latch-up detection circuit [35].

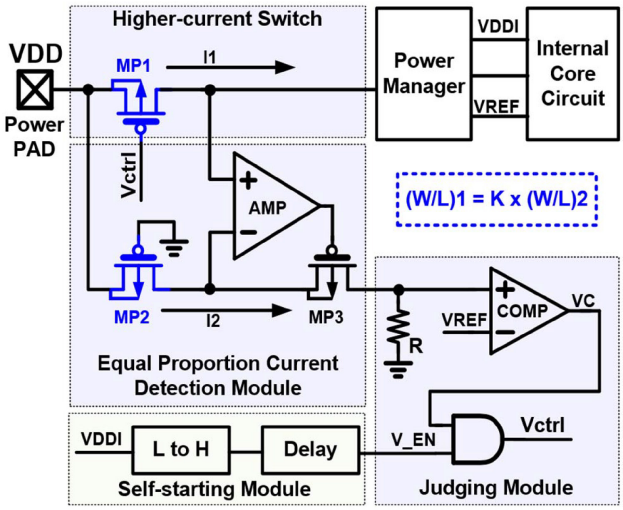

FIGURE 14. The latch-up over-current prevention circuit independent of power module [36].

C. VOLTAGE REGULATION WITH LATCH-UP PREVENTION CIRCUIT [35]

The combination of voltage regulation and latch-up prevention circuit is shown in Fig. 13(a) [35]. The voltage regulation is composed of an amplifier (AMP), a power transistor MNPWR, and a latch-up detection circuit. The latch-up prevention circuit is made up of a latch-up detection circuit, a switch transistor MP1, and MN1. The output (node C) of latch-up detection circuit is used to enable or disable the power transistor (MNPWR) by switching MP1 and MN1. The corresponding circuit implementation for the latch-up detection circuit is shown in Fig. 13(b), which includes the transistors MN2, MP2, MP3, MN3, an RC averaging circuit (R1 and C1), and a feedback transistor MN4. The AMP output node A is connected to the gate of MN2, whose drain is connected to the external power supply voltage VDD1 and whose source is connected to the source of two series-connected MP2 and MP3. Node M is defined by the coupled sources of transistors MN2 and MP2, which are also connected to the capacitor C2 to stabilize the voltage at node M. Node I is connected to the gates of MP3 and MN3, as well as the RC averaging circuits R1 and C1.

During normal circuit operation, the voltage regulation provides a constant voltage to the internal core circuit, and the gate of transistor MP1 is turned on due to the latch-up detection circuit output (node C) being at a lower voltage. The MN1 is turned off, and the power transistor MNPWR is turned on.

If the latch-up path inside the internal core circuit was triggered on, a huge latch-up current will flow from VDDI to GND, and the VDDI is dropped down. The internal power supply voltage VDDI is connected to the input of the detection circuit, and the voltage at node I decreases with a time constant determined by R1 and C1. As the voltage level of node I falls below that of node M by two threshold voltages (i.e., the threshold voltage drops of transistors MP2 and MP3), the output C rises to a high voltage value, and then transistor MN4 is turned on, which further discharges node I and increases the rising voltage of output C. The latch-up detection circuit turns off the transistor MP1 and turns on the transistor MN1. Then, the MNPWR is turned off to stop the latch-up current in the internal core circuit.

D. LATCH-UP OVER-CURRENT PREVENTION CIRCUIT [36]

The latch-up over-current prevention circuit independent of power module is shown in Fig. 14, which consists of a higher-current switch MP1, an equal proportional current sensing module, a judging module, and a self-starting module. A higher-current switch MP1 is connected to the power pad (VDD), the chip power manager module, and the internal core circuit, while the chip power manager module is connected to the self-starting module. The switch MP1 is used to interrupt the latch-up current path from the power line VDD to the internal core circuit. The latch-up state can be released and then auto-reset back to normal operation again by the self-starting module and the judging module.

An equal proportion current detection module consists of a lower-current switch MP2, an operational amplifier (AMP) connected to a negative feedback loop, which is used to ensure that the drain voltage of higher-current switch MP1 and lower-current switch MP2 are identical, and a PMOS transistor MP3 is used to control the feedback voltage. In addition, the sources of the higher-current switch MP1 and the lower-current switch MP2 are connected to the power supply VDD to ensure that I1 and I2 are proportional, and I1 is the K times of I2, which provides the current sense function of MP1 and MP2 to be enabled synchronously.

In the judging module, an equal proportion of output current (I2) is converted to voltage with the drain of transistor MP3 via resistor R1, which is connected to the positive input terminal of a comparator (COPM). Besides, the negative input terminal reference voltage (VREF) is used to

determine whether the I2 exceeds the pre-set threshold or not. The self-starting module is composed of a low-voltage-to-high conversion circuit (L to H) and a delay circuit. The output voltage of the self-starting circuit (V_EN) and output voltage (VC) of COMP are the input terminals to the logic AND gate in the judging module. The output (Vctrl) of logic AND gate is used to control whether the MP1 is enabled or disabled.

Under normal conditions, the output current I2 of the equal proportion detecting module is converted to a voltage by R, which is less than the reference voltage VREF. Therefore, the output of COMP (VC) is logic low, the output of the judgment module is also logic low, and the higher-current switch MP1 is kept in conduction.

When the latch-up issue occurs in the internal core circuit, the current I1 flowing to VDDI will be increased significantly. Thus, the output of the equal proportion current detecting module incrementally exceeds the default reference voltage, followed by the corresponding output voltage of I2. As a result, the judgment circuit generates the signal (Vctrl) "High" to turn off the switch MP1, and the current to the power manager for the internal core circuit will be stopped. The latch-up occurrence in the internal core circuit will be resolved when the power supply to the power manager is disconnected. After that, the power manager module is detected at a low-level voltage by the self-starting circuit. The high-current switch MP1 is turned on again, the power manager is recovered, and the normal functional operation of the internal core circuit is restored.

V. DISCUSSION AND COMPARISON

With the inherent parasitic SCR paths in CMOS technology, the latch-up issue has been one of the main reliability concerns in CMOS IC products. To avoid damage or reliability issues from latch-up events in harsh environments, such as industrial applications or automotive applications, latch-up prevention must be paid more attention not only in chip layout phase, but also in the beginning of circuit design phase. It may be a good way to use the additional process modification provided by the foundry to overcome latch-up issues. But, the corresponding cost of chip fabrication will become expensive. Hence, the cost-efficient solution by using circuit methods was proposed to enhance latch-up immunity in the IC industry.

The devices located at the I/O pads must be surrounded by double guard rings, as specified by the design rules of foundry, to overcome the latch-up issues at the I/O pads. Thus, the latch-up event would not occur in the IO cells, when the I/O cell layout has been drawn with the suitable guard rings. But, the internal circuits, with no guard rings surrounding the devices, are sensitive to latch-up issues. To reduce the latch-up trigger current (that applied at the I/O pad with the I/O circuits) injected into the internal core circuits, the circuit solution of "active guard ring" has been proposed to improve latch-up immunity. In addition, the auto-detector circuit with the corresponding control circuits was invented to detect the latch-up trigger current that injected toward the internal circuits, and then to stop the power supply of the internal circuits to avoid the permanent hardware failure. The power supply of the internal circuits will be automatically re-supplied when the injected latch-up trigger current was disappeared. On the other hand, when the transient current or voltage was coupled into the internal core circuits to cause latch-up events inside them, the power supply of internal circuits can be reset and re-started by the MOS switch to shut down the latch-up current path inside the internal circuits. The MOS switches are controlled by the corresponding latch-up detection circuits, which required some additional layout area to implement the switch with acceptable transient and steady-state voltage drops.

In the design of "active guard ring", with some additional devices directly connected to the I/O pads, a little increase of capacitive loading from the added devices will be seen by the signals at the I/O pads. In the circuit solution of auto-detector circuit or the method to restart power supply, there was no device of the proposed circuits directly added to the I/O pads. Thus, no capacitive loading was seen by the signals at the I/O pads. The comparisons among various latch-up prevention by circuit solutions were summarized in Table 1.

VI. EXAMPLE OF APPLICATION

To explore the advantage of the proposed auto-detector circuit [31], a CMOS digital IC with 44 pads is depicted in Fig. 15, where there are 40 I/O pads, two power pads, and two ground pads. The power and ground pads used for I/O cells are usually different from the power and ground pads used for internal circuits. The auto-detector circuit and LDO are supplied with the power (VDDI) and ground (VSSI) pads for internal circuits, and the power of internal circuits (logic gates) is supplied by the output of LDO (voltage regulator). With the I/O cell library provided by foundry, each I/O cell has been drawn with a fix cell layout area of 60μm x 180μm, including the bonding pad. There are 11 pads arranged at each side of the 44-pin CMOS IC, and the corner cells are applied at the four corners to provide the metal connections among the I/O cells located at the four sides of the chip layout. Finally, the total chip area of this 44-pin CMOS IC realized in a 0.18-μm 1.8V/3.3V CMOS process with the typical I/O cell library is 1085μm x 1085μm, whereas the area for the internal core circuits is 725μm x 725μm. The spacing between the I/O cells and the internal core circuits is 15 μm, in which the P+ and N+ diffusion rings used to detect the latch-up trigger current injecting from the I/O cells are drawn as 2 μm in width, and 2 μm spacing between them. These P+ and N+ diffusion rings, which are placed at each side between the I/O cells and the internal core circuits, are connected together by metal lines to the latch-up auto-detector circuit. Thus,

TABLE 1. Comparisons among the circuit solutions to improve latch-up immunity.

Methods	Reduce Trigger Current from I/O Pad (Active Guard Ring)		Auto-detector Circuit to Stop Latch-up Current Path	Restart Power Supply to Stop Latch-up Current Path			
References	[29]	[30]	[31]	[33]	[34]	[35]	[36]
Design Complexity	Low	Low	Low	Low	Low	High	High
Occupied Silicon Area	Middle	Middle	Small	Middle	Middle	Large	Large
Standby Leakage Current	No	No	No	Yes	Yes	Yes	Yes
Add Loading to the I/O Signal	A little	A little	No	No	No	No	No
Latch-up I-test result (at room temperature)	+74mA / -810mA	+ 300mA / -380mA	Over ± 500mA	N.A.	N.A.	N.A.	N.A.

TABLE 2. Layout area occupied by each block in a CMOS digital ic of 44 pads implemented with auto-detector circuit.

Layout Area of Each Block		Occupied Area
Total 44 I/O PADs		55.83%
Internal Core Circuit (Logic Gate)		40.5%
LDO (Voltage Regulator)	Total LDO	3.6%
	Power MOS (W/L=6000μm/0.35μm)	Power MOS (2.2%)
Auto-detector Circuit		0.07%
Latch-up immunity		> ± 500mA

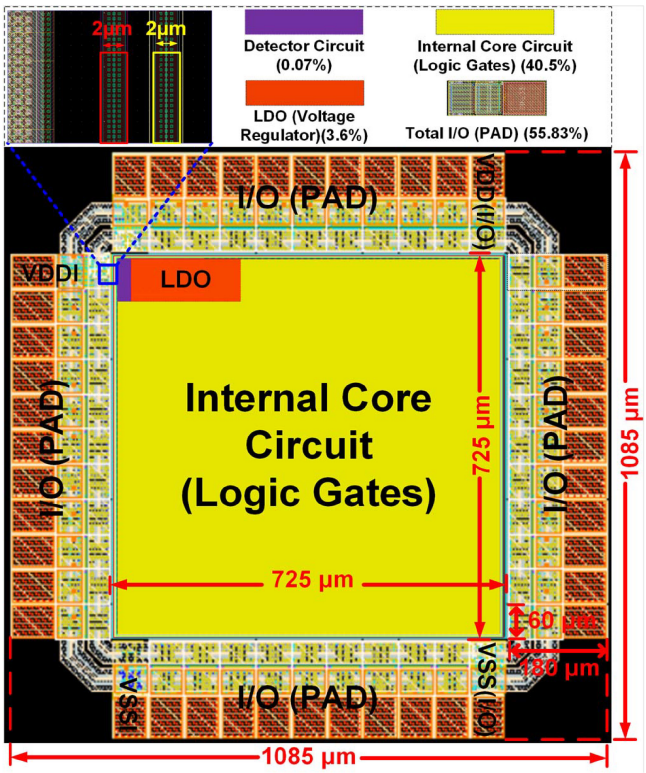

FIGURE 15. The chip layout to show the application of the proposed auto-detector circuit and LDO in a CMOS digital IC with 44 pads, realized in a 0.18-μm 1.8V/3.3V CMOS process.

the latch-up trigger current applied to the I/O pads at each side of the CMOS IC can be detected and sent to the auto-detector circuit. The output of the auto-detector circuit is used to shut down the LDO (voltage regulator) which supplies the power to the internal circuits (logic gates). Thus, the latch-up current in the internal circuits can be fully stopped to avoid the burned-out failure. When the latch-up trigger current disappears, the LDO (voltage regulator) will return back to its normal function to supply the power for internal circuits.

Layout area occupied by each block in a CMOS digital IC of 44 pads implemented with auto-detector circuit to overcome latch-up issue has been listed in Table 2. With the calculation on the layout area of each block in Fig. 15, the area occupied by all I/O cells (including pads), the internal core circuit (logic gates), the LDO (voltage regulator), and the auto-detector circuit are 55.83%, 40.5%, 3.6%, and 0.07%, respectively. Without widely enlarging the spacing between the I/O cells and internal circuits, the proposed method with the auto-detector circuit and LDO co-operation can perform high latch-up immunity for the CMOS IC to meet the practical applications in harsh environments.

VII. CONCLUSION

A comprehensive overview of circuit solutions for latch-up prevention is presented in this article. The parasitic p-n-p-n structure is inherent in the bulk CMOS technology, which often caused latchup failure of CMOS ICs during the field

applications. In the applications with harsh environment, the overshooting/undershooting noise glitches coupling to the microelectronics systems (equipped with CMOS ICs) would be huge. The latchup immunity of CMOS ICs in such harsh applications has been requested with a much higher specification, as compared to that used in the consumer electronics. In the scaled-down CMOS technology with shorter distances between devices in the chip layout of CMOS ICs, the latch-up paths would be easily triggered on by the external transient currents or noise voltages. To effectively improve latch-up immunity of CMOS ICs, circuit solutions have been proposed to overcome the latch-up issues, which did not require high costs of utilizing additional process layer or a wider distance in chip layout. Latchup prevention in CMOS ICs by circuit solutions is an emerging topic that IC designers shall pay attention.

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