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Investigation of CDM ESD Protection Capability Among Power-Rail ESD Clamp Circuits in CMOS ICs With Decoupling Capacitors

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ABSTRACT The power-rail electrostatic discharge (ESD) clamp circuits have been widely used in CMOS integrated circuits (ICs) to provide effective discharging paths for on-chip ESD protection design. Among all ESD events, the most serious threat is posed to ICs by the charged-device model (CDM), as compared with other ESD models. In this work, the CDM ESD protection capability among different power-rail ESD clamp circuits was studied and analyzed with the very-fast transmission line pulse (VF-TLP) and all the measurements are performed at room temperature. The combinations of power-rail ESD clamp circuits with internal circuits together, which are realized by ring oscillator and different decoupling capacitors, were fabricated in the 0.18-μm CMOS technology with the 1.8-V devices to further investigate their overall CDM ESD robustness under chip-level field-induced CDM (FI-CDM) ESD stress. The investigation result of this work is helpful to provide the best selection on the power-rail ESD clamp circuit for on-chip CDM protection design in CMOS ICs.

INDEX TERMS Electrostatic discharge (ESD), power-rail ESD clamp circuit, charged-device model (CDM), very-fast transmission line pulse (VF-TLP), decoupling capacitor.

I. INTRODUCTION

It is an inevitable issue for IC products to be confronted with ESD events. For the purpose to solve the ESD problem and elevate the robustness of IC products, different kinds of power-rail ESD clamp circuits have been reported [1], [2], [3]. The power-rail ESD clamp circuits must remain off-state during normal functional operation of the internal circuits and can be quickly turned on to discharge ESD current when the ESD event occurs. Among all ESD events, the CDM ESD event has become a greater challenge due to the trend toward thinner gate oxide and larger package sizes in CMOS ICs [4].

The peak value of CDM discharging current is strongly dependent on the parasitic capacitance of the device under test (DUT), which will be with the peak value of 5 ~ 10A under the test condition of 500V [5]. The parasitic capacitance of DUT is dominated by the silicon chip dimension and also the package size. The discharging current of CDM ESD event is possessed with a rise time of ~ 200 ps and a duration time of 1~ 5 ns [5]. Due to the faster speed and higher amplitude of current peak value in CDM ESD event, as compared with the human-body model (HBM) and machine-model (MM) ESD events, the power-rail ESD clamp circuits which have been widely used to protect HBM and MM ESD events should be further investigated to find their protection capability during CDM ESD events.

In this work, three different types of power-rail ESD clamp circuits are investigated with VF-TLP to verify their turn-on behavior in the time domain, turn-on resistance (R_{on}), and I_{t2} to determine the CDM protection capability. Further observation on the ESD discharging NMOS (M_{ESD}) devices with different channel lengths is also studied under VF-TLP stress. Moreover, the combinations of power-rail ESD clamp circuits with internal circuits together, which are realized by ring oscillator and different decoupling capacitors, were fabricated in 0.18-μm CMOS technology to investigate their

overall CDM ESD robustness under field-induced CDM (FI-CDM) ESD stress.

II. STAND-ALONE POWER-RAIL ESD CLAMP CIRCUITS

Three power-rail ESD clamp circuits are studied in this work, which are named as the gate-coupled NMOS (GCNMOS) [6], the RC-INV-NMOS [7], and the stacked-diodes-triggered NMOS [8]. The 1.8-V devices in a 0.18-μm CMOS technology are used to realize those ESD clamp circuits in this work.

A. GATE-COUPLED NMOS

The power-rail ESD clamp circuit of gate-coupled NMOS (GCNMOS) is shown in Fig. 1(a). The parasitic capacitance (C_{GD}) is depended on the device (M_{ESD}) itself, and the resistor R is realized by poly layer with a resistance of 1 kΩ. While CDM stressing on the power pin (VDD1), the CDM ESD current paths discharged by GCNMOS (M_{ESD}). The HSPICE simulation results on the gate voltage V_G during the normal power-on condition and ESD-like stress condition are shown in Figs. 1(b) and1(c), respectively. During normal circuit operation, the 1.8-V power supply with a longer power-on time (~1ms) is hard to couple up the gate voltage of M_{ESD}. Thus, the V_G is always staying at 0V, as the simulation waveform shown in Fig. 1(b), and the M_{ESD} remains in off-state. Under ESD-like stress condition in Fig. 1(c) with a pulse height of 5.5V (before 1.8-V device drain breakdown) and a short rising time (~10ns), the gate voltage of M_{ESD} was slightly increased due to the gate-coupling effect. But, the coupled gate voltage was still too low to turn on the channel of M_{ESD}. The voltage of the ESD-like pulse selected as 5.5V before device breakdown voltage may not enough for parasitic capacitance (C_{GD}) to demonstrate gate-couple behavior and to turn on the M_{ESD}. The gate-couple effect can be further enhanced, if the additional coupling capacitor was added and the resistance of R was increased.

B. RC-INVERTER-NMOS

The 2nd power-rail ESD clamp circuit studied in this work is shown in Fig. 2(a) with the main ESD device M_{ESD}. During normal circuit operation, the power-on time (~1ms) is larger than the time constant of V_{RC} which is determined by R and C. V_{RC} is charged to logic "high" to keep V_G staying at logic "low" through the inverter formed by M_{P1} and M_{N1}, as the simulation waveforms shown in Fig. 2(b), thus the M_{ESD} remains in off-state. Under ESD stressing in Fig. 2(c) with a pulse height of 5.5V (before 1.8-V device drain breakdown), the rising time of ESD-like pulse (~10ns) is smaller than the time constant of V_{RC}, and thus V_{RC} remains in logic "low". Therefore, the M_{ESD} is turned on through the inverter formed by M_{P1} and M_{N1} to discharge the ESD current. The HSPICE simulation results on the gate voltage V_G shown in Figs. 2(b) and 2(c) of verify the aforementioned ESD detection mechanism of the RC-INV-NMOS power-rail ESD clamp circuit.

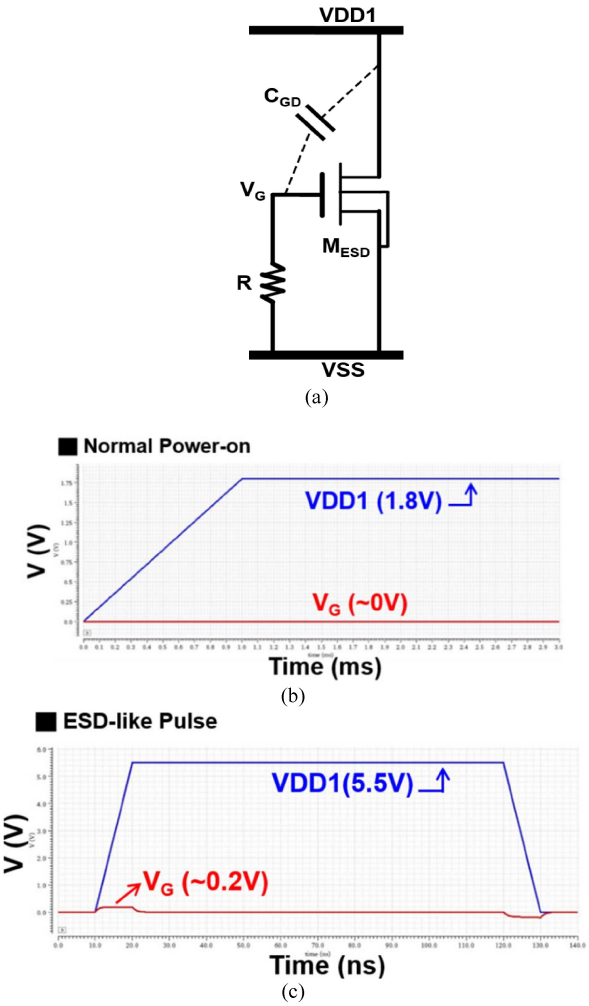


FIGURE 1. (a) The power-rail ESD clamp circuit realized by gate-coupled NMOS (GCNMOS). (b) The HSPICE simulation result under the normal power-on condition with 1.8-V power-on time of 1 ms, and (c) the HSPICE simulation result under ESD-like pulse with 5.5-V pulse height and a rising time of 10ns.

C. STACKED-DIODES-TRIGGERED-NMOS

The 3rd power-rail ESD clamp circuit studied in this work is shown in Fig. 3(a) with the stacked-diodes-triggered NMOS, which detects the voltage level to trigger on the ESD device M_{ESD}. During the normal circuit operation, the voltage on the power line (1.8V on VDD1 with the rising time of 1ms) is not enough to turn on the diode string made by four diodes, and thus V_G stays in logic "low" to keep M_{ESD} turned-off, as the HSPICE simulation waveforms shown in Fig. 3(b).

Under ESD stressing in Fig. 3(c) of HSPICE simulation with a pulse height of 5.5V (before 1.8-V device drain breakdown) and rising time of 10ns on VDD1, it is enough to make all four diodes in the diode string enter the forward-bias region. The current flows from the diode string to the resistor R, a voltage drop is created on R to turn M_{ESD} on, and then to discharge ESD current. The simulation results shown in Figs. 3(b) and 3(c) verify the aforementioned ESD detection mechanism in the power-rail ESD clamp circuit with stacked-diodes-triggered NMOS.

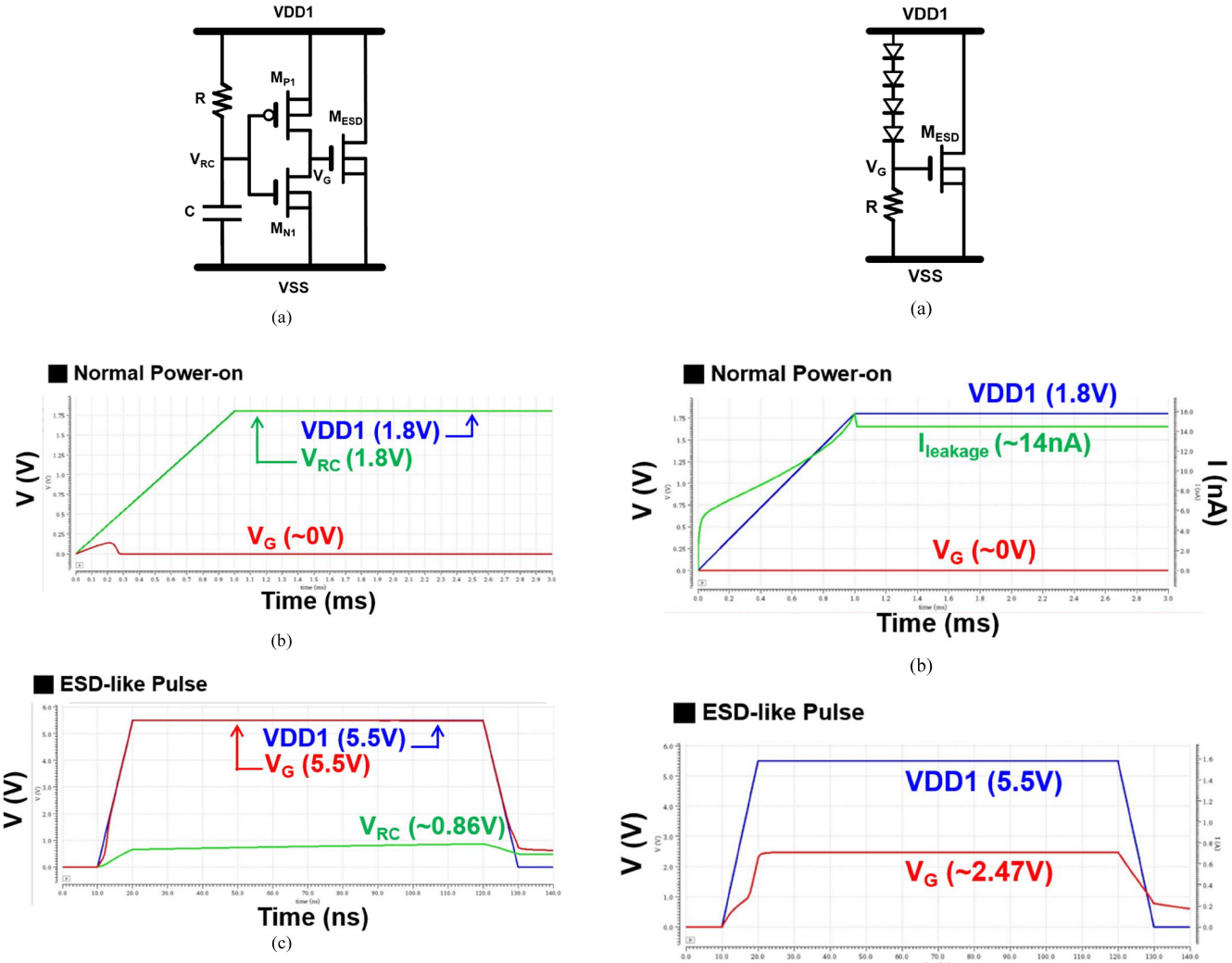


FIGURE 2. (a) The schematic of RC-INV-NMOS power-rail ESD clamp circuit, (b) the HSPICE simulation result under the normal power-on condition with 1.8-V power-on time of 1 ms, and (c) the HSPICE simulation result under ESD-like pulse with 5.5-V pulse height and a rising time of 10ns.

FIGURE 3. (a) The schematic of the power-rail ESD clamp circuit with stacked-diodes-triggered NMOS, (b) the HSPICE simulation result under the normal power-on condition with 1.8-V power-on time of 1 ms, and (c) the HSPICE simulation result under ESD-like pulse with 5.5-V pulse height and a rising time of 10ns.

III. EXPERIMENTAL RESULTS OF STAND-ALONE POWER-RAIL ESD CLAMP CIRCUITS

The splits of test circuits used in this study are listed in Table 1. The stand-alone power-rail ESD clamp circuits with the main ESD devices M_{ESD} drawn with different channel lengths are fabricated by TSMC 0.18-μm CMOS technology with 1.8V devices. The channel width of M_{ESD} is drawn with a fixed dimension of 36x28 μm (each finger width of 36μm, total 28 fingers), whereas the channel lengths are split with 0.18μm, 0.54μm, and 1.0μm to investigate their CDM ESD protection capability. The layout top view of M_{ESD} is shown in Fig. 4. The M_{ESD} is drawn with multi-finger style, and the silicide block layer is put on its drain/source region. The M_{ESD} is surrounded by the P-type guard ring at the outside.

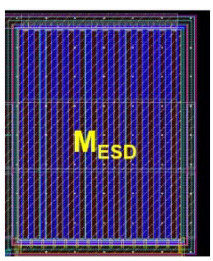


FIGURE 4. The layout top view of M_{ESD} drawn in multi-finger style with the silicide block layer put on its drain/source region.

A. VF-TLP MEASUREMENT

To characterize the robustness among different types of power-rail ESD clamp circuits with M_{ESD} of different channel lengths, the VF-TLP [9], [10] measurement with Thermo Scientific Celestron is used in this work. The pulse width of the VF-TLP measurement is selected as 5ns and the pulse rising time is 200ps. The typical VF-TLP measured I-V curve

TABLE 1. Splits of test structures on power-rail ESD clamp circuits for VF-TLP measurement.

Cell Name (Testkey Number)	Description (W/L in μm/μm)					
	R (kΩ)	C (pF)	Diode (W*L)	M_{P1} (W/L)	M_{N1} (W/L)	M_{ESD} (W/L)
SA-1 (Type A : GCNMOS)	~1	-	-	-	-	36*28 / 0.18
SA-2 (Type A : GCNMOS)	~1	-	-	-	-	36*28 / 0.54
SA-3 (Type A : GCNMOS)	~1	-	-	-	-	36*28 / 1
SB-1 (Type B : RC-INV-NMOS)	~749	3.5	-	8*10 / 0.4	3*7 / 0.4	36*28 / 0.18
SB-2 (Type B : RC-INV-NMOS)	~749	3.5	-	8*10 / 0.4	3*7 / 0.4	36*28 / 0.54
SB-3 (Type B : RC-INV-NMOS)	~749	3.5	-	8*10 / 0.4	3*7 / 0.4	36*28 / 1
SC-1 (Type C : Stacked-Diodes-Triggered NMOS)	~20	-	(10*10)	-	-	36*28 / 0.18
SC-2 (Type C : Stacked-Diodes-Triggered NMOS)	~20	-	(10*10)	-	-	36*28 / 0.54
SC-3 (Type C : Stacked-Diodes-Triggered NMOS)	~20	-	(10*10)	-	-	36*28 / 1

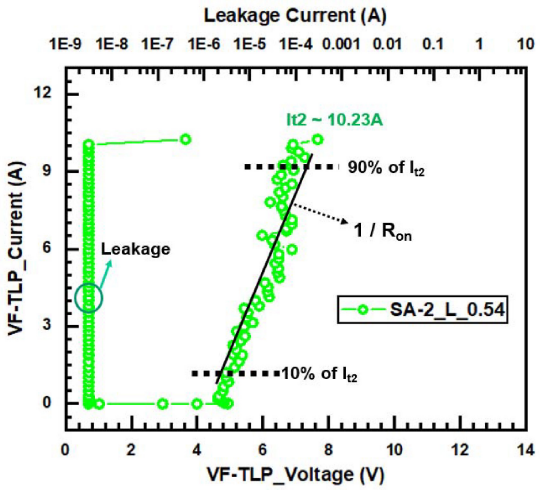


FIGURE 5. The calculation of turn-on resistance on the VF-TLP measured I-V curve. The turn-on resistance (Ron) is defined as the reciprocal of the slope from the point of 10% value of I_{t2} to the point of 90% value of I_{t2}.

is shown in Fig. 5, where the turn-on resistance (R_{on}) is defined as the reciprocal of the slope from the point of 10% value of I_{t2} to the point of 90% value of I_{t2}. This turn-on resistance (R_{on}) is one key factor to evaluate the protection capability of the power-rail ESD clamp circuit. The VF-TLP measured I-V curves among the fabricated power-rail ESD clamp circuits are shown in Figs. 6(a) ~ 6(d). The values of VF-TLP measured I_{t2} (10.47A for SA-1, 10.95A for SB-1, and 10.75A for SC-1) are almost the same among the test structures, since the sizes of M_{ESD} in these three splits are the same. In Fig. 5(a), the R_{on} of SA-1, SB-1, and SC-1 are 0.255Ω, 0.225Ω, and 0.237Ω by calculation. Under the same channel length (0.18 μm) and channel width (36x28 μm) of M_{ESD}, the SB-1 (RC-INV-NMOS) shows the smallest turn-on resistance, as compared with the other two structures.

To investigate the effect of channel length of M_{ESD} on the R_{on} of test structures, the measured results among three different structures of power-rail ESD clamp circuits are shown in Figs. 6(b) ~ 6(d). In Fig. 6(b) with the power-rail ESD clamp circuit of GCNMOS, the holding voltage (V_{hold}) is increased as the channel length of M_{ESD} is increased, where the V_{hold} are 4.029V, 4.639V, and 6.156V for lengths of 0.18μm, 0.54μm, and 1μm, respectively. The R_{on} is increased as the channel length of M_{ESD} is increased, where R_{on} are 0.255Ω, 0.281Ω, and 0.294Ω for lengths of 0.18μm, 0.54μm, and 1μm, respectively. In Fig. 6(c) with the power-rail ESD clamp circuit of RC-INV-NMOS, the R_{on} are 0.225Ω, 0.243Ω, and 0.284Ω for channel lengths of 0.18μm, 0.54μm, and 1μm, respectively. In Fig. 6(d) with the power-rail ESD clamp circuit of Stacked-Diodes-Triggered-NMOS, the R_{on} value is also increased as the length of M_{ESD} is increased, where R_{on} are 0.237Ω, 0.262Ω, and 0.278Ω for channel lengths of 0.18μm, 0.54μm, and 1μm, respectively. In addition, among these three types of power-rail ESD clamp circuits, the VF-TLP measured I_{t2} are all increased as the channel length of M_{ESD} is decreased, due to the corresponding smaller R_{on}.

B. INVESTIGATION ON TURN-ON SPEED

To compare the turn-on speed among different types of power-rail ESD clamp circuits under the very-fast CDM ESD event, the time for voltage clamping down by each power-rail ESD clamp circuit under 5-A VF-TLP measurement is calculated as the index for comparison on turn-on speed. The voltage waveforms at VF-TLP current of 5A are chosen, based on the test condition of small capacitance under CDM 500-V stress in the CDM test standard [5]. The voltage clamping-down time in this study is illustrated in Fig. 7, as the time period from the point of the peak voltage to the point of stable voltage in the corresponding time domain waveform at VF-TLP current of 5A. Such a voltage transient waveform can be found in the recorded data of VF-TLP measurement system.

The voltage transient waveforms in the time domain under 5-A VF-TLP measurement among the fabricated power-rail ESD clamp circuits are shown in Figs. 8(a) ~ 8(d), where the power-rail ESD clamp circuits are drawn with the same channel width (36x28 μm) of M_{ESD} but different channel lengths.

In Fig. 8(a), with the same channel length (0.18μm) and the same channel width of M_{ESD} in these three power-rail ESD clamp circuits, the voltage clamping-down time of SA-1, SB-1, and SC-1 are 4.15ns, 3.75ns, and 4ns, respectively. The power-rail ESD clamp circuit with the RC-INV-NMOS structure has the shortest voltage clamping-down time to discharge the CDM ESD current among these three circuits under investigation.

In Fig. 8(b), the voltage clamping-down times on the power-rail ESD clamp circuit of GCNMOS structure at 5-A VF-TLP measurement are 4.15ns, 4.3ns, and 4.5ns for the M_{ESD} with channel lengths of 0.18μm, 0.54μm, and 1μm,

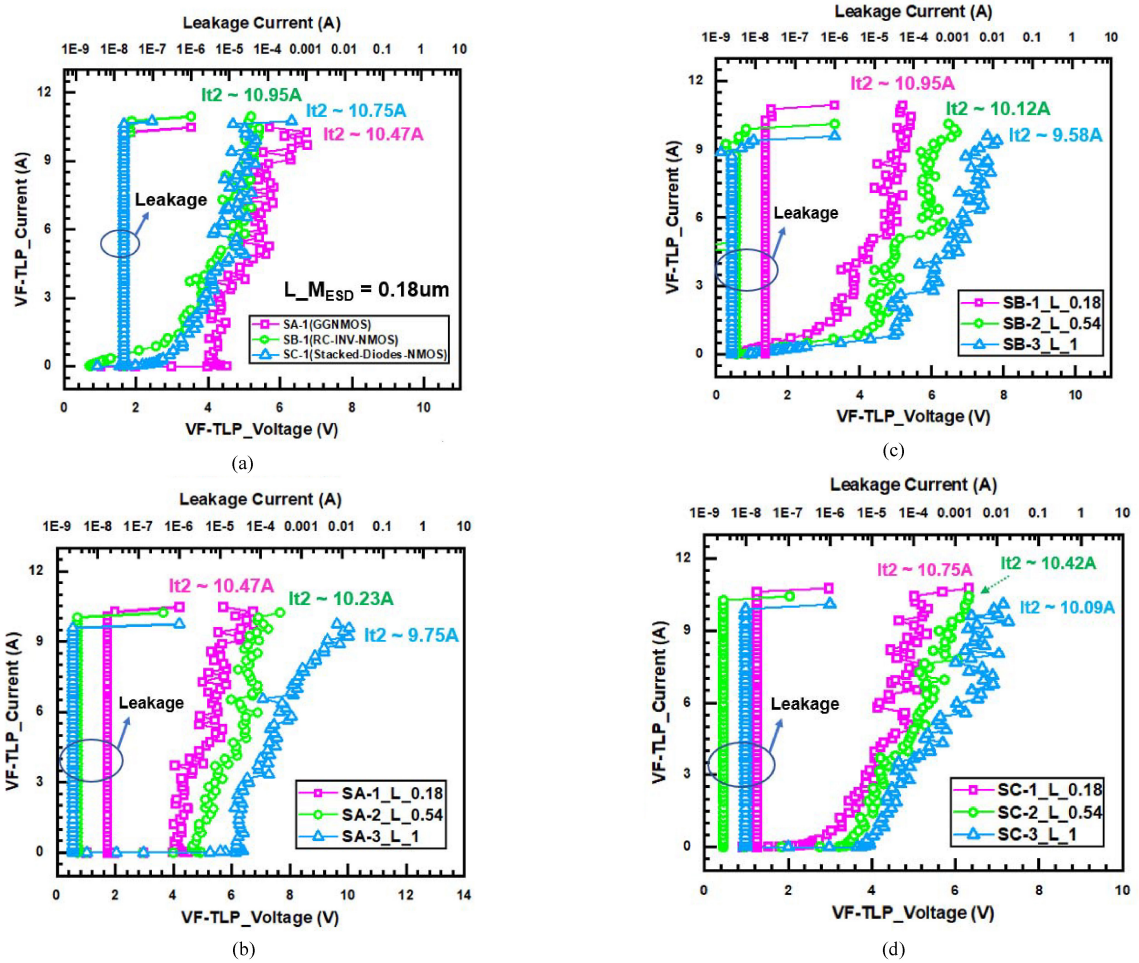


FIGURE 6. VF-TLP measured results (I-V curves) of (a) three types of the power-rail ESD clamp circuits with the same channel length of 0.18μm, (b) GCNMOS structure with different channel lengths, (c) RC-INV-NMOS structure with different channel lengths, and (d) Stacked-Diodes-Triggered NMOS with different channel lengths. The channel widths of M_{ESD} in these three splits are the same of 36x28 μm.

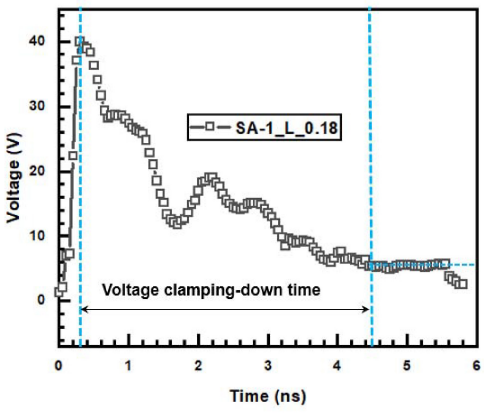


FIGURE 7. The calculation of voltage clamping-down time on the VF-TLP measured voltage waveform. The voltage clamping-down time is defined as the time period from the point of the peak voltage to the point of stable voltage in the time domain waveform at VF-TLP current of 5A.

respectively. In Fig. 8(c), the voltage clamping-down times on the power-rail ESD clamp circuit of RC-INV-NMOS structure at 5-A VF-TLP measurement are 3.75ns, 3.9ns, and 4.2ns for the M_{ESD} with channel lengths of 0.18μm, 0.54μm, and 1μm, respectively. In Fig. 8(d), the voltage clamping-down times on the power-rail ESD clamp circuit of Stacked-Diodes-Triggered-NMOS structure at 5-A VF-TLP measurement are 4ns, 4.1ns, and 4.35ns for the M_{ESD} with channel lengths of 0.18μm, 0.54μm, and 1μm, respectively. The voltage transient waveforms under 5-A VF-TLP measurement on these three circuits for the M_{ESD} with channel length of 0.54μm are similar to those with other channel lengths. Without complex overlapping curves to simplify the figures for clearly reading, only the voltage transient waveforms on the test circuits with channel lengths of 0.18μm and 1μm are shown in Figs. 8(b) ~ 8(d). As viewed on the voltage transient waveforms in each figure with the same structure of power-rail ESD clamp circuit, the test circuit with the shortest channel length has a shortest voltage clamping-down time.

The test results on three stand-alone power-rail ESD clamp circuits of different circuit structures with different channel lengths are summarized in Table 2, including the turn-on resistance (R_{on}), I_{t2}, and voltage clamping-down time. It

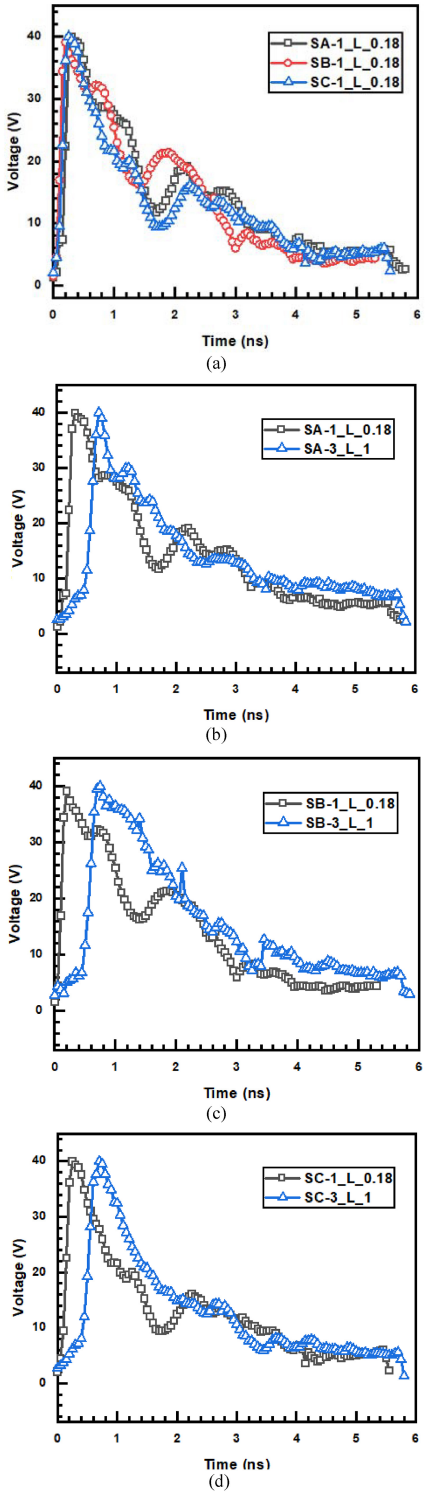


FIGURE 8. The voltage transient waveforms in the time domain under 5-A VF-TLP measurement of (a) three types of the power-rail ESD clamp circuits with the same channel length of 0.18μm, (b) GCNMOS structure with different channel lengths, (c) RC-INV-NMOS structure with different channel lengths, and (d) Stacked-Diodes-Triggered NMOS with different channel lengths.

is clearly observed that the shorter the channel length of M_{ESD} in the power-rail ESD clamp circuits is selected, the smaller R_{on} and the shorter voltage clamping-down time are

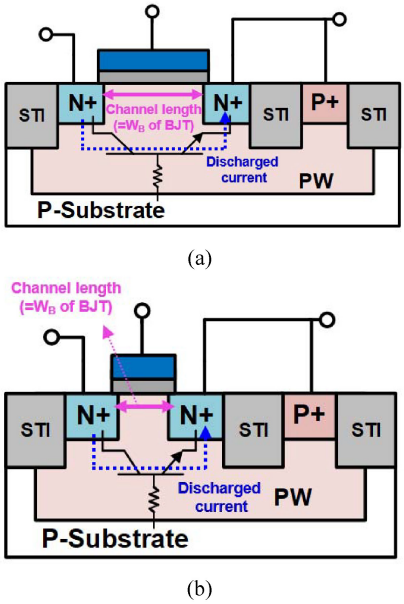


FIGURE 9. The cross-sectional views of (a) larger channel length of M_{ESD}, and (b) shorter channel length of M_{ESD}. The larger the channel length of M_{ESD}, the larger the R_{on}, and longer voltage clamping-down time is observed.

TABLE 2. VF-TLP test results on the stand-alone power-rail ESD clamp circuits.

Cell Name (Testkey Number)	Description			
	R_{on} (Ω)	I_{t2} (A)	Voltage Clamping - Down Time (ns)	Power Consumption @ 5A VF-TLP current (W)
SA-1 (Type A : GCNMOS)	0.255	10.47	4.15	25.83
SA-2 (Type A : GCNMOS)	0.281	10.23	4.3	27.63
SA-3 (Type A : GCNMOS)	0.294	9.75	4.5	37.93
SB-1 (Type B : RC-INV-NMOS)	0.225	10.95	3.75	22.21
SB-2 (Type B : RC-INV-NMOS)	0.243	10.12	3.9	26.01
SB-3 (Type B : RC-INV-NMOS)	0.284	9.58	4.2	35.16
SC-1 (Type C : Stacked-Diodes-Triggered NMOS)	0.237	10.75	4	24.85
SC-2 (Type C : Stacked-Diodes-Triggered NMOS)	0.262	10.42	4.1	26.67
SC-3 (Type C : Stacked-Diodes-Triggered NMOS)	0.278	10.09	4.35	28.77

*The power consumption (I x V) of each stand-alone power-rail ESD clamp circuit is calculated at the point of VF-TLP I-V curve at 5-A current.

demonstrated. As shown in Fig. 9, the R_{on} is proportional to the value of L/W of M_{ESD}. With the fixed channel width (W), the larger the channel length (L) of M_{ESD}, the larger the base width of lateral parasitic n-p-n BJT is. With the longer path that current needs to transit, the larger R_{on} is observed. The voltage clamping-down time is also relative to the base transit time of the BJT component. As illustrated in Fig. 9, the base transit time is defined as $W_B^2/2D_N$, the W_B represents the base width of the parasitic lateral BJT which is the channel length of M_{ESD}. The longer the M_{ESD} channel length, the longer the base width of the BJT, and results in longer voltage clamping-down time.

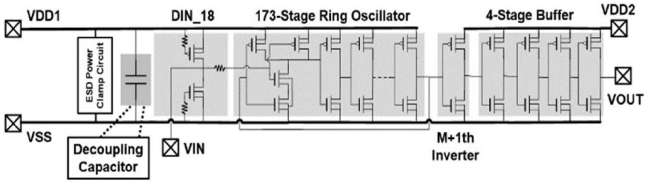


FIGURE 10. The schematic of test circuit with internal functional circuits (173-stage ring oscillator and decoupling capacitor) and a power-rail ESD clamp circuit to verify the corresponding effectiveness of CDM ESD protection.

Among all the three test circuits, the power-rail ESD clamp circuit of RC-INV-NMOS with a minimum channel length (0.18μm) of M_{ESD} performs the smallest turn-on resistance, the highest I_{t2}, and the shortest voltage clamping-down time. Thus, it can provide the best CDM ESD protection capability to protect the internal circuits of CMOS ICs.

IV. POWER-RAIL ESD CLAMP CIRCUITS WITH INTERNAL CIRCUITS

From the previous study with CDM ESD test results and detailed failure analysis [11], the on-chip decoupling capacitors added to maintain the stability of power supply voltage level had been confirmed to cause serious degradation on CDM robustness of CMOS ICs. The CDM discharging current can be considered as a high-frequency signal, which is discharging to the ground through the low-impedance path of Z=1/sC provided by decoupling capacitors, resulting in the gate oxide damages on the decoupling capacitors.

To verify the CDM ESD protection capability among the power-rail ESD clamp circuits, a functional circuit should be placed on the same chip as a testing vehicle with the ESD protection circuit together. Based on the prior work [11], the internal functional circuits are built with a ring oscillator and decoupling capacitors as the testing vehicles for verifying the CDM ESD protecting capability of different power-rail ESD clamp circuits.

A. TEST CIRCUITS

The internal functional circuits as a testing vehicle are realized with a 173-stage ring oscillator and decoupling capacitors [11]. The testkey splits of a ring oscillator with combinations of different decoupling capacitors and different power-rail ESD clamp circuits are listed in Table 3, where the channel lengths (widths) of M_{ESD} among the different power-rail ESD clamp circuits are all chosen to be 0.18μm (36x28 μm). The circuit schematic of test circuit with internal functional circuits and power-rail ESD clamp circuit to verify the corresponding effectiveness of CDM ESD protection is shown in Fig. 10. A 173-stage ring oscillator with decoupling capacitor is used as a testing vehicle to verify the CDM ESD protecting capability of power-rail ESD clamp circuit. The decoupling capacitor is very vulnerable to CDM ESD stress, so it is a good candidate as testing vehicle to investigate CDM ESD protecting capability of power-rail ESD clamp circuit. To clear identify whether the internal circuits (including the decoupling capacitors) were damaged by CDM, the output waveform of ring oscillator directly observed on the screen of digital oscilloscope can be monitored. When comparing the output waveform of ring oscillator, before and after CDM ESD tests, the CDM ESD protecting capability of different power-rail ESD clamp circuits can be clearly evaluated.

TABLE 3. Combinations of testkey splits with internal circuits and different power-rail ESD clamp circuits.

Cell Name	Description			Positive CDM Robustness (kV)	Negative CDM Robustness (kV)
	Testing Vehicle	Decoupling Capacitors	Power Clamp Circuits		
REF	Ring Oscillator	-	-	1	-1
Type D1	Ring Oscillator	NMOS	-	0.75	-0.5
Type D2	Ring Oscillator	PMOS	-	1	-0.75
Type D3	Ring Oscillator	Varactor	-	0.5	-0.75
Type A-1	Ring Oscillator	NMOS	GCNMOS	1.25	-1.25
Type A-2	Ring Oscillator	PMOS	GCNMOS	>1.5	-1.25
Type A-3	Ring Oscillator	Varactor	GCNMOS	1.25	-1.25
Type B-1	Ring Oscillator	NMOS	RC-INV-NMOS	>1.5	-1.25
Type B-2	Ring Oscillator	PMOS	RC-INV-NMOS	>1.5	>1.5
Type B-3	Ring Oscillator	Varactor	RC-INV-NMOS	1.25	-1.25
Type C-1	Ring Oscillator	NMOS	Stacked-Diodes-Triggered NMOS	>1.5	-1.25
Type C-2	Ring Oscillator	PMOS	Stacked-Diodes-Triggered NMOS	1.25	>1.5
Type C-3	Ring Oscillator	Varactor	Stacked-Diodes-Triggered NMOS	1.25	-1.25

*The M_{ESD} sizes of the power-rail ESD clamp circuits are all kept the same with the L of 0.18μm and W of 1008μm (36x28 μm).

The decoupling capacitors used in this study are with the device structures of NMOS, PMOS, and varactor, as those illustrated in Figs. 11(a), 11(b), and 11(c), with the capacitance of 5 pF. The test chip with the 13 splits listed in Table 3, as well as the 9 splits of stand-alone power-rail ESD clamp circuits listed in Table 1, was fabricated by TSMC 0.18-μm 1.8V/3.3V CMOS technology with 1.8V devices. The OM micrograph of the fabricated test chip is shown in Fig. 12(a), and the marked illustrations in Fig. 12(b) show the locations of the 13 test splits of Table 3 and the 9 test splits of Table 1.

Before CDM ESD testing, the output function is verified to ensure the ring oscillator and decoupling capacitors are functioning properly. The typical measured output waveform from the VOUT node of Fig. 10 is shown in Figs. 13(a) and 13(b), where an 82-MHz clock-like voltage waveform generated by the ring oscillator can be found. The peak-to-peak voltage swing on the power line (VDD1) is especially observed to judge whether the decoupling capacitor is functional, or not.

The peak-to-peak voltage swing on VDD1 in Fig. 13(a) is 1.061V for the test circuit (REF) with ring oscillator only. When an NMOS decoupling capacitor of 5 pF is added to the

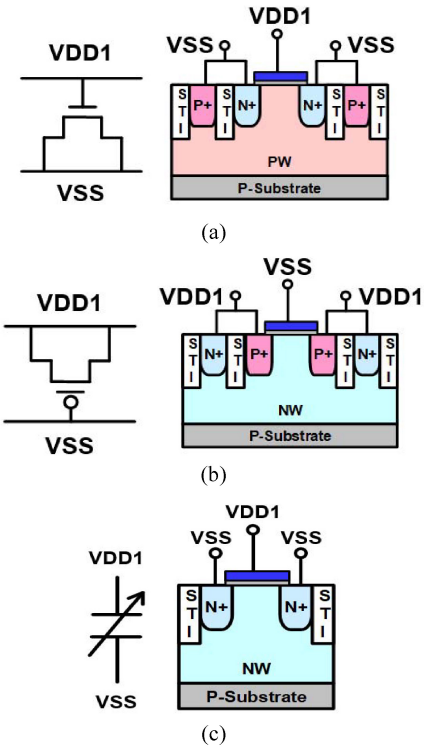


FIGURE 11. The symbols and device cross-sectional views of (a) NMOS decoupling capacitor, (b) PMOS decoupling capacitor, and (c) varactor decoupling capacitor, implemented in a 0.18-μm 1.8-V CMOS process.

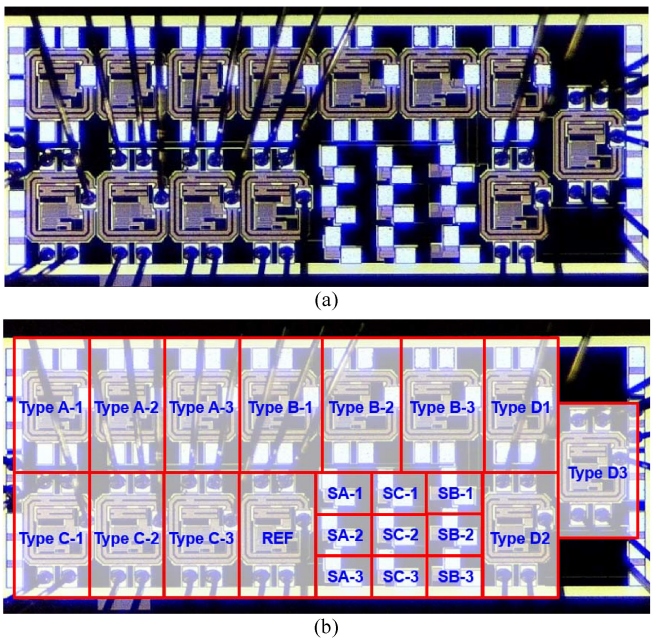


FIGURE 12. (a) The OM micrograph of the test chip fabricated in a 0.18-μm 1.8V/3.3V CMOS process, and (b) the chip micrograph with marked illustrations to show the locations of the 13 test splits of Table 3 and the 9 test splits of Table 1.

ring oscillator in the test circuit together, the peak-to-peak voltage swing on VDD1 is reduced to 0.593V, as shown in Fig. 13(b). The peak-to-peak voltage swing on the power line

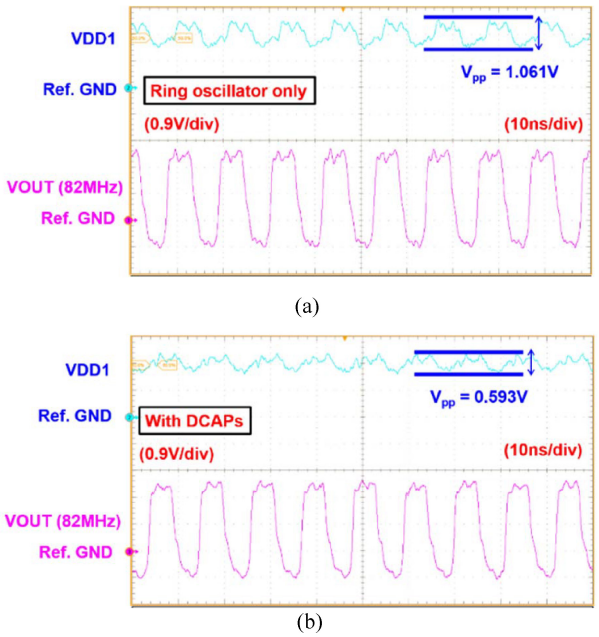


FIGURE 13. Measured voltage waveforms to verify the function of the test circuit with (a) ring oscillator only, and (b) ring oscillator with NMOS decoupling capacitor.

is induced by the L*di/dt effect with the parasitic inductance of about 5nH (1nH/1mm) [11]. In Type D1 (ring oscillator with NMOS decoupling capacitor), Type D2 (ring oscillator with PMOS decoupling capacitor), and Type D3 (ring oscillator with varactor decoupling capacitor), the measured voltage swings on VDD1 are 0.593V, 0.616V, and 0.613V, respectively. This has verified the effectiveness of the on-chip decoupling capacitor on suppressing the power line transient noise.

B. CDM ESD TESTING

The non-socket field-induced CDM test is performed with Thermo Scientific Orion 3 in this work. The CDM ESD testing is processed by placing the grounded pogo pin onto the VDD1 pin which is the power pin for the internal circuits (the ring oscillator and decoupling capacitors) with power-rail ESD clamp circuit together. The CDM ESD testing with positive and negative voltage polarities are schematically illustrated in Figs. 14(a) and 14(b), respectively. The device under test (DUT) is a silicon chip (with the 13 splits, as listed in Table 3) inside a 48-pin COB package. The zapping step is 250V, and the failure criterion is defined as the I-V curve shifting over 30% from its initial curve after CDM stressing, or the leakage current under 1.8-V bias increases over 10 times of magnitude from the initial leakage current for electrical verification. For function verification, the failure criterion is defined as the output frequency of ring oscillator is incorrect or deviates from the initial output waveform.

The CDM ESD testing results on all 13 testkey splits are also listed in Table 3, where if the DUT passed 250V qualification but failed at 500V, the CDM level is listed as

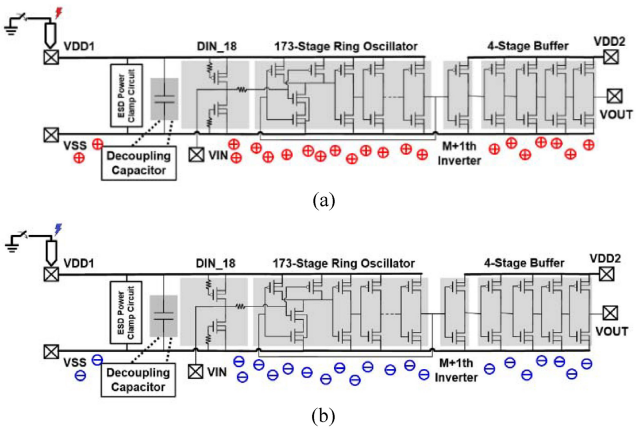


FIGURE 14. Schematic diagrams to show CDM ESD stressing on VDD1 pin with (a) positive and (b) negative polarities.

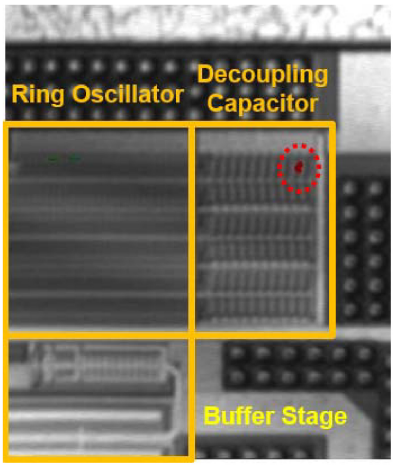


FIGURE 15. The EFA result of Type D1 testkey split (ring oscillator with decoupling capacitor of NMOS). The hot spot is located on the decoupling capacitor in the photo.

250V. As seen in Table 3, the test circuits with decoupling capacitors (Type D1, D2, and D3) show worse CDM levels than that of the baseline design (REF, no decoupling capacitor). The on-chip decoupling capacitor is very vulnerable to CDM ESD stress, so it is a good candidate as testing vehicle to investigate CDM ESD protection capability of the power-rail ESD clamp circuit.

With the CDM ESD testing results in Table 3, the test circuits with the presence of different power-rail ESD clamp circuits (Type A, Type B, and Type C) show better CDM levels than those of the test circuits with decoupling capacitors (Type D1, D2, and D3) only. The power-rail ESD clamp circuits have successfully discharged the displacement current induced by CDM ESD stressing, and thus enhance the CDM robustness.

Among the test circuit splits of Type D1, D2, and D3, the Type D2 (ring oscillator with decoupling capacitor of PMOS) shows a higher CDM level, as compared with the other two splits (D1 and D2). In the PMOS decoupling capacitor structure, the gate is connected to VSS and the source/drain (P+) diffusions are connected to VDD1 with the bulk diffusion (N+) in N-well, as illustrated in Fig. 11(b). During CDM ESD stressing on the VDD1 pin, the charges accumulated in the p-substrate can be discharged to the external ground through the p-sub/N-well junction with N+ bulk diffusion, and thus decreasing the probability of sabotaging the gate oxide. Among the test circuit splits Type A to Type C listed in Table 3, the Type B splits with the power-rail ESD clamp circuit of RC-INV-NMOS structure have higher averaged CDM levels than those of Type A and Type C splits.

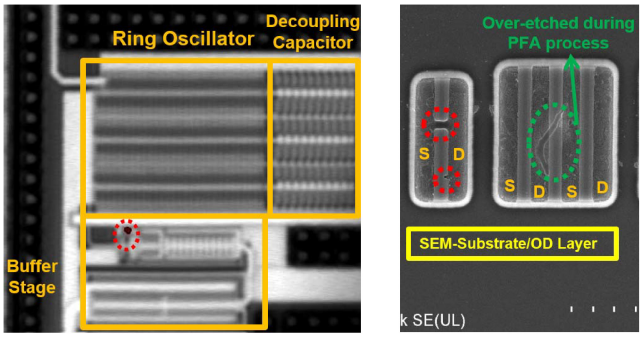
Among 13 test circuit splits in Table 3, the Type B-2 (decoupling capacitor of PMOS with the power-rail ESD clamp circuit of RC-INV-NMOS structure) shows the highest CDM level. As corresponding to the measured results of voltage clamping-down time by VF-TLP, the structure of the power-rail ESD clamp circuit with shorter voltage clamping-down time and smaller turn-on resistance shows a higher CDM ESD protection capability. The CDM ESD testing results listed in Table 3 are fully consistent with the aforementioned VF-TLP measured results on the stand-alone power-rail ESD clamp circuits in Table 2.

C. FAILURE ANALYSIS

The electrical and physical failure analysis (EFA and PFA) are performed on the DUT after CDM ESD stressing. The InfraRed Optical Beam Induced Resistance Change (IR-OBIRCH) is applied to do the electrical failure analysis. The instrument locates the failure point by scanning and heating through the surface of the biased circuits with an IR laser. The position that impedance variation is different from other regions has a higher probability that is considered to be a failure point.

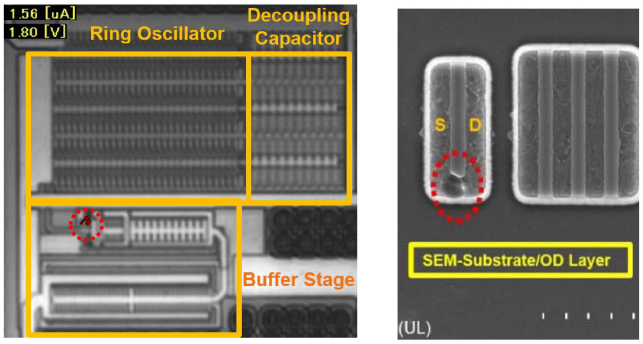
The EFA result on the Type D1 testkey split (ring oscillator with decoupling capacitor of NMOS) is shown in Fig. 15. As seen in the micrograph photo, the failure point is detected on the decoupling capacitor after −750V CDM ESD stressing. From the EFA result, the degradation of CDM tolerance caused by the presence of a decoupling capacitor has been verified again.

Fig. 16 and Fig. 17 show the EFA and PFA results of Type A-2 (the ring oscillator with decoupling capacitor of PMOS and power-rail ESD clamp circuit of GCNMOS) and Type C-2 (the ring oscillator with decoupling capacitor of PMOS and power-rail ESD clamp circuit of Stacked-Diodes-Triggered NMOS) after CDM ESD stressing of -1.25kV and +1.25kV, respectively. In Fig. 15(a) and Fig. 16(a), the failure locations are spotted on the cross-domain interface circuits in the VDD2 power domain. According to Fig. 16(a) and Fig. 17(a), further PFA is done with a total-delayer process, and Scanning Electron Microscope (SEM) is used to get the clear FA pictures shown in Fig. 16(b) and Fig. 17(b).



(a) (b)

FIGURE 16. Failure analysis results of Type A-2 testkey split (ring oscillator with decoupling capacitor of PMOS and power-rail ESD clamp circuit of GCNMOS). The (a) EFA and (b) PFA results on the Type A-2 testkey after −1.25kV CDM ESD stressing.



(a) (b)

FIGURE 17. Failure analysis results of Type C-2 testkey split (ring oscillator with decoupling capacitor of PMOS and power-rail ESD clamp circuit of Stacked-Diodes-Triggered NMOS). The (a) EFA and (b) PFA results on the Type C-2 testkey after +1.25kV CDM ESD stressing.

Through contact anomalies inspection and poly profile by High Acceleration Voltage (HKV) SEM, the damage spike towards gate oxide is clearly observed on the PMOS of the M+1th inverter (circuit schematic shown in Fig. 10), which serves the purpose of partially isolating the effect of the capacitive load [12]. Since the power-rail ESD clamp circuits are placed in the VDD1 power domain only, the long dissipation path of the ESD current during CDM ESD stress could induce a large potential difference across the interface circuits between the separated power domains, and therefore to cause gate-oxide damage on the interface circuits [13].

V. CONCLUSION

Three power-rail ESD clamp circuits with the corresponding test circuit splits have been fabricated in 0.18-μm CMOS process with 1.8-V devices to investigate their CDM ESD protection capability. With the calculations on turn-on resistance, voltage clamping-down time, and I_{t2} from VF-TLP measured I-V curves, the CDM ESD protection capability among the power-rail ESD clamp circuits can be quantitatively compared. The on-chip decoupling capacitor is very vulnerable to CDM ESD stress, so it is a good candidate as testing vehicle to investigate CDM ESD protection capability of the power-rail ESD clamp circuits. From the comprehensive testing results on the silicon chip, it has been confirmed that the power-rail ESD clamp circuits with the main ESD device (M_{ESD}) of the shortest channel length can perform the shortest voltage clamping-down time and smallest turn-on resistance, therefore to perform the best CDM ESD protection capability. Moreover, the power-rail ESD clamp circuit with the RC-INV-NMOS structure [7] has demonstrated a better CDM ESD protection capability among the three different power-rail ESD clamp circuits.

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