Received 21 September 2022; revised 16 November 2022; accepted 20 November 2022. Date of publication 24 November 2022; date of current version 21 February 2023. The review of this article was arranged by Editor S. Ikeda.

Digital Object Identifier 10.1109/JEDS.2022.3224206

Doping-Free Complementary Metal-Oxide-Semiconductor Inverter Based on N-Type and P-Type Tungsten Diselenide Field-Effect Transistors With Aluminum-Scandium Alloy and Tungsten Oxide for Source/Drain Contact

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This work was supported in part by JST CREST under Grant JPMJCR16F4; in part by JSPS Grant-in-Aid for Scientific Research under Grant 20K04616; in part by the Research Grant for Tokyo Tech Challenging Research Award; and in part by the Samco Foundation.

ABSTRACT In this study, we experimentally demonstrated concepts for realizing doping-free Tungsten Diselenide (WSe_2) complementary metal-oxide-semiconductor (CMOS) inverter by developing alloys and compound metals used as source/drain (S/D) contacts. Aluminum – scandium alloy (AlSc) and tungsten oxide (WO_x)-based S/D contacts enable efficient electron and hole injection into WSe_2 for n-type and p-type FET operation because the work function (WF) of AlSc and WOx are aligned to neighboring the conduction and valence band edge of WSe_2, respectively. A dual-gate bias architecture is used to improve electrical characteristics of FETs and enhance CMOS inverter performance after device fabrication. By utilizing AlSc and WO_x-based S/D contacts in conjunction with the dual-gate bias architecture, our fabricated WSe_2 CMOS inverter realized a higher gain at V_{dd} of 1 V or higher than those in the literatures. Furthermore, the fabricated WSe_2 CMOS inverter is operated at a power supply voltage (V_{dd}) of as low as 0.5 V. This study paves the way towards research and development of transition metal dichalcogenides-based devices and circuits.

INDEX TERMS 2D-FETs, CMOS inverter, doping-free, WSe_2.

I. INTRODUCTION

Semiconducting transition metal dichalcogenides (TMDCs) have been the focus of growing interest as channel materials in field-effect transistors (FETs) for next-generation low-power digital electronics [1]. Since a complementary metal-oxide-semiconductor (CMOS) inverter constructed using pairs of n-type and p-type FETs is a fundamental constituent in modern digital electronics [2], implementation of both n-type and p-type FETs based on semiconducting TMDCs is of particular importance [3]. The two-dimensional (2D) crystal nature of TMDCs provides dangling-bond-free surfaces and enables the manipulation of physical thickness down to

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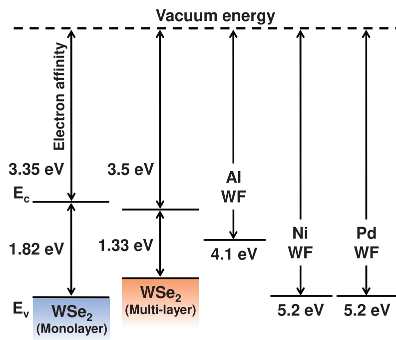

FIGURE 1. Band alignment of WSe_2 and several elemental metals.

a single layer with maintained high mobility of electrons and holes, which is in contrast to conventional bulk silicon (Si) channels [4]. Therefore, TMDCs are suitable for application in low-voltage CMOSFETs and energy-efficient digital electronics [5]. Among various semiconducting TMDCs, tungsten diselenide (WSe_2) is one of the strong candidates for application in CMOSFETs because of its ambipolar transport and high mobility of both electrons and holes [6], [7]. These notable features of WSe_2 make it highly attractive for use in the research and development of CMOSFETs.

One of the challenges is to develop an appropriate source and drain (S/D) contact for operation of both n-type and p-type FETs. Fig. 1 shows band alignment of WSe_2 and several elemental metals [8]. Note that multilayer WSe_2 is suitable as a component of S/D contacts compared with a single layer of WSe_2 [9]. Since the bandgap of WSe_2 decreases with increasing layer number, decreasing barrier height between metal and WSe_2 can be realized [8], [9]. As a result, an efficient carrier injection from S/D to WSe_2 and a higher drain current of FETs are attainable. As summarized in Fig. 1, the work function (WF) of S/D metals should be aligned to the vicinity of the conduction band minimum (CBM) and valence band maximum (VBM) for n-type and p-type operations, respectively [8]. For n-type FET operation, since CBM of multi-layer WSe_2 is quite small (3.5 eV), even with aluminum (Al), which is a representative low-WF metal (4.1 eV), corresponds to the midgap value of WSe_2 [8]. A metal with a lower WF than Al must be adopted for n-type FET operation, however, metals with WF less than 4 eV are chemically unstable, highly reactive, and easily oxidized [10]. It is thus necessary for operating n-type WSe_2 FET to find a metal with a lower WF than Al and has chemical stability. For p-type FET operation, VBM of multi-layer WSe_2 results in 4.83 eV because the bandgap of multi-layer WSe_2 is 1.33 eV [8]. At first glance, high-WF nickel (Ni) or palladium (Pd) is suitable for p-type FET operation, while ambipolar transport characteristics have been reported even in FETs with Ni and Pd as S/D contacts [11]. Therefore, it is important to develop appropriate S/D contacts for stable p-type WSe_2 FET operation.

The central idea and strategy of this study is to use alloys and compound metals in S/D contacts in WSe_2 FETs for n-type and p-type operations. Various material properties including WF, adhesion strength, and chemical stability may be artificially tailored by modulating the compositional ratio or preparation method for alloys and compound metals [12]. In this study, aluminum – scandium alloy (AlSc) is used in S/D contacts for n-type FET operation with WSe_2. In contrast to the single-element metals Al and Sc, alloyed AlSc was reported to remarkably improve material properties including low resistivity, high thermal stability, and high immunity to oxidation [13]. It is speculated that the WF of alloyed AlSc is lower than that of Al and is intermediate between those of Al (4.1 eV) and Sc (3.5 eV) [14]. On the other hand, tungsten oxide (WO_x), which is a transition metal oxide, is utilized as an S/D contact for p-type FET with WSe_2 in this study. WO_x has been adopted as hole-selective layer in photovoltaic devices because of its high work function ranging from 5.3 to 6.5 eV [15]. In addition, UV ozone oxidation of the WSe_2 surface was found to result in the formation of WO_x with high electrical conduction [16]. It can be hypothesized that the formation of WO_x at the WSe_2 surface is applicable to the formation of S/D contacts for p-type FET operation. In this study, we adopted a doping-free process for the fabrication of both n-type and p-type WSe_2 FETs because 2D crystals are basically incompatible with conventional ion doping technology owing to the restrictions of channel thickness and annealing temperature, which are not the case for bulk Si [17], [18]. The focus is on the fabrication and characterization of n-type and p-type WSe_2 FETs with AlSc and WO_x as the S/D contacts. Of particular interest in this study is on how these S/D contacts fabricated using AlSc and WO_x affect the electrical characteristics of WSe_2 FETs. The effectiveness of our approach is demonstrated in this study through the fabrication and characterization of devices.

II. DEVICE FABRICATION AND EXPERIMENT

The schematics of cross-sectional views of devices and the device concepts considered in this study are shown in Fig. 2. A 50-mm-thick WSe_2 was prepared by mechanical exfoliation. This prepared WSe_2 is thick enough to be regarded as bulk WSe_2 with a bandgap of 1.33eV. Conventional photolithography and etching methods were used for device fabrication, whereas the lift-off process was not utilized in this study. Although electrical characteristics of WSe_2 FETs with the back-gate architecture were mainly investigated, WSe_2 FETs with top-gate structure were also prepared for dual-gate operation that enables the modulation of device performance after device fabrication [19]. The fabrication process and optical images of fabricated WSe_2 FETs are shown in Fig. 3. A heavily doped p-type silicon substrate (p^+-Si) was thermally oxidized to form a 20-nm-thick silicon dioxide (SiO_2) gate dielectric for the back-gate architecture. Mechanically exfoliated WSe_2 was transferred to the substrate using a poly(dimethylsiloxane) (PDMS) elastomer and a micromanipulator [20]. Then, a 15-nm-thick Al_2O_3 layer

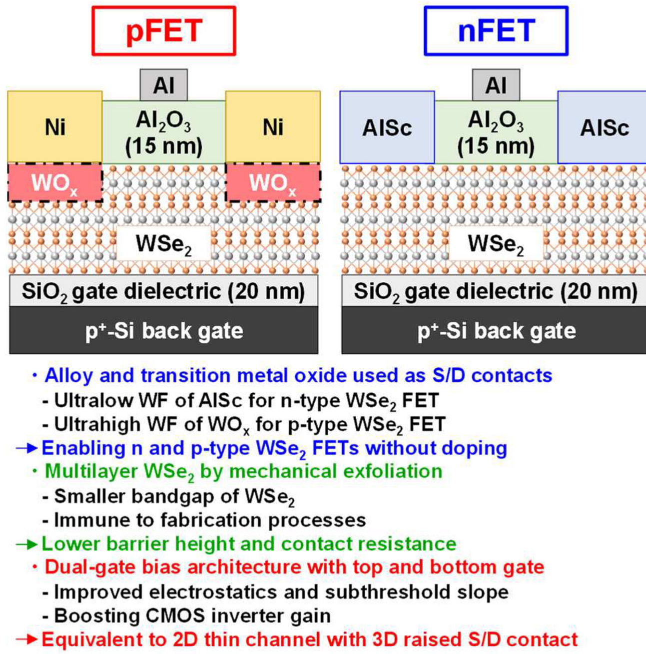

FIGURE 2. Schematic cross-sectional views and device concepts in this study.

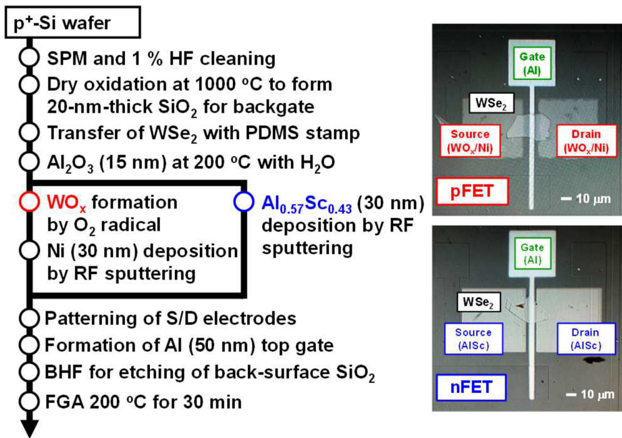

FIGURE 3. Fabrication process and optical image of fabricated WSe_2 FET.

was formed on the WSe_2 surface by atomic layer deposition (ALD) at 200 °C with H_2O as a passivation layer. Subsequently, a contact hole was opened to form the S/D contact. Next, AlSc (30 nm) was deposited by RF sputtering (RF power, 50 W, process pressure, 0.55 Pa, argon flow rate, 7 sccm, deposition rate, 1 nm/min) for n-type WSe_2 FET. The electrical resistance of deposited AlSc was 184 μΩ-cm. The sputtering target for the compositional ratio of $Al_{0.57}Sc_{0.43}$ was purchased from a commercial supplier. For p-type WSe_2 FET, WO_x was formed on the surface by radical oxidation (microwave power, 500 W, frequency, 2.45 GHz, process pressure, 0.025 Torr, oxygen flow rate, 10 sccm, room temperature, duration, 5 min), followed by Ni deposition by RF sputtering (RF power, 50 W, process pressure, 2 Pa, argon flow rate, 40 sccm, deposition rate, 1 nm/min). After the patterning of S/D electrodes, the Al topgate was fabricated on Al_2O_3. Finally, the devices were annealed at 200 °C in forming gas ($H_2 : N_2 = 3\% : 97\%$) for 30 min. The gate length between S and D (L_{bg}) was 25 μm and the length of the top gate (L_{tg}) was 5 μm. The gate width for n-type and p-type FET were estimated to be 19 μm and 26 μm by optical microscope, respectively. In this study, n-type and p-type FET were not integrated on same wafer but fabricated on individual substrates separately. Proposed fabrication process in this study is based on the deposition of passivation layer on WSe_2 surface, subsequent lithography, and etching of passivation layer for S/D contact hole opening, followed by S/D metal deposition. When the fabrication process of S/D contact for n-type FET is proceeding, WSe_2 channel for p-type FET is completely protected by deposited passivation layer. Moreover, this fabrication process does not require high temperature annealing. For future technology, this presented method is thus promising a way to fabricate both n-type and p-type WSe_2 FETs on the same wafer, simultaneously. The electrical characteristics were measured with a manual probe station in an atmospheric pressure without inert gas purge at room temperature using a precision LCR meter (Agilent E4980 A) and a precision semiconductor parameter analyzer (Agilent 4156 C).

III. RESULTS AND DISCUSSION

A. PROPERTIES OF ALSC AND WO_X FOR S/D CONTACTS

Firstly, the WF of $Al_{0.57}Sc_{0.43}$ was investigated using a MOS capacitor (MOSCAP) with a SiO_2 gate dielectric and an n-type Si substrate [21]. A flatband voltage (V_{FB}) of SiO_2/Si MOSCAP is fundamentally determined by the difference in between the WF of the metal gate and the Fermi level of the Si substrate because the effects of fixed charges in the SiO_2 gate dielectric and trap states at the SiO_2/Si interface on V_{FB} are negligibly small, less than 50 mV [2]. Consequently, V_{FB} can be expressed as [2]

$$V_{FB} = \phi_m - \phi_s \tag{1}$$

where ϕ_m is the WF of the gate metal and ϕ_s is the Fermi potential of the Si substrate. The Fermi potential ϕ_s of the Si substrate is defined as [2]

$$\phi_s = -\frac{E_f}{q} \tag{2}$$

where q is electronic charge and E_f is the Fermi level of Si. The Fermi level E_f of n-type Si is defined as [2]

$$E_f - E_i = kT \ln\left(\frac{N_{sub}}{n_i}\right) \tag{3}$$

where E_i is the intrinsic Fermi level, k is Boltzmann's constant, T is the absolute temperature, N_{sub} is the substrate impurity concentration, and n_i is the intrinsic carrier concentration [2]. The WF can be estimated by solving Eq. (1), Eq. (2) and Eq. (3) using measured V_{FB}. Fig. 4(a) shows bidirectional C–V characteristics of SiO_2/Si MOSCAP with

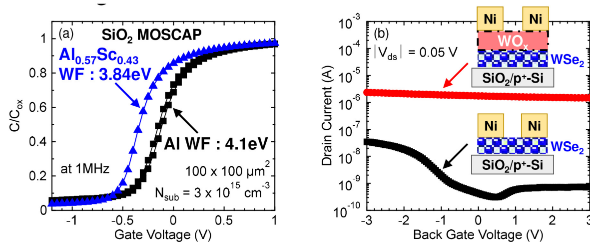

FIGURE 4. (a) Bidirectional C–V characteristics of SiO_2/Si MOSCAP with $Al_{0.57}Sc_{0.43}$ and Al gate. (b) I_d–V_g characteristics of WSe_2 FET with and without WO_x layer.

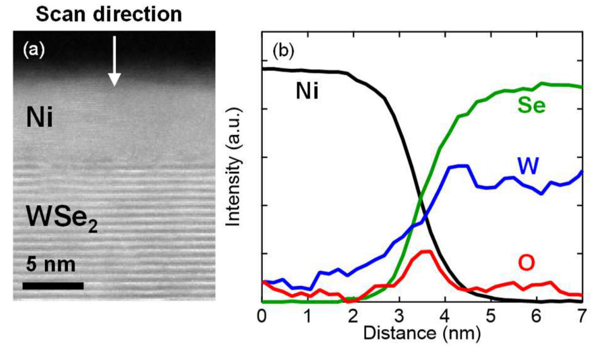

FIGURE 5. (a) TEM image and (b) Intensity profiles obtained by EELS of the $Ni/WO_x/WSe_2$ contact interface in p-type FET.

the $Al_{0.57}Sc_{0.43}$ gate. The C–V characteristics of the Al gate was also shown as a reference in Fig. 4(a). Observed hysteresis was less than 50 mV for both AlSc and Al gate. The substrate impurity concentration of n-type Si was 3×10^{15} cm^{-3}. The low-WF metal induces a negative V_{FB} shift of C–V characteristics and vice versa [21]. The C–V characteristics of the AlSc gate shifted to the negative direction compared with those of the Al gate. This finding indicates that the WF of the AlSc alloy is lower than that of Al metal. By solving (1), (2) and (3), the WF of $Al_{0.57}Sc_{0.43}$ was 3.84 eV. As mentioned in Introduction, the AlSc alloy has a lower WF than Al, which has a WF of 4.1eV. AlSc was found to be a peculiar metallic material that simultaneously satisfies the contradictory properties of being chemically stable and having a low work function. Note that the amount of oxygen inside AlSc depends on the compositional ratio of AlSc [22]. The amount oxygen inside AlSc increases with increasing Sc content and vice versa. Since the work function of AlSc also varied according to the compositional ratio, the modulation of compositional ratio involved in both residual oxygen content and the work function.

Next, the WO_x layer formed by radical oxidation was characterized with the back-gate FET. The transferred WSe_2 was exposed to oxygen radicals to form WO_x at the topmost WSe_2 surface. After that, Ni metal was deposited by RF sputtering to form S/D electrodes. Conventional WSe_2 without WO_x formed was also prepared as a reference. The effect of the WO_x layer on I_d–V_g characteristics is shown in Fig. 4(b). The ambipolar characteristic was observed in conventional WSe_2 FET without the WO_x layer, which is consistent with a previous report [11]. On the other hand, the drain current of FET with the WO_x layer is almost constant irrespective of back-gate voltage applied. This finding implies that the WO_x layer formed by radical oxidation shows highly doped degenerate semiconductor or metal-like conductivity [16]. The same experimental results were also obtained for UV ozone oxidation to form the WO_x layer on the WSe_2 surface [16]. Since WO_x was formed between WSe_2 and the Ni electrode in this study, the current should not flow from WSe_2 through WO_x to the Ni electrode if WO_x is not bulk-conducting. Consequently, bulk conduction within the WO_x layer is considered to be occurred.

Cross-sectional transmission electron microscopy (TEM) and electron energy-loss spectroscopy (EELS) were conducted to obtain detailed information on the S/D contact structure. Fig. 5(a) and (b) show the TEM image and the intensity profiles of various elements obtained by EELS analysis in the $Ni/WO_x/WSe_2$ contact interface of p-type FET. The profiled of four elements, namely, oxygen (O), tungsten (W), selenium (Se), and Ni, are presented in Fig. 5 (b) as a function of distance. The oxide layer can be clearly observed between Ni and WSe_2 channel. The film thickness of WO_x was estimated to be about 1.5 nm. Since WO_x was formed at room temperature and resultant thickness was a few nm, prepared WO_x is thought to be amorphous structure [23]. From TEM observation and EELS profiles, the WO_x/WSe_2 interface is considered to be a sharp interface. No structural transition layer was observed. According to a previous study of CIGS (copper indium gallium diselenide) solar cells [24], solid phase metal oxides are produced during the oxidation process of CIGS accompanied by the generation of gas phase SeO_2. Therefore, gas phase SeO_2 and solid phase WO_x are considered to be formed during the oxidation of WSe_2. In fact, no Se element was detected in the WO_x layer formed on the surface of WSe_2 by ozone oxidation [25], [26]. It was concluded that the WO_x layer was formed at the topmost part of the WSe_2 surface by radical oxidation.

B. CHARACTERIZATION OF FETS AND CMOS INVERTER

The most important experimental results to present our proof of concept in this study are shown in Fig. 6(a). Fig. 6(a) shows the back gate operation of I_d–V_g characteristics in WSe_2 FET with AlSc and WO_x S/D contacts. The ambipolar characteristic of the WSe_2 FET with the Ni S/D contact is also included as a reference. Both n-type and p-type WSe_2 FET operations were clearly demonstrated by applying AlSc and WO_x as the S/D contacts. Obtained threshold voltages for n-type and p-type FET were 0.3V and −1.1V, respectively. Since this study applied the same metal as gate electrodes to both n-type and p-type FET, the difference between threshold voltage of n-type and p-type FET reflects the bandgap of WSe_2. Actually, these difference in

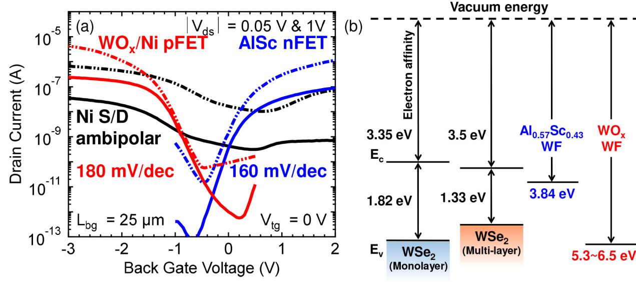

FIGURE 6. (a) Back gate operation of I_d–V_g characteristics in WSe_2 FET with AlSc and WO_x S/D contacts at $|V_{ds}|$ of 0.05 V and 1V. Ambipolar characteristic with Ni S/D contact was also shown. (b) Expected band alignment between WSe_2 and S/D contact metals with AlSc and WO_x.

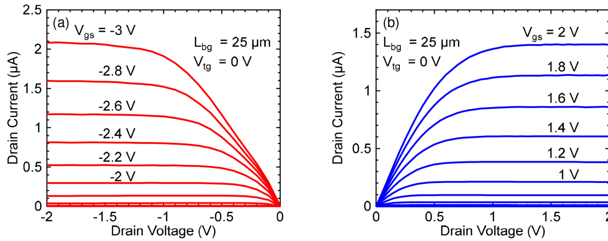

FIGURE 7. Back gate operation of I_d–V_d characteristics in WSe_2 FET with (a) WO_x and (b) AlSc S/D contacts.

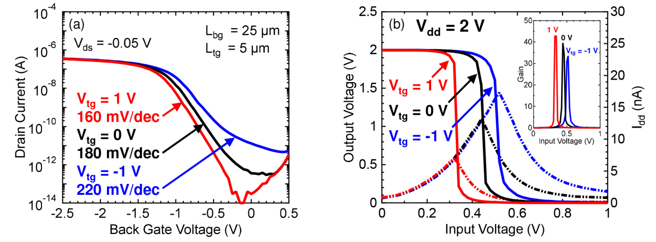

FIGURE 8. (a) I_d–V_g characteristics of p-type FET as a function of the back gate voltage for various top gate (V_{tg}) values of p-type FET. (b) Transfer characteristics of CMOS inverter as a function of the back gate voltage for various top gate (V_{tg}) values of p-type FET. CMOS inverter gain as a function of the back gate voltage for various top gate (V_{tg}) values of p-type FET is also shown in the inset of Fig. 7(b).

threshold voltage well coincides with the bandgap of WSe_2. Utilization of different gate metals is one of the promising approaches to attain the symmetric V_{th} between n-type and p-type FET. The extracted electron and hole mobility including contact resistance in the present WSe_2 are 10 and 23 cm^2/Vs, respectively. These results are almost consistent with previous study in [27]. The drain current of n-type FET is found to be lower than that of p-type FET. Fig. 6(b) shows expected band alignment between WSe_2 and S/D contact metals with AlSc and WO_x. The work function of WO_x was quoted from the reference [15]. As shown in Fig. 6(b), this lower drain current is considered to be associated with the larger barrier height of n-type FET with AlSc than that of p-type FET with WO_x. On the other hand, the subthreshold slope (SS) of p-type FET is degraded compared with that of n-type FET. This higher SS probably resulted from the difference in WSe_2 thickness since the SS increases with increasing thickness of the channel layer [28]. Representative I_d–V_d characteristics by back gate operation are shown in Fig. 7(a) and (b). The linear dependence of drain current at a low drain voltage was clearly observed, as shown in Fig. 7(a) and (b). These findings indicate that the AlSc and WO_x S/D contacts provide ohmic-like characteristics [21]. Fig. 6 and 7 demonstrate the effectiveness of the approach presented in this study.

As previously described, the dual-gate bias architecture enables the modulation of electrical characteristics even after device fabrication [19]. Fig. 8(a) shows the I_d–V_g characteristics of p-type FET as a function of the back gate voltage for various top gate (V_{tg}) values. As shown in Fig. 8(a), the threshold voltage (V_{th}) and SS were controllable after device fabrication owing to the dual-gate bias architecture [19]. Degradation of SS for pFET was improved by applying the appropriate top-gate voltage [19].

As a result, SS of p-type FET was recovered and became identical to SS of n-type FET for 160 mV/dec. This improvement of SS by applying the positive bias at top gate results from the increase in depletion layer width underneath the top gate. This increase in depletion layer width corresponds to the decrease in the physical thickness of the channel layer [28]. Since the Al top gate was formed without any overlap between the gate electrode and the S/D contacts, this structure is similar to that of the Silicon on Thin Box (SOTB) MOSFET with a raised S/D region [19]. It is quite important to investigate the characteristics of CMOS inverters because both n-type and p-type WSe_2 FET operations were demonstrated. Fig. 8(b) shows the transfer characteristics of the CMOS inverter as a function of the back gate voltage for various top gate (V_{tg}) values of p-type FET. Note that the top gate voltage for n-type FET was fixed to 0 V to maintain the SS of 160 mV/dec in n-type FET. Operation of the CMOS inverter was clearly observed with the fabricated n-type and p-type WSe_2 FETs. The through current in the CMOS inverter (I_{dd}) and the CMOS inverter gain as a function of top gate voltage for p-type FET are also shown in Fig. 8(b) and its inset, respectively. The gain of the CMOS inverter can be estimated as Gain $= dV_{out}/dV_{in}$ [2]. The reduction of I_{dd} and the increase in gain were demonstrated in these experiments. These results are attributed to the improvement of the subthreshold characteristics of p-type FET by applying the positive bias at top gate and the resultant symmetric I_d–V_g characteristics of n-type and p-type FET. The dual-gate bias architecture enhances the performance of the CMOS inverter after device fabrication. These improvement and enhancement cannot be realized with back gate alone. Fig. 9(a) and (b) show the transfer characteristics and the gain of CMOS inverter as functions of power supply voltage (V_{dd}), respectively. The operation of the CMOS inverter was observed at V_{dd} of as low as 0.5 V, as shown in Fig. 9(a) and (b), which was realized

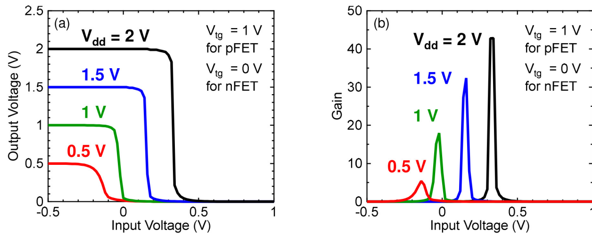

FIGURE 9. Transfer characteristics and (b) gain of CMOS inverter as functions of power supply voltage (V_{dd}).

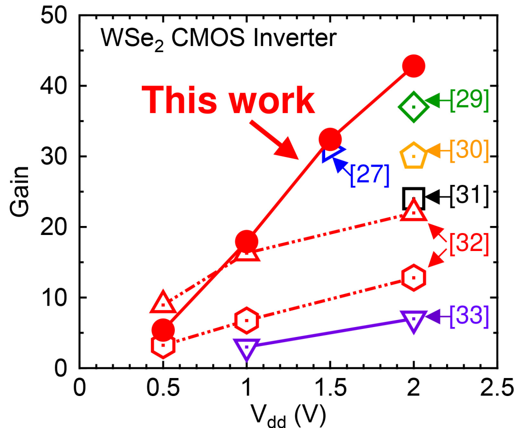

FIGURE 10. Gain as a function of supply voltage (V_{dd}) of fabricated WSe_2 CMOS inverter in this study along with other those of WSe_2 CMOS inverters from the literatures.

by developing the alloy and compound-metal-based S/D contacts.

Finally, gain as a function of supply voltage (V_{dd}) of fabricated WSe_2 CMOS inverter in this study along with other those of WSe_2 CMOS inverters from the literatures as comparisons are shown together in Fig. 10 [27], [29], [30], [31], [32], [33]. Our fabricated CMOS inverter was found to attain a higher gain at V_{dd} of 1 V or higher than those in the literatures. On the other hand, the gain of the CMOS inverter was limited to 5 at a low V_{dd} of 0.5 V and was lower than that of our previous work [32]. This small gain is associated with the 20-nm-thick SiO_2 layer of the back-gate structure. Note that CMOS inverter characteristics can be further improved by establishing the appropriate compositional ratio and preparation method for alloys and compound metals for S/D contacts in WSe_2 FETs. In particular, the AlSc alloy with higher Sc concentration is anticipated to show a WF lower than 3.84 eV of $Al_{0.57}Sc_{0.43}$, resulting in a higher drain current of n-type FET owing to the decreased barrier height. These are the issues that remain to be addressed in our future work.

IV. CONCLUSION

In this study, we demonstrated the concepts for realizing doping-free WSe_2 CMOS inverters with alloys and compound metals used as S/D contacts. The use of AlSc and WO_x-based S/D contacts resulted in the operation of both n-type and p-type WSe_2 FETs. FET characteristics including in V_{th} and SS were electrically tunable by using the dual-gate bias architecture after device fabrication. By using the established S/D contact and dual-gate bias architecture, we experimentally demonstrated the operation of CMOS inverter with high gain. Moreover, the fabricated WSe_2 CMOS inverter was operated at a V_{dd} as low as 0.5 V. This study opens up interesting directions for research and development of TMDC-based devices and circuits.

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