Received 12 October 2022; revised 20 November 2022; accepted 21 November 2022. Date of publication 24 November 2022; date of current version 21 February 2023. The review of this article was arranged by Editor G. I. Ng.

Digital Object Identifier 10.1109/JEDS.2022.3224500

Suppression of Kink in the Output Characteristics of AlInN/GaN High Electron Mobility Transistors by Post-Gate Metallization Annealing

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This work was supported by the Centre for NEMS and Nanophotonics (CNNP), Indian Institute of Technology Madras.

ABSTRACT In this paper, we report the effect of post-gate metallization annealing on the performance of GaN-based High Electron Mobility Transistors (HEMTs). The performances of HEMTs annealed at 200 °C (HEMT1) and at 400 °C (HEMT2) for 5 minutes in N_2 ambient are compared. While there is a kink in the output characteristics of HEMT1, there is no such kink in the output characteristics of HEMT2. The kink is attributed to impact ionization in the GaN channel. Surface and interface traps of HEMT1 increase the peak electric field at the drain side gate edge and cause impact ionization. The post-gate metallization annealing at a higher temperature reduces the surface and interface traps, which reduces the peak electric field in HEMT2 and suppresses impact ionization. This is substantiated by TCAD simulations. Threshold voltage instability on the application of negative gate bias stress was also examined for these devices. A positive shift in threshold voltage was observed in HEMT1 on the application of negative gate bias stress, whereas the corresponding shift was negative in HEMT2, indicating the presence of two different types of traps in HEMT1 and HEMT2.

INDEX TERMS HEMT, impact ionization, floating source, negative gate bias stress, traps.

I. INTRODUCTION

GaN-based High Electron Mobility Transistors (HEMTs) are suitable for high-power [1], [2] and high-frequency [3], [4] applications because of the wide band gap of GaN [5] and high electron velocity in the channel [6]. To be suitable for high-power applications, GaN-based HEMTs should be able to withstand high drain voltage in the off-state. To design high-power GaN-based HEMTs, it is imperative to understand the breakdown mechanism of the devices. Impact ionization is one of the reasons for the breakdown of semiconductor devices. Though the occurrence of impact ionization in GaN is debatable due to its high bandgap [7], [8], several research groups have presented the evidence of impact ionization in GaN-based devices [9], [10], [11], [12]. Impact ionization in GaN-channel causes a premature breakdown of the device [13]. In some devices, impact ionization manifests as a "kink" in the output characteristics [9], [12] for drain biases greater than the bandgap of the GaN channel [9]. While the kink in the output characteristics is visible at room temperature in some devices, it is visible only at cryogenic temperature in other devices. Brar et al. [9] observed kink at room temperature, and the kink amplitude increased at lower temperatures. On the other hand, Bisi et al. [12] observed kinks in the output characteristics of N-polar GaN MIS-HEMTs only at cryogenic temperatures. For their devices, the impact ionization rate at room temperature is not sufficient to create kinks in the output characteristics. At cryogenic temperature, the mean free path of electrons increases, which helps in gaining sufficient energy for impact ionization. As a result, the impact ionization rate increases at cryogenic temperature, and kinks in the output characteristics become visible. The origin of

the electrons causing impact ionization could either be the source or the gate through the leakage path in the barrier. Wang and Chen [14] have shown that the origin of electrons for the impact ionization is the source rather than the gate. The design of high voltage HEMT should consider the suppression of impact ionization at the channel by reducing source injected electrons into the channel in the off-state and by reducing the electric field, particularly at the drain-side edge of the gate. The reduction in the electric field at the gate edge can be achieved either by using field plates [1], [15], [16] or by using surface passivation [17]. Usually, in GaN-based HEMTs, the donor-like surface states become positively charged by donating electrons to the 2DEG. It is reported in the literature that with the increase in the surface donor concentration, the surface potential increases, which increases the electric field at the gate edge [18]. The surface states and different interface states can be reduced by performing a Post-gate Metallization Annealing (PMA) at a relatively high temperature (∼400-500 °C) [19], [20].

Various groups have reported different effects of PMA on device performance, e.g., improvement in the drain current ON/OFF ratio and subthreshold swing of Schottky gate HEMTs [21], removal of shallow traps with a shorter time constant, and introduction of deep traps with a longer time constant [22], positive shift in threshold voltage due to the reduction of the electron density at the channel [23] as well as an increase in the Schottky barrier height and reduction in the gate leakage current [24]. Calzolaro et al. [25] showed that the combination of surface preconditioning and post-gate metallization annealing reduced the interface traps and improved threshold voltage instability under positive gate bias stress in AlGaN/GaN MIS-HEMTs. However, in none of these studies, the effect of PMA on the impact ionization in the channel of GaN-based HEMTs was addressed.

In this paper, for the first time, we show that PMA at a higher temperature suppresses the kink effect in the output characteristics of AlInN/GaN-based Schottky gate HEMT. As already mentioned, PMA reduces the electric field at the gate edge by reducing the surface/interface states. This reduction in the electric field due to PMA is responsible for the suppression of the kink effect by reducing the probability of impact ionization.

II. DEVICE FABRICATION

The wafers with $Al_{0.83}In_{0.17}N$/GaN heterojunction used in this study are commercially available from the Novagan Corporation, Switzerland. The different layers on the SiC substrate were grown by Metal-Organic Chemical Vapor Deposition (MOCVD), as shown in Fig. 1. The source and the drain ohmic contacts were formed by depositing Ti/Al/Ni/Au (30/140/40/100 nm) metal stack and annealing at 810 °C for 60 seconds. Mesa isolation was performed by Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) to an etched depth of 200 nm. The gate length of 250 nm was defined by electron beam lithography, and a Ni/Au (30/80 nm) gate metal stack was deposited. For the contact pad metals, 40/100 nm of Ni/Au was used. In this study, we have fabricated HEMTs on two samples of the same wafer. HEMT1 had gone through PMA at 200 °C for 5 minutes, while HEMT2 had gone through PMA at 400 °C for 5 minutes. The devices under test have a gate length (L_G), gate width (W), source-to-gate spacing (L_{SG}), and gate-to-drain spacing (L_{GD}) of 250 nm, 55 μm, 2 μm, and 2 μm, respectively. The schematic cross-section of the device is shown in Fig. 1.

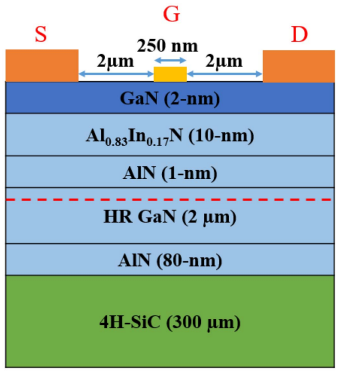

FIGURE 1. Schematic cross-section of the GaN-based HEMT on silicon carbide substrate.

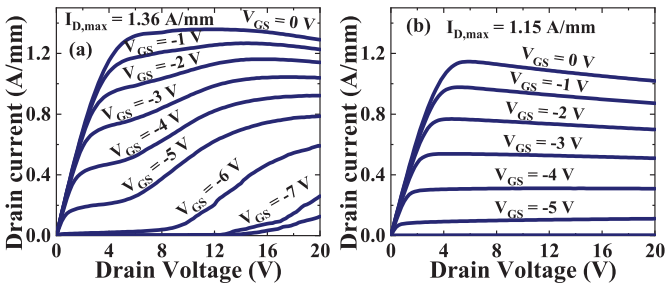

FIGURE 2. Output characteristics of (a) HEMT1: annealed at 200 °C and (b) HEMT2: annealed at 400 °C.

III. RESULTS AND DISCUSSION

The output characteristics of the devices under test at room temperature are shown in Fig. 2. At a gate-to-source voltage (V_{GS}) of 0 V, the maximum saturation drain current ($I_{D,max}$) of HEMT1 is 1.36 A/mm and of HEMT2 is 1.15 A/mm, respectively. The on-state resistances (R_{ON}) of HEMT1 and HEMT2 at a drain-to-source voltage (V_{DS}) = 1 V and V_{GS} = 0 V are 2.76 Ω-mm and 3.03 Ω-mm, respectively. The output characteristics of HEMT2 (Fig. 2b) are almost ideal, and there is no kink. But a significant kink is observed in the output characteristics of HEMT1 (Fig. 2a) for $V_{DS} \geq 6$ V.

Different research groups have extensively studied the kink effect in the output characteristics of GaN-based HEMTs [9], [12], [26], [27]. It has been suggested that there are two reasons for the kink, namely (a) detrapping of electrons from the deep levels [26], [27], and (b) generation of electron-hole pairs due to band-to-band impact ionization [9], [12]. In the case of (a), hot electrons knock out trapped electrons from the deep levels increasing the channel conductivity, and the

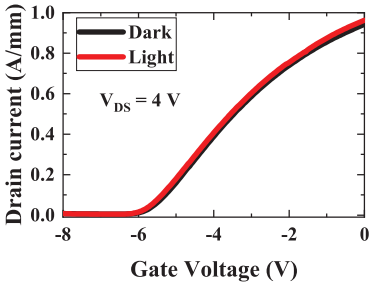

FIGURE 3. Transfer characteristics of HEMT1 measured in the pre-kink region (V_{DS} = 4 V) in the dark (black) and under illumination by an incandescent lamp (red).

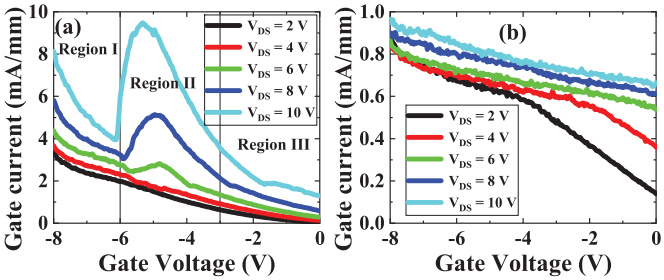

FIGURE 4. I_G-V_{GS} characteristics of (a) HEMT1, and (b) HEMT2 for different V_{DS}.

kink becomes visible in the output characteristics. However, trapping/detrapping of electrons is usually a slow process, and the kink in the output characteristics is visible only when a slow drain voltage sweep rate (less than 0.2 V/s) is applied [27]. For a fast sweep rate of the drain voltage, the kink is visible only in the first sweep, and consecutive sweeps do not show any kink. On the other hand, in our case, the output characteristics were taken with a drain voltage sweep rate of 6.5 V/s with a 20 ms delay between two consecutive gate voltage measurements. Such a fast sweep rate does not allow deep traps sufficient time to release and recapture electrons. In order to ensure that the detrapping of electrons from the deep levels is not the reason for the kink in HEMT1, transfer characteristics were measured in the pre-kink region in the dark condition and under constant illumination by an incandescent lamp (Fig. 3). Meneghesso et al. [26] reported that under illumination by an incandescent lamp, the pinch-off voltage shifts towards the positive direction due to enhanced trapping of electrons. From Fig. 3, we can see that there is no significant shift in the threshold voltage of HEMT1 under illumination. Meneghesso et al. [26] observed kink for all the gate voltages (even at V_{GS} = 0 V). However, in our case, kink amplitude is maximum at V_{GS} = –5 V and diminishes at V_{GS} = 0 V. So, unlike them, we cannot attribute detrapping of electrons from the deep levels as the reason for the kink in HEMT1. The probable reason for the kink in the output characteristics of HEMT1 may be impact ionization. The impact-generated holes reduce the source-to-channel barrier by accumulating at the source side of the gate. As a result, a sudden increase in the drain current is observed [9].

In order to find out whether impact ionization is occurring in HEMT1 or not, gate current (I_G) was measured as a function of V_{GS} for different V_{DS} values, and the measurement results are shown in Fig. 4. The gate current of both HEMT1 and HEMT2 are high. The gate current in AlInN/GaN HEMTs is usually higher than their AlGaN/GaN counterparts due to a thinner barrier layer and high electric field in the barrier layer due to higher polarization charge [28]. The higher I_G in HEMT1 compared to HEMT2 could be due to the presence of traps in the access region. In Fig. 4, a bell-shaped nature is observed in the I_G-V_{GS} characteristics of HEMT1, which is absent in HEMT2. For lower values of V_{DS} (< 6 V), I_G of HEMT1 decreases with an increase in V_{GS} (Fig. 4a). However, for higher values of V_{DS} (≥ 6 V), three distinct regions exist. Region I (V_{GS} ≤ –6 V): I_G decreases with an increase in V_{GS}. Region II (–6 V < V_{GS} < –3 V): I_G increases with V_{GS}, becomes maximum at V_{GS} = –5 V, and then starts decreasing. Region III (V_{GS} ≥ –3 V): I_G again decreases with an increase in V_{GS}. The bell-shaped nature of I_G was also observed by other research groups, and the reason was attributed to impact ionization in the channel [9], [11], [29], [30]. In region I, where V_{GS} is less than the pinch-off voltage of HEMT1, sufficient electrons are not there in the channel to initiate impact ionization. As a result, I_G reduces as V_{GS} increases from –8 V to –6 V. In region II, when the device is in the semi-on state condition, the product of channel electron concentration and the lateral electric field is high. The electrons gain sufficient energy from the lateral electric field and initiate impact ionization. The impact-generated electrons are collected by the drain. Some of the impact-generated holes accumulate below the gate, while some holes are collected by the gate. As a result, I_G increases. The hole current is maximum at V_{GS} = –5 V, where the impact ionization rate is maximum. In region III, the electron concentration is high, but the electric field is low. In addition, higher electron concentration increases the carrier-carrier scattering and decreases the electron mean free path. As a result, impact ionization is negligible in this region. On the other hand, as shown in Fig. 4b, for all values of V_{DS}, I_G of HEMT2 monotonically decreases as V_{GS} increases from –8 V to 0 V. For a certain V_{DS}, as V_{GS} increases from –8 V to 0 V, $|V_{GD}|$ decreases. As a result, the electric field at the drain-side gate edge reduces, which reduces I_G. I_G increases with an increase in V_{DS}, as higher V_{DS} increases the electric field at the drain-side gate edge.

To check whether impact ionization is indeed responsible for the bell-shaped nature of the I_G-V_{GS} curve of Fig. 4, floating source measurement of I_G was carried out [30]. In this experiment, I_G was measured as a function of the gate voltage (V_G) while the source terminal was kept floating. Fig. 5 shows the I_G-V_G characteristics of (a) HEMT1 and (b) HEMT2 for different drain voltages (V_D) with floating source. Comparing Fig. 4a and Fig. 5a, we can see that the bell-shaped nature of the gate current of HEMT1 is completely absent for all values of V_D in the floating source condition. It is reported in the literature that a high electric

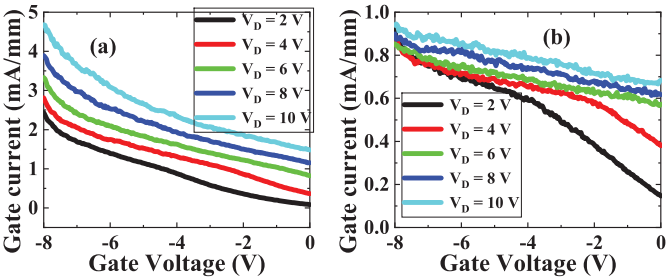

FIGURE 5. I_G-V_G characteristics of (a) HEMT1, (b) HEMT2 with a floating source condition.

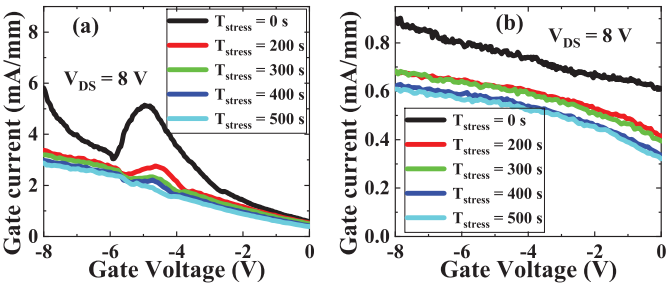

FIGURE 6. I_G-V_{GS} characteristics of (a) HEMT1, and (b) HEMT2 at V_{DS} = 8 V with different negative gate bias stress time.

field between the gate and drain alone is not sufficient for impact ionization. There should also be the injection of source electrons into the channel to be accelerated by the lateral electric field to become hot electrons [30], [31], [32]. As already mentioned, the bell-shaped nature of I_G in Fig. 4a is due to the impact-generated hole current in addition to the electron current. In the floating source condition, there is no impact ionization due to the absence of the source electrons and hence no extra hole current. Therefore, in this condition, I_G of HEMT1 in Fig. 5a monotonically decreases as the gate voltage increases from –8 V to 0 V. On the other hand, comparing Fig. 4b and Fig. 5b, we can see that there is not much difference in the I_G of HEMT2 between the grounded source condition and the floating source condition. This is because, in both these cases, there is no impact ionization at the channel of HEMT2.

The observation so far suggests that the impact ionization is taking place in HEMT1. However, impact ionization at such a low V_{DS} in a wide band gap material, like GaN, is questionable. So to find out the role of access region traps in impact ionization, I_G as a function of V_{GS} was measured for different negative gate bias stress time (T_{stress}) as shown in Fig. 6. The negative gate bias stress was applied at $V_{GS} = -8$ V and $V_{DS} = +8$ V for a duration of T_{stress}. Immediately after T_{stress}, I_G was measured as a function of V_{GS}. Throughout the stress time and the measurement time, the source terminal was grounded. From the I_G-V_{GS} characteristics of HEMT1 with different stress times (Fig. 6a), we can see that along with the reduction in I_G with the stress time, the bell-shaped nature of I_G also reduces and ultimately vanishes at $T_{stress} = 500$ s. The low annealing temperature of HEMT1 is insufficient to reduce the surface and the interface traps. The donor-like surface traps become positively charged by donating electrons and raise the potential of the access region. As a result, the electric field at the drain-side gate edge increases. Since the concentration of access region traps in HEMT1 is usually higher, even at a relatively lower drain-to-source voltage ($V_{DS} = 6$ V), the electric field at the drain-side gate edge becomes sufficiently high to create hot electrons resulting in impact ionization. As the stress time increases, more electrons are captured by the access region traps, lowering the access region potential. As a result, with the increase in stress time, the impact ionization rate and hence the bell-shaped nature of the I_G-V_{GS} curve reduces and ultimately disappears for $T_{stress} = 500$ s. From Fig. 6b, we can see that I_G of HEMT2 also decreases as the stress time increases from 0 s to 500 s. Though the high annealing temperature (400 °C) of HEMT2 has significantly reduced the surface and interface traps, some traps may still exist in the access regions. Filling of the access region traps with electrons reduces I_G by reducing the electric field at the drain-side gate edge.

From the stress measurement, it is clear that the donor-like surface traps play a significant role in the impact ionization of HEMT1. In order to verify our speculation that the surface states accelerate impact ionization by increasing the electric field at the drain-side edge of the gate, TCAD simulations of the devices under test were performed, which give a deeper insight into the electric field distribution along the channel. To do so, we calibrated the simulation with experimental DC transfer characteristics. In the simulation, we used the inbuilt polarization model to consider the effect of polarization charges in GaN-based materials. A surface donor density of 3.8×10^{13} cm^{-2} was considered with an energy level of 0.4 eV below the conduction band. The unintentional buffer doping was set to be 1×10^{15} cm^{-3}, while an acceptor trap concentration of 3×10^{16} cm^{-3} was considered in the GaN buffer to get a good match. The work function of the Schottky gate was set to be 4.4 eV, while non-local electron tunneling was activated to make the source and drain contacts ohmic. To match the characteristics of HEMT1, we used donor traps with a density of 7×10^{19} cm^{-3} at an energy level of 0.2 eV below the conduction band in the GaN cap layer, while in the case of HEMT2, we used donor traps with a concentration of 1×10^{17} cm^{-3} at the same activation energy as HEMT1. We kept all the parameters of HEMT1 and HEMT2 the same and varied only the concentration of donor traps in the GaN cap layer to get a good match. The drift-diffusion equations were solved along with the physical model, viz, doping and high field-dependent mobility, thermionic emission, Shockley-Read-Hall (SRH) recombination, and Fermi statistics. The simulated electric field under the gate of HEMT1 (solid line) and HEMT2 (dotted line) at $V_{GS} = -5$ V, and $V_{DS} = 2$, 4, 6, 8, and 10 V are shown in Fig. 7. While the maximum electric field at the drain side edge of the gate of HEMT1 varies from 0.94 to 2.1 MV/cm, for HEMT2, it ranges from 0.26 to 0.52 MV/cm. The simulation shows that PMA at 400 °C significantly reduces

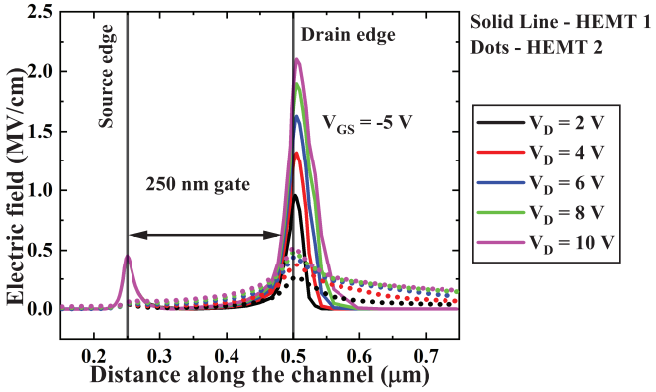

FIGURE 7. Electric field distribution of HEMT1 (solid line) and HEMT2 (dotted line) under the gate.

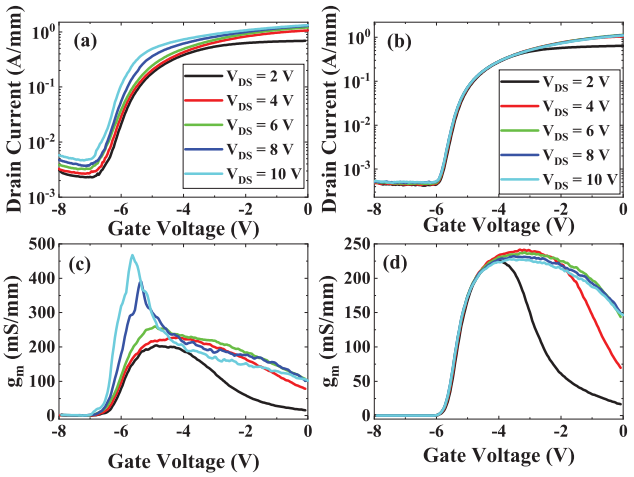

FIGURE 8. Transfer characteristics of (a) HEMT1 and (b) HEMT2; transconductance of (c) HEMT1 and (d) HEMT2.

the electric field and hence suppresses impact ionization in HEMT2.

Fig. 8 shows the transfer characteristics of (a) HEMT1 and (b) HEMT2. The threshold voltage of HEMT1 shifts towards the negative direction with an increase in the drain voltage (Fig. 8a), while the threshold voltage of HEMT2 hardly changes within the limits of the measurement (Fig. 8b). These results indicate a much better gate control in HEMT2 than in HEMT1. Moreover, we can see a sharp spike in the transconductance of HEMT1. This is because the impact-generated holes lower the source-to-channel potential barrier and suddenly increase the drain current at $V_{GS} = -5$ V, where the impact ionization rate is maximum. This sudden increase in the drain current of HEMT1 manifests itself as a spike in the transconductance. Such a spike is absent in HEMT2, as there is no impact ionization.

The threshold voltage instability of the devices under test was examined on the application of negative gate bias stress at a biasing condition of $V_{GS} = -8$ V and $V_{DS} = 100$ mV for 100 s (Fig. 9). The threshold voltage was extracted using the linear extrapolation method [33]. The unstressed threshold

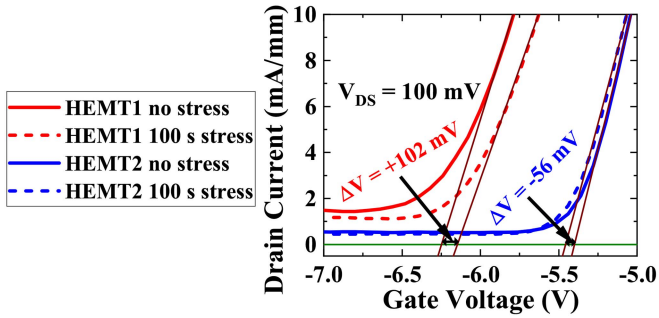

FIGURE 9. Threshold voltage shift due to negative gate bias stress at $V_{GS} = -8$ V and $V_{DS} = 100$ mV for 100 s.

voltages of HEMT1 and HEMT2 are –6.30 V and –5.45 V, respectively. PMA at higher temperatures removes shallow traps from the Ni/AlInN interface and introduces deep traps, which are usually filled with electrons [22]. The filled deep traps deplete electrons from the channel below the gate and shift threshold voltage towards the positive direction. On application of negative gate bias stress, the threshold voltage of HEMT1 shifts towards the positive direction by 102 mV, and that of HEMT2 shifts towards the negative direction by 56 mV from the unstressed condition. This indicates the presence of two different types of traps in HEMT1 and HEMT2. The stressing condition of this experiment is usually not favorable for buffer-related trapping/detrapping [34]. So the stress-induced trapping/detrapping must be due to the traps at the gate metal/barrier layer interface and/or in the AlInN barrier layer and/or AlInN/GaN interface. When a negative gate bias stress is applied in HEMT1, the shallow interface traps below the gate accept electrons and become negatively charged, which deplete electrons from the 2DEG and shift the threshold voltage towards the positive direction. On the other hand, when a negative gate bias stress is applied in the off-state of HEMT2, detrapping of electrons occurs from the deep levels [35]. In order to maintain the charge neutrality under the gate, the 2DEG concentration increases, and the threshold voltage of HEMT2 shifts towards the negative direction.

IV. CONCLUSION

Effects of the post-gate metallization annealing on the performance of the AlInN/GaN-based HEMTs have been studied. Kinks are observed in the output characteristics of the devices where PMA is carried out at 200 °C. From the bell-shaped nature of the gate current characteristics and floating source measurements, it is inferred that the kink is due to impact ionization. Unpassivated positively charged traps at the access region increase the electric field at the drain side gate edge and the probability of impact ionization. It is shown that annealing at a higher temperature (400 °C) suppresses the kink in the output characteristics by reducing the surface and interface traps and, consequently, the electric field. This is confirmed through TCAD simulations. Annealing at a higher temperature also

reduces the shift in the threshold voltage with increasing drain-to-source voltage. This study shows the importance of post-gate metallization annealing for better performance of the HEMTs.

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