Guest Editors' Introduction: Special Issue on Design and Test of Multidie Packages

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In 2017, *IEEE Design&Test* published a special issue on "3D-TEST" (referring to both the workshop with that name, as well as the topic), featuring three articles on various test-related issues of the AMD Radeon R9 Fury, a marvel of multidimensional packaging. Since then, the market has lurched tentatively in the same direction. Expectations were high for single-tower many-die stacks, but the realities of power and thermal issues still hold that promise at bay. Slowly, the market has been tackling each obstacle placed in front of it. Once thought to be a mere stepping-stone to true 3D-IC stacking, side-by-side stacking onto an interposer has created its own place on the product roadmaps and is here to stay. The word "chiplet" has yet to claim space in the dictionary, but chiplets (dies meant to be stacked as part of a larger chip) are front and center in advanced chip design projects. Placed upon passive or active interposers, these building blocks enable the path to heterogeneous integration: architecting submodules of a package with various technology nodes, and therefore with just the right balance of performance and cost. The debate has shifted to interchiplet communications. HBI+ and OpenHBI, ultra-short reach(USR)/extra-short reach (XSR), and the nascent Universal Chiplet Interconnect Express (UCIe) interface are battling for the structured high-speed interconnect market. Certainly, memory stacking has won with high bandwidth memory (HBM) stacks seen on several production devices.

But the devil is in the details. Test for manufacturing defects is a largely solved problem, but the word is leaking out slowly. IEEE Std 1838 has delivered on its promise of connecting test infrastructure up and down the stack and across the interposer—defining the hardware necessary to achieve this goal. The article "Applying IEEE Test Standards to Multidie Designs" by McLaurin and Cron brings in a host of other IEEE standards that help a user bridge the automation gap between implementation and integration of tooling and tester.

Many EDA tools on the market today support IEEE Standards to improve flow interoperability as a design moves from the development phase to high-volume manufacturing. In "Affordable and Comprehensive Testing of 3-D Stacked Die Devices" by Côté et al., many facets of automation of multidie packaged products are discussed from an EDA perspective.

While through-silicon via (TSV) manufacturing has advanced to a point where their yield is quite

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acceptable, the bonding of dies through microbumps still needs some yield improvement. Yet, testing these connections can only be done postbond. Two articles, "A Global Self-Repair Method for TSV Arrays With Adaptive FNS-CAC Codec," by Wei et al. and "Broadcast-TDMA: A Cost-Effective Fault-Tolerance Method for TSV Lifetime Reliability Enhancement," by Ni et al., present redundant interconnect as a potential yield-enhancing solution. ■

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