Interview

An Interview With Professor Chenming Hu, Father of 3D Transistors

Yao-Wen Chang
National Taiwan University

Yao-Wen Chang, IEEE Design and Test of Computers Interviews Editor, spoke with the Father of 3D Transistors Dr. Chenming Hu at National Taiwan University, on 22 September 2016.

Prof. Chenming Hu and the interviewer, Prof. Yao-Wen Chang (photo taken on 22 September 2016 at National Taiwan University)

The D&T interview editor, Yao-Wen Chang, had a great chance to interview world-renowned Prof. Chenming Hu, the Father of 3D Transistors, between his two invited talks held at the Graduate Institute of Electronics Engineering of National Taiwan University in Taipei, Taiwan, on 22 September 2016. In this interview, Prof. Hu shared with our D&T readers the motivations and properties of the FinFET transistor, some key technology needs for semiconductors, his insightful tips on innovation, and his inspiring suggestions to researchers.

Before this interview, the Editor prepared over 20 questions and also called for questions from experts in the field. So for each question, we credit the individuals who proposed the question. As a result, totally 19 questions and their answers are compiled in this interview article. We hope that our D&T readers will enjoy this interview. Thank you!

Dr. Chenming Hu has been called the Father of 3D Transistors for developing the FinFET in 1999. Intel was the first company to use FinFET in 2011 production, calling it the most radical shift in semiconductor technology in over 50 years. By 2015 all top servers, computers, Android, and iOS phones use FinFET processors. He received the National Technology and Innovation Medal from President Obama in the White House in 2016. The world's largest technology association IEEE called him "Microelectronics Visionary" when presenting him the 2009 Nishizawa Medal for "achievements critical to producing smaller yet more reliable and higher-performance integrated circuits." The 2011 Asian American Engineer of the Year Award cited his industry-standard transistor model "used in designing IC products with cumulative sales of many hundreds of billions of dollars." The 2013 Kaufman Award noted his "tremendous career of

Digital Object Identifier 10.1109/MDAT.2017.2729511
Date of publication: 24 July 2017; date of current version: 13 September 2017.

2168-2356/17 © 2017 IEEE Copublished by the IEEE CEDA, IEEE CASS, IEEE SSCS, and TTTC

creativity and innovation that fueled the past four decades of the semiconductor industry." The U.S. Semiconductor Industry Association lauded his research leadership for the "advancement of the electronics industry and of our national economy."

He is TSMC Distinguished Professor Emeritus in the Graduate School of University of California, Berkeley, Board Director of Ambarella and Inphi, and Chairman of the Nonprofit Friends of Children with Special Needs. From 2001 to 2004, he was the Chief Technology Officer of TSMC, the world's largest dedicated integrated circuits manufacturing company. He was the Founding Chairman of Celestry Design Technologies until its acquisition by Cadence Design Systems.

Prof. Chenming Hu received the National Technology and Innovation Medal from President Obama in the White House in 2016. (Courtesy of the Associated Press.)

Part I: Questions on IC technologies

Yao-Wen Chang: How did you come up with the idea of FinFETs? (Similar questions were also provided by Prof. Jiang Hu of Texas A&M University and Prof. Chien-Mo Li of National Taiwan University.)

Chenming Hu: In a 1999 Science article published by Intel authors, it was said that MOSFET scaling would end because of the following three limits:

- gate oxide thickness,
- junction depth, and
- dopant density fluctuation.

At that time, people generally believed that the gate oxide thickness should scale linearly with the channel length because gate capacitance (inversely proportional to gate oxide thickness) should be larger than drain capacitance (inversely proportional to channel length) for the gate to control the switching operation of a transistor. For the 35-nm technology, as a result, we would have needed to reduce the gate oxide thickness to 0.5 nm which is equivalent to about one SiO_2 module thickness. So the 1999 ITRS Roadmap presented no solution for transistor scaling beyond the 35-nm technology node. It is still true that the gate oxide thickness is limited to 0.5 nm, but it is not true that the gate oxide thickness needs to scale with the channel length.

In the same year, we published our FinFET transistor of 45-nm gate size with better $I_d - V_g$ and $I_d - V_d$ characteristics than then-130-nm MOSFET, showing that the gate oxide thickness does not need to scale with the channel length, neither does channel doping concentration nor the junction depth. At that time, we had an observation that even with very small gate oxide thickness, there could still be significant leakage current in the body along the path between source and drain below the semiconductor/insulator interface at a depth that is about 1/4 of the gate length, so small gate oxide thickness is really not effective for stopping this subsurface leakage current. (See Figure 1a for the traditional FET structure with a leakage path between source and drain.) Instead, our underlying idea is to develop a thin body FET so that no semiconductor is far from the gate to reduce leakage current effectively. (See Figure 1b for a thin body FET.)

For our 1999 FinFET transistor, the gate oxide thickness is 2.7 nm, much larger than the 0.5-nm limit. There is no body doping, so the problems with random doping fluctuation can be eliminated. In particular, the subthreshold swing is only 69 mV/decade, much smaller than 100 mV/decade for the then-planar MOSFET and close to the thermal limit of 60 mV/decade. [See Figure 2 for a FinFET transistor with such a structure change, and Figure 3 for the $I_d - V_g$ (left) and $I_d - V_d$ (right) characteristics of the first FinFET transistor with 45-nm gates published in the paper: X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEEE International Electron Devices Meeting Technical Digest*, pp. 67–70, 1999.]

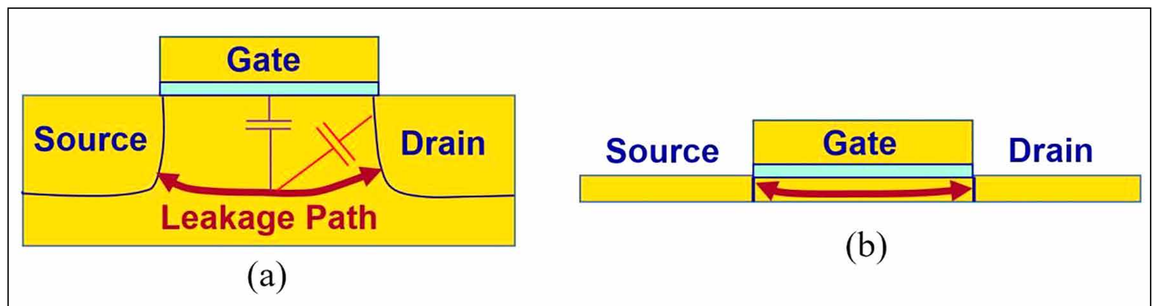

Figure 1. Transistor structures. (a) Traditional FET structure. (b) Thin body FET structure.

Chang: What are the key features to make FinFET a dominating technology for advanced IC designs? (Similar questions also provided by Prof. Jiang Hu of Texas A&M University and Prof. Chien-Mo Li of National Taiwan University.)

Hu: Traditionally, the IC technology relies on scaling to achieve desired power, performance, and cost benefits because of smaller capacitance and resistance and higher packing density with a scaled device. When continued scaling becomes more difficult, it is desirable to develop different techniques to achieve the same benefits at reasonable costs. The FinFET technology allows scaling to continue and provides additional benefits with a disruptive transistor *architecture*. For a FinFET (see Figure 2b), for example, the FET gate wraps around three sides of the transistor's channel, forming a fin shape. The vertical fins (and thus transistors) can intrinsically be packed closer, leading to higher packing density which is particularly suitable for dense designs such as SRAM layouts. By increasing the heights of the fins, the FinFET can use a smaller layout area to a given channel width and performance than the traditional MOSFET. Furthermore, the manufacturing cost for the FinFET transistor can be kept reasonable because no extra mask is needed to make the silicon fin. Also, the FinFET channel is well controlled and does not need heavy doping; as a result, it is less sensitive to random dopant fluctuations. So with its better power/performance behaviors, short-channel-effect control and scalability, the FinFET transistor has become the most promising alternative for advanced IC technology.

Chang: How does FinFET achieve better power/performance benefits? (Similar questions were also provided by Dr. Kai-Yuan Chao of Intel and Prof. Yuan Xie of UCSB.)

Hu: Different from the traditional MOSFET architecture, the FinFET transistor has a channel that is not defined by the doping underneath the channel, but rather by physical boundaries, where the depletion zone fills the entire body of the transistor. This

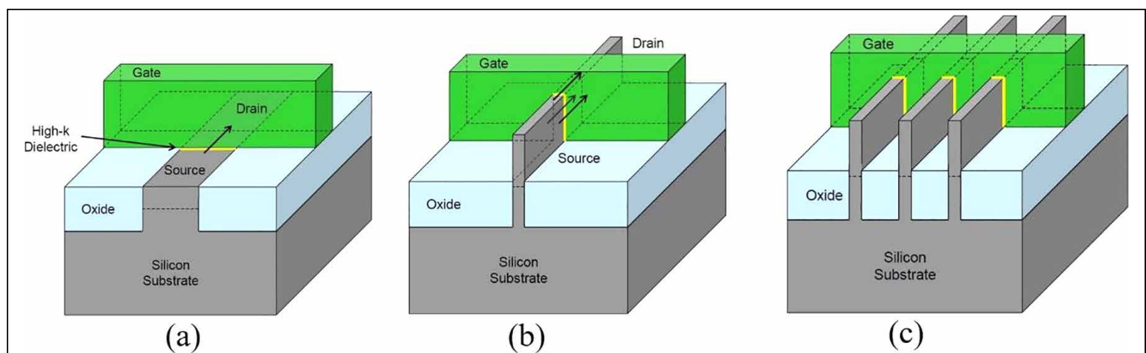

Figure 2. Planar transistor and 3D FinFETs. (a) Planar transistor: A 2D planar transistor forms a conducting path between the source and drain under the gate when it is "ON." (b) A 3D FinFET (tri-gate) transistor forms a conducting path on three sides of a vertical fin. (c) 3D FinFET with three fins to increase the total drive strength for higher performance. (M. Bohr and K. Mistry, "Intel's Revolutionary 22-nm Transistor Technology," May 2011. See http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-details_presentation.pdf.)

design improves gate control over the conducting channel, so only very little current is allowed to leak through the body when the transistor is turned off. The FinFET transistor can also be operated at a lower voltage for a given leakage current, substantially reducing its dynamic power consumption because the transistor can have a lower threshold voltage for the same leakage, facilitating low voltage operation.

Chang: What are your suggestions for dealing with the potential challenges on self-heating, variability, and miller capacitance for the FinFET technology? (**Self-heating:** prior work by Scholten *et al.* in IEDM 2009 shows about 40 °C higher temperature over the planar MOSFET. **Variability:** FinFET may suffer from line and fin edge roughness-based process, voltage, and temperature variation with scaling. **Miller capacitance:** The 3D nature of the fins causes higher gate capacitance, which affects miller capacitance and thus its stage delay.)

Hu: I am not familiar with the report of 40 °C higher temperature over the planar MOSFET. Perhaps 40 °C higher was reported under DC bias at high I_d and high V_d and the power consumption, $I_d * V_d$, is in the *mW* range. A real circuit containing one billion FinFETs may consume a watt, so each transistor consumes one billionth of a watt on average. That is many orders of magnitude less than *mW*. Of course IC designers should be concerned about hot spots, and EDA design tools are available for catching them. For example, the FinFET SPICE model, BSIM-CMG, that we developed at UC Berkeley includes self-heating. The situation is no different than designing a planar MOSFET IC.

FinFET introduces a fin structure and related variability issues. They are more addressable by the smart processing and equipment engineers than the random dopant variability and the gate length variability issues of the planar MOSFET at 14 nm. Otherwise, companies would not have replaced planar MOSFET with FinFET for new technology nodes.

FinFET increases the Miller capacitance, so it may not be the choice for RF centric chips. In the future, I expect that FinFET device design and FinFET RF design to both become better and FinFET SOC integration with RF will be common.

In all these three areas, continuing process technology improvement, accurate device models, and good design tools and flows are needed.

Chang: What are the impacts of the FinFET technology on EDA?

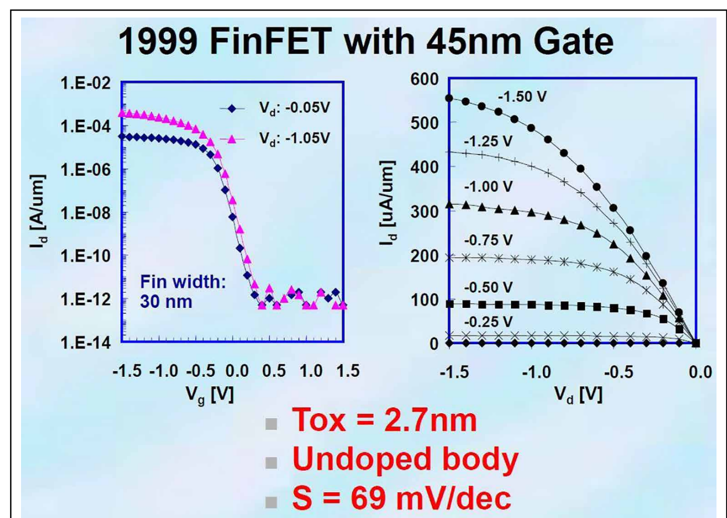

Figure 3. The I_d–V_g (left) and I_d–V_d (right) characteristics of the first FinFET transistor with 45-nm gates published in 1999.

Hu: Many key stages of our current EDA tool chain would be significantly impacted, including transistor-level process modeling and simulation, mask synthesis and production, physical layout design, RC extraction, and verification. New tools have been developed to best consider and utilize the FinFET technology such as its ultralow leakage currents and voltages, its quantized channel widths and layout structures (fin width, height, and pitch), and so on. This has been a welcome boost of business to the EDA industry. We at UC Berkeley have developed the SPICE compact model for FinFET and for gate-all-around (GAA) transistors, BSIM-CMG, and provided it for free to the world as the industry standard SPICE model that provides the link, or the language for communication, between the two halves of the semiconductor world—the fab/device half and the EDA/design half.

Chang: What is next after FinFET?

Hu: Many innovations are needed to further improve the IC technologies after FinFET. The thin body FET has become the concept that guides future CMOS transistor structure evolution. Future devices with tall fins, GAA, thin film (such as Ultra-Thin-Body FET developed at UC Berkeley in 2000, also known as fully depleted silicon on insulator, FD-SOI), and thin wires (pillar FET, nanowire FET, and so on) would be candidates of future thin body transistor technologies. For an ultimate thin body FET, a monolayer of 2D semiconductor (such as MoS_2, WSe_2, C,

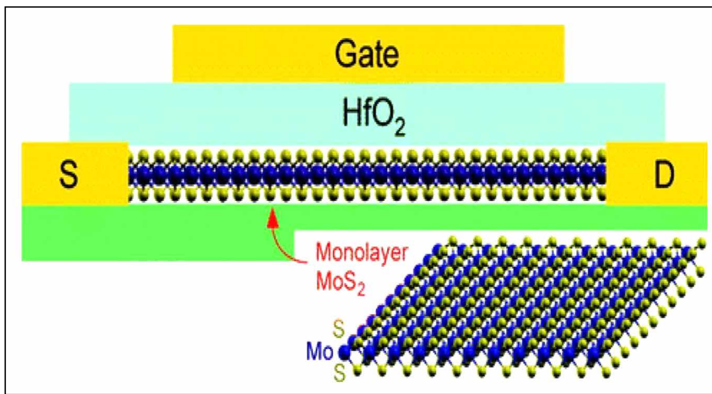

Figure 4. An ultimate thin body FET with a monolayer of MoS_2.

P, and so on) is a promising channel material. They do not have any surface bonds and may be grown by chemical vapor deposition on amorphous dielectric surface. (Figure 4 illustrates an ultimate thin body.) To break the 60 mV/decade switching limit of MOSFETs (and BJT, diode, and so on), nanoelectromechanical switches (NEMSs), tunnel transistors, negative-capacitance transistors (by amplifying the applied gate voltage), and spintronics have shown promises. To lower the cost, improve power/speed and packing density, monolithic 3D stacked ICs, EUV, and directed self-assembly (DSA) are at varying stages of R and D. There are many technology challenges and opportunities after FinFET to further advance the semiconductor industry.

Chang: People are talking that Moore's Law is dead. But we believe (hope) the scaling can continue, even at a slower rate. What are your comments? (Provided by Professor Bei Yu of the Chinese University of Hong Kong and Dr. Kevin Chao of Intel.)

Hu: It depends on what you think Moore's Law is. If you are talking about the single transistor size, there is surely intrinsic physical limit. Current state-of-the-art transistor lengths are of only tens of atoms, so we are close to that limit. Nevertheless, I would not say it is "dead," but scaling will gradually slow down. In a more general sense, Moore's Law is about improving power, speed, density, and cost. Can we further improve power, speed, density, and cost without relying on transistor and interconnect scaling? I think so, but it would need many innovative ideas and continuous hard work.

Chang: What would be the alternatives to continue performance/power scaling after transistor stops shrinking? (Provided by Prof. Yuan Xie of UCSB.)

Hu: Performance/power needs continuous improvement through innovations beyond classical transistor scaling, such as smart transistor structures, 3D stacking, power reduction through NCFET, tunnel FET and NEMS, and so on, new physical principals, materials, computing architectures, and systems. These new technologies, together, will provide continued performance/power improvement. As an example, dynamic power is given by $P = CV_{dd}^2 f/2$. We could reduce C by constructing air gaps between device components and f by applying architecture solutions such as multi-cores. For V_{dd}, we have $I_{ds} \alpha \mu (V_{dd} - V_t)$. We could reduce $V_{dd} - V_t$ with high mobility material such as strained Si, Ge, III–V, and CNT. To Reduce V_t, we can use tunneling or the negative-capacitance concept. In short, we have many alternatives other than transistor scaling to continue to improve performance/power to the end of this century.

Chang: What is the best material or interconnect (manufacturing or design) to cope with the fast increasing resistance with transistor scaling? (Provided by Dr. Kai-Yuan Chao of Intel.)

Hu: I do not have a clear picture, but I like the thought of graphene and carbon nanotubes. The most challenging problem is the resistance at the interfaces between different materials. Some breakthrough is needed here.

Chang: What are the main current research opportunities in semiconductor?

Hu: Let me address this question from five aspects:

- Transistor: as traditional scaling becomes more and more difficult, more attentions should be paid on new architectures, materials, and physics for breakthroughs.
- Low RC: RC reductions for interconnects, contacts, and devices and new architecture remain key issues for further power/performance improvement.
- Low cost: continued cost reductions through true 3D integration, new lithography technologies such as DSA, and so on, are crucial.
- Coinnovation: device, circuit, and architecture coinnovations are needed to advance the semiconductor industry (this will provide many cross-disciplinary research opportunities for academia).
- Value: higher value creation through more-than-Moore techniques, big-data applications, new business models, and so on, would be needed for a healthy semiconductor industry.

Chang: What are your concluding remarks on current IC technology research needs?

Hu: Past IC technology advancement relies mainly on scaling, which will inevitably slow down due to physics limits. Nevertheless, power-speed-cost-value will continue to improve through innovations. The world will need more and more smart technologies, and only IC technology can enable them—but future IC devices, materials, architectures and systems may be very different from today's. The differences will result from many decades of gradual evolution rather than an abrupt reorganization of the IC industry.

Part II: Questions on innovation

Chang: What is the secret of your innovative mind? (Question provided by Prof. Chien-Mo Li of National Taiwan University.)

Hu: Don't be afraid of failures. It is good for a researcher to face difficult challenges. As the saying goes, "When the going gets tough, the tough get going." Difficulties create opportunities for innovation. There are always needs for technology breakthroughs, even when someday we do not use semiconductors to make ICs, we still need ICs to keep the world going. Future technology challenges could be huge, but the rewards for technology innovation would be even greater.

Chang: Could you please share with our D&T readers your tips for innovation?

Hu: Innovation is a problem-solving and confidence-building process. Problem solving is a skill that can be learned and improved, so innovating skill can be learned and improved, too. Here are my four tips for innovation for whatever they are worth:

- Understand the problem: We need to REALLY understand the problem and why other solutions are not good enough before looking for new innovative ideas.
- Study successes: It is often fruitful to learn from the experiences and examples of success to create new success.
- Pick problems that have impact: If you are going to spend time solving a problem, you might as well pick a problem whose solution would make a large impact.
- Pick problems with a right time frame: Aiming too far in time and too out of the box may not be desirable unless you do not care whether your good idea can be implemented or not.
- Innovation requires passion. Remember the wise words of Thomas Edison, "Genius is one percent inspiration and 99 percent perspiration."

Chang: How to solve impactful problems?

Hu: We first need to cultivate both deep domain and broad knowledge, so we really need to study hard in school and out of it. To solve problems with big impacts, we must have the confidence to take on big problems. We build up our confidence through small successes of increasing sizes.

Chang: What role should universities play for innovation?

Hu: In my view, universities are great places to produce occasional innovations. More importantly, universities play a pivotal role in cultivating knowledgeable, confident, and passionate students those later make innovations in industry. The innovations in industry are much more numerous but more private and less talked about, but they are the engine of economic growth and deserve to be praised more. So in this regard, universities are one of the most critical links for creating innovations.

Part III: Other questions

Chang: You started up Celestry Design Technologies, Inc. in 1996 as its chairman (acquired by Cadence in 2003), became the CTO of TSMC 2001–2004, and is a Board Member of SanDisk since 2008 (and also Ambarella and Inphi). What are your suggestions for academia-industry collaboration to achieve the best benefits to our own research, our semiconductor industry, and society? (A similar question about how to keep a good balance between academia and industry was also provided by Prof. Bei Yu of the Chinese University of Hong Kong.)

Hu: It is important to leverage the strengths from both sides to achieve a higher goal. The cost of research failure and the pressure of outcome delivery (time-to-delivery) in academia are typically much lower than those in industry, and academia has a stream of new blood in students who have passion and dare to experience failures (as the saying goes, "the deaf is not afraid of thunders"). So it is easier for academia to try out crazy ideas. On the other hand, industry often has better resources (such

as funding), clearer focus in research directions and understanding of applications, and valuable expertise in design and development. Academia and industry should help each other to create win-win.

Chang: The silicon semiconductor industry started in the US, but now has largely moved to other geographies—especially on the manufacturing side. Will the future of this industry be like that of the US Auto Industry? What are the major factors of such move and the impacts on the future semiconductor development? Any suggestions under such trend? (A similar question was also provided by Dr. Sani Nassif of Radyalis.)

Hu: Still, Tesla was started in the US and other new “auto” companies are being started in the US. The fact is that the US used to have 100% of world’s semiconductor manufacturing, and it should not be surprising that the market share has moved around, first to Japan, then South Korea and Taiwan. Next will be China and perhaps India. The semiconductor industry is large. No single region can expect to be the biggest in manufacturing, IC design, equipment, and innovation, at least not for long. When I grew up in the 1960s, the U.S. did much to help the underdeveloped countries and to make the world more equal. The world has become more equal and will be even more so, thanks to the good will of men.

Chang: You received a B.S. degree from National Taiwan University (NTU) and an M.S. and a Ph.D. from UC-Berkeley. What are your most unforgettable things during these school days? Any particular reasons that guided you to the semiconductor research? Any suggestions to those juniors for their study at school? Any special training required for a college/graduate student?

Hu: During my undergraduate study at NTU, the solid training on mathematics and physics was critical for my research career. Most importantly, the self-confidence and positive attitude built up, then, has supported me to face challenges and explore new things. At Berkeley, I was introduced to the world of semiconductor by Dr. Frank Fang of IBM and a Visiting Professor at NTU for six months. I was lucky to have attended both universities and be given the chance to meet and learn from smart people such as Andrew Grove. Luck or Karma is definitely a part of it all. So, study hard, build confidence, and be lucky.

Chang: What are your advices to young researchers? Any particular suggestions for those working on semiconductor?

Hu: Be focused on the field you choose and do your work with passion. There are lots of wonderful things yet to be done in semiconductor. ■

Acknowledgments

The interview editor would like to thank Prof. Chenming Hu for his insightful answers and in-depth explanations to the interview questions and his careful revision to the article. He would also like to thank Dr. Kai-Yuan Chao, Prof. Jiang Hu, Prof. Chien-Mo Li, Dr. Sani Nassif, Prof. Yuan Xie, and Prof. Bei Yu for providing their interesting questions for this interview.

Yao-Wen Chang is an IEEE Fellow and is currently Deputy Vice President for Academic Affairs of National Taiwan University (NTU) and Distinguished Professor of the Department of Electrical Engineering of the same university. He serves as the Vice President of Conferences of the IEEE Council on EDA. He has co-edited one textbook on electronic design automation and co-authored one book on routing and over 270 ACM/IEEE conference and journal papers in these areas, including a few highly cited works on floorplanning, placement, routing, manufacturability, and FPGA. His current research interests include physical design and manufacturability for integrated circuits. Dr. Chang received four awards at the 50th DAC in 2013 for the First Most Papers (34 DAC papers) in the Fifth Decade, and so on. He is a first-place winner of six recent EDA contests. He has receive eight Best Paper Awards (most recently from DAC 2017) and 24 Best Paper Award nominations from EDA top conferences. He has received many prestigious awards, including the Distinguished Research Award (highest honor) from the Ministry of Science and Technology of Taiwan (three times), the IBM Faculty Awards (three times), MXIC Chair Professorship, the Distinguished Teaching Award (highest honor) from NTU, and so on. He has served as the steering committee/general/program chairs of ISPD, and general/program chairs of ICCAD, and program chair of ASP-DAC and FPT, and on the IEEE CEDA Executive Committees for six years. He is a co-founder of the Maxeda Technology, Inc.

■ Direct questions and comments about this article to Yao-Wen Chang, Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan; email: ywchang@ntu.edu.tw.