ICCAD Roundtable

The Many Challenges of Triple Patterning

More and more techniques are being used to go down the Moore's law curve to smaller dimensions while being stuck at the same 193-nm wavelength light source, and multiple patterning methods are chief among them. This roundtable discusses the move from double patterning to triple patterning and beyond. What is the status of triple patterning today, and what does it really solve? At what dimension will it show its benefit? Will quadruple patterning be next, and when? How does multiple patterning fit in with a roadmap that includes extreme ultraviolet (EUV), direct write, and directed self-assembly? The panelists discuss the state of the art and future challenges.

Design & Test thanks the roundtable participants: moderator William Joyner (SRC), Jamil Kawa (Synopsys), Lars Liebmann (IBM), David Z. Pan (University of Texas at Austin), and Martin Wong (University of Illinois at Urbana-Champaign). *D&T* gratefully acknowledges the help of David Yeh (SRC), our Roundtables editor, who also participated in the event.

■ **William Joyner: Thank** you all for participating. We are here to discuss what problem triple patterning will solve, and when we will need it. One of the speakers at the ICCAD "Triple Patterning: Triple the Trouble?" session said, "Well, the 28-nm node is fine with single patterning; then at 20 nm, we need double patterning; at 14 nm, we need triple patterning; and at 10 nm, we may need quadruple patterning." So what is the status of triple patterning? What problems do you think it is going to solve?

Lars Liebmann: When will we need triple patterning? To answer this question, we first need to discuss node nomenclature and 193i resolution limits. It is public knowledge that the 14-nm node uses a minimum wiring pitch of 64 nm. Our unwavering commitment to well-established scaling laws dictates that 10 nm is somewhere around 45 nm, and 7 nm will be around 32 nm. The practical 1-D pitch resolution of 193i lithography has been agreed to be around 80 nm. As a final data point: multiple exposure patterning techniques that rely on interdigitating gratings run out of steam pretty quickly below 50–45 nm—this is due to overlay control rather than fundamental diffraction limits. These simple boundary conditions put the 14-nm node squarely into the LELE (i.e., double patterning) domain.

The 10-nm node is already dangerously close to the overlay-induced resolution limit of double patterning, meaning that back-end-of-line wiring levels benefit substantially from sidewall-image-transfer-based frequency multiplication techniques to reduce the risk of dielectric breakdown. These sidewall image transfer techniques (or self-aligned double patterning techniques, as some call them) are notoriously difficult to implement for bidirectional design levels. To accommodate aggressive 2-D design scaling for lower metal levels and local interconnect levels litho-etch-litho-etch (LELE) continues to be used. The challenge with LELE at the 10-nm node (other than the risk of overlay-induced errors) is that the interaction range between features that must be placed onto different masks grows significantly versus 14 nm—in reality, the interaction

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range stays fixed relative to 14 nm, but we pack more design features into that same space. This, in turn, causes more features to interact, which causes more odd cycles and forces either more restrictive design or the introduction of a third color. In summary, triple patterning does not provide a pitch resolution benefit over double patterning (i.e., LELELE versus LELE); it provides better 2-D scaling and a more flexible design environment.

And so, what we are calling the 10-nm node is where we are introducing triple patterning on several levels—not to get to a tighter pitch, but to maintain the 2-D scaling: to get the tip-to-side, tip-to-tip kind of resolution in addition to the pitch scale, and to get the densities. We cannot just keep dividing 80 by an arbitrary integer and then keep getting better and better resolution. That is not going to work in the physical world.

Joyner: I would like to ask our university colleagues, who are working with people from industry as well, the same thing: What problems do you think triple patterning might solve, and when will it be needed?

Martin Wong: I agree with Lars: so far, triple-patterning lithography (TPL) is not being used yet, so the earliest entry point is likely going to be the 10-nm node. I also agree that the main reason we need TPL is because DPL has a lot of these cycles, where we have stitches and overlay, and so on. So I think the main thing is to resolve these odd cycles.

We did an investigation of this, in fact, in 2012. We basically looked at multiple patterning. Even at 14 nm—if the router is aware of TPL, and the router is also aware of DPL—if we optimize at the routing level, we can see a tremendous difference in a number of stitches. So if we scale it to go down to the 10-nm node, the benefit would be tremendous. On the other hand, of course, at 10 nm, there may be other choices besides multiple patterning.

Joyner: Well, that's what I wonder. Let's let David and Jamil comment on that, and then maybe we can look at what other choices we see down the road.

David Z. Pan: From a simplistic perspective, the single-pitch, single-exposure, single-patterning limit is about 80-nm pitch. So for anything less than that we have to use double or multiple patterning. For double patterning, ideally we can achieve 40 nm in pitch, but in practice, maybe 50 nm, when we consider all those overlays. To get tight pitches and resolve conflicts, we have to go beyond double patterning—for example, triple patterning or quadruple patterning.

A couple years back, I heard an eye-opening talk by Intel's Senior Fellow Yan Borodovsky, who was giving a talk about future developments in multiple patterning—double patterning, triple patterning, quadruple patterning, or even double-quadruple (2×4) patterning, triple-triple (3×3) patterning, and so on. Of course, this was on the theoretical side as the relative overlay could be too high, and the costs would probably make it impractical. But, still, one of the main goals of multiple patterning is to make the pitch tighter. That has been the driving force of Moore's law. How much tighter really depends on the overlay control and so on.

Liebmann: Yes, to overcome the overlay-induced resolution limit and go below 50–45-nm pitch we would have to go to a self-aligned double patterning approach or a sidewall image transfer approach, as we call it in IBM. Basically, we're building up a mandrel feature: a topography feature as a way to deposit sidewalls.

We can repeat that process several times. We can do a self-aligned double patterning, self-aligned quadruple patterning—people talk about self-aligned octuplet patterning. You can keep adding sidewalls onto these sidewalls, and they're fairly well controlled. Then, we have to cut these gratings into useful shapes. Now this whole game starts over again, where we can have a single exposed cut mask, we have a double-pattern cut mask—we can use a triple-pattern cut mask. So the number of exposures certainly will continue to increase, but what I was saying is the fundamental pitch of litho-etch-litho-etch—we're not going to push it much below 45–50 nm.

Jamil Kawa: Lars summed it very nicely in terms of allowing the cell density to be very dense; the first metal layer, in particular, has to be multidirectional. So sidewall image transfer is not an optimal or a fully feasible solution for that problem. There is no alternative—if you're going to minimize the end-line tip to end-line tip spacing and have dense cells—than to have litho-etch-litho-etch-litho-etch. And, because of overlay problems, the theoretical pitch you are capable of with just double patterning is around 36 nm, with a k1 factor of below 0.25. The bottom line is to alleviate the overlay problems, alleviate odd cycles, and come up with dense patterns.

Joyner: When will we start quadruple patterning, do you think? Is it going to be litho-etch-litho-etch-litho-etch-litho-etch? Or is it going to be a different approach?

Liebmann: If we do the simple math of starting with 80 at 22, then 10 nm is right at that 40-nm pitch boundary. So a 7-nm node would have to be achieved with extreme ultraviolet (EUV) lithography or something other than just double patterning. It's not going to be litho-etch to the *n*th power. It's going to be a sidewall image transfer type approach—probably self-aligned quadruple patterning with cut mask.

Pan: For 7 nm, if we have to use quadruple patterning, it will most likely be, as Lars mentioned, self-aligned quadruple patterning.

Kawa: In its raw form? Or a combination of self-aligned double patterning plus litho-etch-litho-etch as a combination? With respect to the way that you raised the classic question of litho-etch-litho-etch to the power of four: the cumulative inaccuracies introduced by alignment make it infeasible or impractical. The question I want to pose is, how does everybody at this table feel about what Lars alluded to, which is complementary patterning in a way of using a combination of sidewall image transfer plus EUV, plus perhaps e-beam direct write?

Liebmann: I'm still a little worried. You know, I've of course seen Yan's presentations many times, and we had the lithography workshop last week. Intel seems to be very confident that they can go to self-aligned quadruple patterning to get to this sub-40-nm regime by a large margin. But the resolution of the cut mask is not so much the issue; it's the alignment.

If we're now doing, say, 28 nm, that would be exactly 40 times 0.7, so that would be the exact scaling point. We have a 14-nm-wide sidewall that we have to land the cut mask on.

You know, a ±5-nm overlay tolerance is quite phenomenal. So now 10 nm of those 14 are gone, and we'd have to control the dimensions of that cut mask to ±2 nm. Otherwise, it will fall off either side and either cut into the neighboring metal line or leave some metal where we really want insulator. So the tolerance on this cut mask, before we even worry about, "How dense can I pack them?" is going to be very, very challenging.

Just in placing things, so that they cut the lines that we want to cut without cutting the neighboring lines is going to be very difficult. I haven't seen any real tricks to make a self-aligned cut mask. If academia were looking at researching this, it would be fantastic if we could get self-aligned cut masks.

Wong: So I assume when we get down to 7 nm, we use self-aligned quadruple patterning (SAQP). We will be printing dense lines. We're not printing 2-D features. So if we're printing dense lines, when we're doing the cut mask, some overlay issues may not be that significant. The end is a line tip, so if there is some variation, it may not affect that much: we're not going to have something along the edge of the line.

So because now we're talking about dense lines, variations there would be okay. But as to how to print this cut mask: then we would probably have to, as you pointed out earlier, go to double patterning. Or maybe we could go to e-beam or EUV and some complementary technology. In fact, when we go down to that level, we may be using EUV to print the guiding templates, and then use directed self-assembly (DSA) to print some final features. It's also a possibility—if EUV and DSA become a reality at that point—that we can use complementary lithography technology when we go even further down, below 7 or so.

Joyner: It seems like we have been waiting a long time for these things, or maybe it's a cost factor of the EUV, DSA, direct-write technologies, and everything. When are they going to show a difference? Or are we still going to also need multiple patterning along with those technologies?

Wong: We wouldn't need multiple patterning. It would just be EUV and DSA if we go down below 7 nm.

Liebmann: I wouldn't be shocked if we introduced EUV in double patterning right out of the gate. By the time we have everything debugged in EUV—and we've invested so much money that it really doesn't make sense to go to a higher numerical aperture, to throw out everything we have and build a whole new tool. I think it's quite possible, not desirable by any means but quite possible, that we would have to introduce EUV with a double-patterning, litho-etch-litho-etch kind of approach.

Pan: A lot of people are still doubtful about whether EUV will make it into prime time. Of course, there has been a lot of EUV investment from ASML, Intel, TSMC, and Samsung: billions of dollars. Still, the biggest problem for the EUV is the light source. It

is still an order of magnitude away from the light intensity needed for volume production. And there are ongoing discussions of when it really reaches prime time, maybe at 7 nm. Then, it becomes subwavelength lithography again, and we do need to use a high numerical aperture and figure out the OPC-like stuff for EUV.

So then, we may still have to use double patterning with EUV. For one generation, maybe 7 nm, we may not need it, but if we want to go a little further, like 5 nm, we will need double patterning again.

Liebmann: All the challenges with EUV aside, just from a fundamental resolution standpoint, I was perhaps naively thinking that, once we introduce EUV, all of our resolution problems are solved.

But this might not be the case. The tip-to-tip and tip-to-side spacing we're achieving at 10 nm, because of techniques like triple patterning, don't look good for scaling to 7 nm with EUV. That's simply because the dimensions on the EUV mask would be getting so small that there's nothing to measure or inspect, so we immediately have a problem: a lot of our 2-D configurations don't scale, even if we have the most optimistic assumptions of bringing EUV online. This is something that caught me off guard recently, looking at some of the resolution predictions of EUV.

Kawa: It is my understanding, from what I've seen on EUV with the current numerical apertures still around 0.35, that optical proximity correction (OPC) is needed, right out of the gate, as Lars said. Again, the first time I encountered EUV, I thought—given the short wavelength of 13 nm—we're done. But it's not, so its overall resolution without enhancement is pretty low for supposedly promising wavelength.

Wong: That's also the mask defect problem for EUV.

Kawa: Yes. Now we can start enumerating the energy, the throughput, and all these things. So EUV will have a role in complementary patterning, but probably not be as much of a workhorse as we thought it would be as an alternative to 193i lithography.

Liebmann: I think there's been tremendous progress, in academia and in the EDA industry, in terms of triple-patterning decomposition. We, of course, all understand that NP-complete problems can't be solved, and there's been good progress in the past two years or so, really, coming up with decomposition solutions. So as a customer of all this, I think what we're really missing in triple patterning to make this useful is really a means of identifying bad layouts—layouts that cannot be decomposed—in a way that a designer can do something with this information.

In double patterning, we have this concept of identifying odd cycles that can be as little as three shapes that come together but we only have two colors, so we have to fix this. With triple patterning, it's immediately a much larger number of shapes that interact to cause a conflict. Showing this to designers in a way that they can understand it and make intelligent choices to fix the layout—that may be the next big breakthrough we need in order to make triple patterning really practical.

Wong: There are actually similar theorems on characterizing three-colorability. Two-colorability is simple: it's just based on odd/even cycles. For three-colorability, you only have necessary, but not sufficient, conditions, so we have all kinds of theorems. But, how well they would actually translate into practice remains to be seen. So, even though there is a wealth of theorems, they may not be as useful as I thought. I agree with Lars that there is much work to be done.

Joyner: You'd like to see some kind of feedback to the designer saying, "These are the kinds of things that are causing problems."

Liebmann: Right. A lot of the academic work has focused on taking big blocks of layout and very efficiently decomposing them, which is a very important piece of work. Then, there are additional constraints on density balancing between the different colors and all of that. But what we really need is a means of implementing a hierarchical design flow. We need to be able to check standard cells in a way that we know they're decomposed. It can be either that we decompose them, that we have a colored flow, or a colorless flow where we don't bother keeping the colors but we present the designers with conflicts so that they can fix them, so by the time the library is checked in, it's color clean.

Then, of course, we need placement methodologies that ensure that during placement we don't mess things up, so when the router comes in and drops more metal shapes into that space, it's all clean. In one perspective, it's a much simpler problem, because we're dealing with small units of

design at any given moment. On the other hand, it's a more complicated design because we have to present the information in a way that somebody who doesn't want to study graph theory can understand what to do with this layout to quickly get to a point where it passes design rule checking (DRC).

Joyner: We've been dealing with the question of "What are the CAD challenges with triple patterning?" We've mentioned several of those already, including feedback to the designers, and placement. What are some other challenges that vendors see coming?

Kawa: First of all, runtime. But the other thing for a standard cell library—when we have all those tight rules for end of line, it gives us very dense cells, but it also puts restrictions on the availability of pins for routing. That's a very messy problem, really.

Pan: I agree about the runtime. Essentially, given an arbitrary layout, we want to quickly tell whether it's decomposable or not. There are other complications, however, whether you allow stitching or not, and so on. Those things will make the problem even more complicated, which is why it's important to have hierarchy and also maybe a bottom-up approach. For example, the standard cells can be precategorized and have different decomposable versions.

Meanwhile, we need a unified standard cell and placement co-design methodology. By using that, hopefully we can obtain compliance through correct-by-construction instead of as an afterthought. Our ICCAD'13 paper (which just won the Best Paper Award on Monday: "Methodology for standard cell compliance and detailed placement for triple patterning lithography") deals with this problem. Routing is another very complicated problem, especially when we deal with pin access. Ultimately, the multiple-patterning-aware physical design has to consider standard cell together with both placement and routing.

Liebmann: I would break this challenge down into two event horizons. From our EDA partners, I would like to see good conflict reporting, as with the three-color equivalent of odd cycles. There's been some progress made there. From academia, where there's sort of a longer event horizon, I think color-aware placement on two axes would be really nice. There's been some work done on keeping the power rails the same color and just worrying about the vertical boundary. Well, we have shapes crossing that power rail that need to be three-color mapped. So having a placer that can solve a color-aware placement problem with three colors in two axes would be really nice to have. I think that goes back to academia; I don't think the EDA industry is quite ready to tackle that one yet.

Wong: I think one of the problems to be addressed is one you mentioned earlier, about "hotspot" detection: figuring out where a layout goes wrong. Recall that we had this approach of characterizing all possible solutions by using a graph where a path corresponds to a coloring solution. If there is no path, that means there is a problem in making it possible to have connectivity. That capability will give designers guidance in how to fix the layout, so I see some promise there. While I have not worked out the details, I think it's possible to provide something like that.

Kawa: Also, another EDA challenge, other than runtime, is color balancing. That's another challenge in itself.

Liebmann: One of the questions we've been discussing is, "Is triple patterning working? Or, how mature is it at this point?" I think on the process side of things, the concept certainly has been demonstrated. But this question of stitching versus color balancing is one where I would expect us on the manufacturing side to reverse our position a few more times. At this point, we're saying that we'd rather not introduce new stitches to get better color balancing. We'll be able to deal with some offset in the relative color distribution. I could see us running into issues with that and then giving feedback to the EDA industry such as, "You need to put more emphasis on color balancing. We'll take a few extra stitches." And we might find out the stitches cause defects. So, we have to engage early so that we can churn this thing a few times.

Kawa: I'm smiling because when I talk to my place-and-route colleagues about the status of things, in terms of their interaction with our partners in the industry, things seem to be changing on a weekly basis.

Liebmann: That's one risk of engaging early. We all understand we have to engage early because these challenges take a long time to solve. But then you have to be prepared for both parties to change their mind a few times before we arrive at the final solution.

Pan: From an academic perspective, whether it's stitch or density, the layout decomposition algorithm must be adaptive. There is a certain kind of weight that can be adjusted, depending on the manufacturing process. Different foundries, whether it's IBM, Samsung, TSMC, or GlobalFoundries, do have their own "secret sauces" and thus different manufacturing processes.

But we can have a framework in which we can adjust weights depending on how well they control different process variations—for example, whether you prefer a bit more stitching to have less penalty in the density or *vice versa*. I think those are the frameworks that academics can provide. As we go to even smaller technology nodes, we will have more and more challenges. For the example of 7 nm, then the conflict across the power rails is going to be really messy.

Wong: I don't think it's a difficult problem that, if you're given a fixed layout, you want to have a solution as balanced as possible. On the other hand, even that may not be very balanced. So then, the question is, during placement and routing and then considering other things such as density, how do they interact? That is the more complicated problem. If the layout is static, there are good strategies available to us where the optimal solution may not be balanced, so then the layout has to be modified. That is the problem: how do you do it?

I see another challenge potentially with triple patterning because of the mask alignment issues. With triple patterning there are even more variations because now we have three masks, and that would impact timing analysis. Suddenly the spacing changes the coupling capacitance and that would affect delay, and so since you have more masks, that would result in more alignment issues.

Liebmann: I was surprised there were no papers at this conference on that topic. I think we as an industry did a good job dealing with extraction and timing optimization for double patterning. But we put in some cheats, some simplifications—basically, we know that our nearest neighbor is always the opposite color from the attacked line. At the distance where it could be the same color, the capacitive coupling is so small that we can ignore it.

But with triple patterning, we have the additional challenge that the neighbor to the right and the neighbor to the left can be the same color or they can be different colors. So they can both attack us in the same direction or be sort of synchronized to each other. That could have a profound impact on the need to do fully, explicitly colored layout, because it matters for timing. This whole discussion that we're having in double patterning on colorless design, colored design—some foundries like to hide all the coloring from their customers with a colorless design. But if it matters for extraction, then we have to color it one way, freeze the colors, and then preserve at least the relative color dependency throughout the flow.

Wong: We would like to solve all these problems, but we lack funding.

Pan: One of the ideas we presented in ASPDAC 2010 describes this kind of overlay compensation. We try to color nets such that the timing variation due to overlay is automatically cancelled out. The idea works like this: In double patterning, when the masks shift, in terms of timing-critical paths sometimes the coupling capacitance is more, sometimes it's less. If we carefully color the masks, we could make the critical-path timing variations cancelled out even with unpredictable mask overlay error. But with triple patterning, the complexity is much higher, as Lars mentioned. So we need to develop new techniques for timing-critical nets where we can take advantage of that kind of compensation effect. As far as I know, there has been very little research on this for triple patterning.

Joyner: This roundtable discussion on triple patterning seems to be an area where there's a real partnership between universities and industry, in terms of moving forward. Would you agree?

Kawa: Absolutely. There is no alternative.

Liebmann: We, from industry, have been doing a much better job engaging our EDA partners earlier, which is significant. The EDA partners have been doing a better job engaging with us early, which is also significant because they are not waiting for the purchase orders to come in to solve these problems. But I think we lack the foresight to engage academia effectively in solving problems that are two or three technology nodes out. The papers at this conference are things that we're concerned about now. So to take it out of academia into the EDA industry, to get a solution onto the table, I think we've almost missed that window of opportunity. We should be talking about things like DSA, or resolution enhancement techniques on EUV, or something similar. But it's getting difficult to

predict what the big challenges will be more than two generations out.

Kawa: Why do you think it's that way? Is it because the targets keep changing? What do you think is going to be a viable technology to emerge within the timeframe of two or three years? It's apt to be an infeasible solution. I'm not disputing your premise; it's very valid. But what's causing it and what's the remedy? Part of my worry is how many technologies we assumed should be the trend of the future in a few years, yet nothing happened. By the same token, DSA—the first talks and papers I started seeing about DSA were more than ten years ago. I said, "It's fascinating, it looks very promising, but when is it going to happen?" And now it's getting closer. So by the same token, how do we—I don't want to use the word "predict"—but how do we minimize the risk of the direction in which we point academia through grants and say, "I want you to focus on this area"?

Wong: With academia, first of all, there are two purposes: doing research and training students for the workforce. We need to start early in developing technology, because by the time the technology becomes viable, it may be too late to involve academia. And if you keep students interested in a problem, they will stay in this area. Otherwise, they might go to work for Google and Facebook. So give them interesting problems, and after graduation they might work in industry, although the kind of problem they work on then may be different. At the same time, one of these technology paths may pan out, and we don't have to play catch-up games within EDA.

Pan: It's very important to work with industry and to know what key problems people are seeking solutions for. For lithography, it's a very fast-changing area. We could be working on something that's a niche type of problem or too forward-looking, and it may not be used. But that's OK and it's the nature of research.

On the other hand, there are many fundamental problems in EDA for which academia can still offer a different kind of approach. For example, for placement, there have been tools from vendors for many years. But it's an NP-hard problem, and there are new academic approaches that can give new thought-provoking results. It's good to have both, to look ahead and to have the elegant approach. I think that would be the best scenario.

Liebmann: The industry has just been very bad at predicting the future more than maybe one node out. We have formal surveys that can confirm we've done a lousy job predicting the future. Part of that is just because the levels of pain we're willing to tolerate just keep increasing. The idea of doing triple patterning would've been completely shot down just five years ago, and now we think, "Yes, this seems pretty reasonable."

Joyner: Placement is still a challenge, although it's been pronounced as a solved problem many times. But, you know, we never get there. I think the best quote about prediction, as Lars said, is attributed to Niels Bohr, "Prediction is very hard, especially about the future." So with that, I'd like to thank our panelists very much. ■

About the participants

William Joyner, our moderator, is a Senior Director of Computer-Aided Design and Test at Semiconductor Research Corporation (SRC).

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