Guest Editors' Introduction: Special Issue on Machine Learning for CAD/EDA

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Moore's Law is still alive and well, as far as increasing the complexity of integrated circuits (ICs) is concerned. Logic ICs with about 20 billion transistors or even more are being manufactured today. Their design is a daunting task. While complexity keeps increasing relentlessly, novel technical challenges (e.g., mask patterning challenges and increasing manufacturing variations) appear as we are moving ever closer to the limits of technology scaling.

Machine learning (ML), including artificial intelligence (AI) techniques, is increasingly being researched as a potential solution to the "design crisis" resulting from these forces. It is being applied for IC design throughout the entire design flow, from hardware–software codesign and system-level optimization all the way down to layout optimization and mask preparation.

In conjunction with DATE 2019, a very successful workshop on the topic of "Machine Learning for CAD" was held. The audience felt that this topic was important and novel enough to warrant a dedicated workshop. Thus, "MLCAD—ACM/IEEE Workshop on Machine Learning for CAD" was born. Its inaugural edition was held already in September 2019 near Banff, AB, Canada. It attracted about 30 high-quality presentations and some 60 participants. For 2020, the second edition of the workshop was planned to be held in Iceland in September. Alas, the pandemic turned out to be more long-lived than initially hoped, so eventually, the workshop was held virtually in November 2020. After another virtual edition in 2021, MLCAD returned to physical presence in September 2022 in Snowbird, UT, USA. Interest in the MLCAD workshop is strong. It attracts a dedicated community of researchers and practitioners working on applying ML/AI to the task of design automation of electronic circuits and systems.

Many of the papers in this special issue are based on presentations held at the second MLCAD workshop, but the contents extend beyond the workshop. Just like the workshop itself, the papers in this special issue address the entire design flow and bring together academic researchers with experienced industry experts from leading companies.

This special issue starts with a keynote paper by Andrew Kahng of University of California at San Diego (UCSD), based on his opening keynote of MLCAD 2020 [A1]. The article explores the relation of learning, optimization, and scaling in the context of ML for CAD. It sketches out a vision for the development of ML for CAD: from today's MLCAD to

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tomorrow's ML-based design automation (MLDA). Just as Andrew's keynote attracted a lot of discussions at the workshop, so will this article influence future research on ML for CAD/EDA.

Before the contributed articles, the special issue also includes a survey paper on ML methodologies for IC design in advanced nodes, mostly by guest editors [A2]. The survey is structured along a taxonomy of ML methodologies. Thus, the reader will learn about state-of-the-art research on EDA for different stages of the design flow using shallow models, convolutional neural networks, graph neural networks, generative models, and finally reinforcement learning, closing with an overview of open challenges and promising directions.

The following contributed articles are arranged along the design flow, from codesign of hardware and software down to design rule checks for manufacturing.

In [A3], Styliani Tompazi and his coauthors (School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, Belfast, U.K.) consider the microarchitecture-aware modeling of timing errors and the estimation of the vulnerability of software programs to such errors. They propose a significance-aware code vulnerability factor (SCVF). This metric quantifies the susceptibility of applications to such timing errors, utilizing an ML-based error prediction model. The proposed workload- and the history-aware error prediction model are based on supervised ML methods.

For [A4], industry authors from Infineon Technologies join forces with researchers from Johannes Kepler University Linz and the Technical University of Munich to demonstrate how the design cost of systems consisting of hardware and software can be improved using ML techniques within an industrial design framework utilizing model-based design. Using hardware–software interfaces as an example, the proposed approach generates optimized solutions using deep reinforcement learning (DRL), based on preferences specified by a designer.

Cheng Zhuo and his coauthors from the College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China, address dynamic voltage and frequency scaling (DVFS) in their article [A5]. DVFS is an essential approach that is widely used to optimize the performance and energy tradeoff. In their paper, the authors employ learning models to predict the workload and then estimate the corresponding power and thermal dissipation. The proposed framework utilizes a DRL-based controller.

In [A6], Peng Cao and his coauthors (National ASIC System Engineering Center, Southeast University, Nanjing, China) discuss how wide-voltage designs can be improved using ML. In wide-voltage designs, timing needs to be verified at a very large number of corners. The article presents a learning-based approach to predict path timing for multiple unknown corners at low voltage. The approach uses long short-term memory (LSTM) to exploit circuit topology correlation with timing and a multigate mixture-of-experts (MMoE) network to capture correlation among all analysis corners.

Haoxing Ren and his coauthors from NVIDIA argue convincingly for the coexistence and actual integration of ML approaches and classical algorithmic approaches in [A7]. Using the standard cell routing problem as a showcase, they demonstrate that the integration of ML techniques with well-established algorithmic approaches can overcome challenges faced by current applications of ML to EDA problems.

Finally, Luis Francisco et al. (Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA) bring together ML and design rule checking (DRC) in [A8]. They apply deep transfer learning to the DRC task. A parameterized synthetic dataset generator is used to train the model, which can identify DRC violations with a detection rate of up to 100%, depending on how complex the rule is. The proposed checker is 7.5x faster than conventional checkers.

Acknowledgments

We would like to acknowledge all the authors for their contributions. Without their technical and scientific expertise and their dedicated effort, this special issue would obviously not exist. A significant number of anonymous expert reviewers ensured in multiple rounds of reviews that only the most suitable manuscripts found their way into this special issue and helped to improve those successful manuscripts with their expertise and insights.

A special thanks is due to the former Editor-in-Chief Jörg Henkel (KIT), who encouraged us to propose this special issue and guided us through the steps of implementing this special issue. Together with Marilyn Wolf, Jörg is also the

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initiator of the MLCAD workshop. Without these two pioneers, neither this special issue nor the workshop would exist at all.

We would also like to especially thank Sara Dailey for her continuous support and her patience with the guest editors who often needed special encouragement to focus on putting together this special issue among numerous other responsibilities. Without her constant guidance, this special issue would not have seen the light of day.

Finally, we hope that readers will enjoy the contributions in this special issue and that the insights offered by them will inspire further novel research on ML for CAD/EDA, which will then be presented at another instance of MLCAD, or some other conference or journal.

Enjoy! ■

Appendix: Related Articles

[A1] A. B. Kahng, "Machine learning for CAD/EDA: The road ahead," *IEEE Des. Test*, vol. 40, no. 1, pp. 8–16, Jan. 2023.

[A2] T. Chen, G. L. Zhang, B. Yu, B. Li, and U. Schlichtmann, "Machine learning in advanced IC design: A methodological survey," *IEEE Des. Test*, vol. 40, no. 1, pp. 17–33, Jan. 2023.

[A3] S. Tompazi et al., "Estimating code vulnerability to timing errors via microarchitecture-aware machine learning," *IEEE Des. Test*, vol. 40, no. 1, pp. 34–42, Jan. 2023.

[A4] L. Servadei et al., "Deep reinforcement learning for optimization at early design stages," *IEEE Des. Test*, vol. 40, no. 1, pp. 43–51, Jan. 2023.

[A5] C. Zhuo et al., "A DVFS design and simulation framework using machine learning models," *IEEE Des. Test*, vol. 40, no. 1, pp. 52–61, Jan. 2023.

[A6] P. Cao et al., "Topology-aided multicorner timing predictor for wide voltage design," *IEEE Des. Test*, vol. 40, no. 1, pp. 62–69, Jan. 2023.

[A7] H. Ren et al., "Machine learning and algorithms: Let us team up for EDA," *IEEE Des. Test*, vol. 40, no. 1, pp. 70–76, Jan. 2023.

[A8] L. Francisco, W. R. Davis, and P. Franzon, "A deep transfer learning design rule checker with synthetic training," *IEEE Des. Test*, vol. 40, no. 1, pp. 77–84, Jan. 2023.

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