Experimental Validation of Dual H-Bridge Current Flow Controllers for Meshed HVdc Grids

Senthooran Balasubramaniam, *Student Member, IEEE*, Carlos E. Ugalde-Loo, *Member, IEEE*, Jun Liang, *Senior Member, IEEE*, Tibin Joseph, *Member, IEEE*, Rose King, *Member, IEEE*, and Andrzej Adamczyk

***Abstract*—The current-carrying capability of dc lines is limited by their thermal and electric stress limits. Thus, the line current must be maintained within the permissible operational region to protect the lines from damage. In a dense dc grid, control over each line current cannot be achieved without including additional control devices. In this paper, a dual H-bridge current flow controller (2B-CFC) is used to manage the dc grid line power flow by providing dc voltage compensation in series with dc lines. A centralized hierarchical control system is proposed to coordinate the operation between multiple CFCs. A novel voltage-sharing control scheme is demonstrated. It is shown that such a scheme reduces the workload on a single CFC by sharing the required control voltage between multiple CFCs, and, in addition, can be used to avoid control conflicts among active CFCs during communication failure. An experimental platform consisting of a three-terminal dc grid and small-scale 2B-CFC prototypes has been developed to validate the concepts. For completeness, the CFC performance has been analyzed for overload conditions and when no communication exists. Small-scale dc circuit breakers have been developed to study the CFC performance under a pole-to-pole fault.**

***Index Terms*—Current flow controller, dc line, dc circuit breaker, H-bridge, multi-terminal HVdc grids, voltage source converter.**

I. Introduction

THE breakthrough in the development of solid-state semiconductor valves in the 1970s has led to the installation of hundreds of point-to-point HVdc links around the globe. HVdc links are suitable for bulk power transmission over long distances due to their lower losses and cost compared to ac links [1]. Particularly, voltage source converter (VSC) based HVdc links have been increasingly adopted due to their decoupled power flow control, black-start capability, control flexibility and reduced footprint [2], [3]. It is desirable to connect additional VSC terminals to existing point-to-point links in a multi-terminal HVdc (MTdc) configuration to maximize power transfer and to achieve an effective power flow management and operational reliability. It is expected that MTdc grids will facilitate a cross-border energy exchange between different countries and will enable reliable power transfer from offshore wind farms [4].

In HVdc systems, dc power can be transmitted via overhead lines (OHLs) or cables. Although cables are inherently suitable for underground or sub-sea transmission and pose a reduced visual and environmental impact compared to OHLs, OHLs are attractive owing to their high voltage and high power handling capabilities and lower cost [5], [6]. However, both dc cables and OHLs have intrinsic operational limits over the amount of power that can be transferred. These limits are determined by thermal and electric stress characteristics [7], [8].

In a very dense MTdc grid, power flow cannot be regulated independently as it is passively determined by the resistance between dc nodes. Since the line current distribution is uncontrolled, some lines may carry excess current while the remaining ones may be under-utilized. System operation beyond thermal and stress limits could damage OHLs and cables and lead to cascaded failure. In a system with high power demand, such a transmission interruption could be very costly. This problem may be relieved through the installation of auxiliary lines, but at the expense of high capital and environmental costs. Moreover, an effective line current control can only be achieved with the inclusion of additional control structures to the system.

Power flow controllers (PFCs) are power electronics based devices capable of providing dc line current control in MTdc grids [9]. Although one way to control dc line current is through the inclusion of a controlled series variable resistor [9], this approach offers a limited controllability and causes high power losses. In recent years, several voltage source-based PFCs have been proposed to eliminate the shortcomings of a resistive-based solution. These devices require an ac connection which can be established through a step-down transformer [10], [11]. Since these PFCs are electrically coupled to the dc side, the voltage difference between the transformer windings and the ground is equal to the rated dc voltage. Therefore, additional insulation is essential to decrease the capacitance between the windings and ground, but this may in turn increase the transformer size and winding resistance. In addition, voltage source-based PFCs generate significant current harmonics in the valve winding, leading to further power losses. To eliminate these issues, the device has to be powered inside the dc grid [12]–[15]. An inter dc grid powered PFC is referred to as a current flow controller (CFC) [12].

Manuscript received February 2, 2017; revised June 15, 2017; accepted August 26, 2017. Date of publication September 18, 2017; date of current version January 22, 2018. Paper no. TPWRD-00162-2017. *(Corresponding author: Carlos E. Ugalde Loo.)*

S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang, and T. Joseph are with Cardiff University, Wales CF24 3AA, U.K. (e-mail: BalasubramaniamS@cardiff.ac.uk; Ugalde-LooC@cardiff.ac.uk; LiangJ1@cardiff.ac.uk; JosephT@cardiff.ac.uk).

R. King and A. Adamczyk are with GE's Grid Solutions Business, Stafford ST17 4LX, U.K. (e-mail: Rosemary.King@ge.com; Andrzej.Adamczyk@ge.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPWRD.2017.2752301

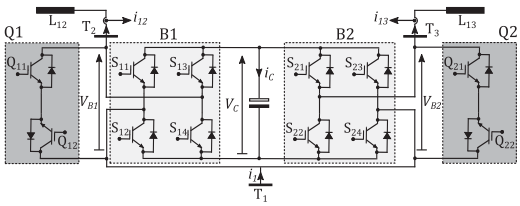

Fig. 1. Topology of a 2B-CFC.

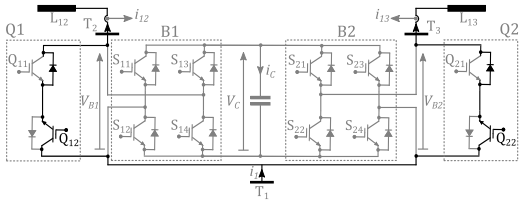

Fig. 2. Operation under the ZC mode.

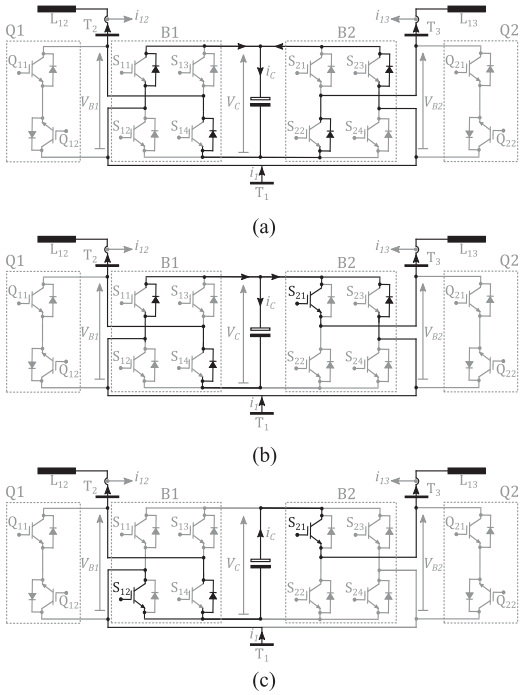

Fig. 3. Operational stages of a 2B-CFC under the CC mode: (a) Charge mode 1; (b) charge mode 2; (c) discharge mode.

In [12], the concept of a dual H-bridge CFC (2B-CFC) was presented, with its operation and control being further examined in [16]–[19]. An average model and a small signal stability based model of a 2B-CFC have been presented in [18] and [20], respectively. Although a 2B-CFC has been experimentally tested in [17], a constant dc voltage source and active loads were used to represent the converters. Therefore, the interaction between the CFC and VSCs was not experimentally verified. To bridge this gap, the operation and control of a 2B-CFC is experimentally validated in this paper using a three-terminal meshed MTdc test-rig. The CFC operation is analyzed using monopole and bipole configurations. A novel centralized hierarchical control scheme is introduced to coordinate the operation between multiple 2B-CFCs. To the knowledge of the authors, the interaction between multiple CFCs has only been discussed in [21]. Moreover, a new control strategy is proposed to increase the grid control flexibility during CFC overloading and absence of communications, with the CFC performance being assessed under such conditions. Although the fault performance of a 2B-CFC has been previously studied in [19] through software simulations, such an initial approach has been extended in this paper to experimental studies. Small-scale solid-state dc circuit breakers (DCCBs) have been implemented to assess the device performance under pole-to-pole dc faults, with the interaction between the DCCB and the 2B-CFC during fault conditions being analyzed.

II. Dual H-Bridge CFC

A 2B-CFC consists of two electrically coupled H-bridges connected in series with dc lines (see Fig. 1, where H-bridges B_1 and B_2 are connected with lines L_{12} and L_{13}, respectively). Switches Q_1 and Q_2 are formed by two anti-series connected IGBTs and are placed in parallel with B_1 and B_2, respectively, to avoid interruptions in the grid current flow and thus ensure the safety of the dc grid upon CFC internal failure. In this configuration, the power taken from L_{12} is equal to the power added to L_{13}, or vice versa.

In the following subsection, the device operation is explained assuming that current flows from terminal T_1 to terminals T_2 and T_3 unless mentioned otherwise.

A. Operation

The 2B-CFC has the operation modes described below.

1) Zero Compensation (ZC) Mode: In this mode of operation, the required line current reduction or increment is zero and thus the series dc voltage compensation is zero. Therefore, B_1 and B_2 must be bypassed. Although this could be achieved by turning on switches S_{12} and S_{14} of B_1, and S_{22} and S_{24} of B_2, the ZC mode is implemented instead by turning switches Q_1 and Q_2 on (as shown in Fig. 2). The reader is referred to Section V-D for further insight on this.

2) Current Control (CC) Mode: A required line current reduction or increment is achieved in this mode by providing a negative or positive dc voltage compensation in series to the controlled dc line. The magnitude of the inserted dc voltage is regulated by switching the H-bridge voltage. The active switch on each H-bridge is determined by the control objective and line current directions. If current flows from terminal T_1 to T_2 and from T_1 to T_3, switches S_{12} and S_{21} of B_1 and B_2 are modulated to reduce the current on line L_{12}, while all other switches (S_{11}, S_{13}, S_{14}, S_{22}, S_{23} and S_{24}) are maintained off. However, when the current flow is reversed (i.e., from T_2 and T_3 to T_1), S_{11} of B_1 and S_{22} of B_2 must be modulated instead to reduce the current in L_{12} while the remaining switches (S_{12}, S_{13}, S_{14}, S_{21}, S_{23} and S_{24}) are kept off. For additional insight on the four quadrant switching selection of a 2B-CFC, the reader is referred to [19].

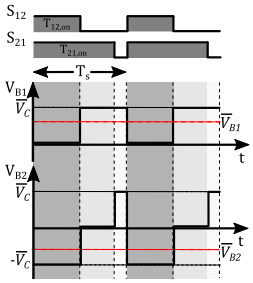

Fig. 4. Switching waveforms for the CC mode.

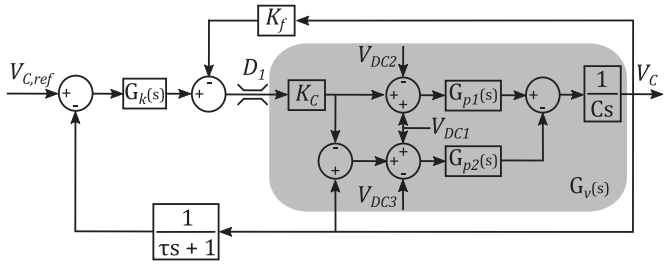

Fig. 5. Capacitor voltage controller.

Fig. 3 shows the operational stages of the CFC during the CC mode when current flows from terminal T_1 to terminals T_2 and T_3. The switching states of the controlled switches and the corresponding changes on the bridge voltages V_{B1} and V_{B2} are shown in Fig. 4. When switches S_{12} and S_{21} are off (Fig. 3(a)), the line currents flow through the naturally commutated diodes and charge the capacitor rapidly. The voltages across terminals T_1 and T_2, and T_1 and T_3, are equal to the inserted dc voltages V_{B1} and V_{B2}, respectively. These are given as:

$$V_{B1,a} = \overline{V}_{\rm C}, \quad V_{B2,a} = \overline{V}_{\rm C}, \tag{1}$$

where $\overline{V}_{\rm C}$ is the average value of capacitor voltage $V_{\rm C}$. This operation results in a decrease in currents i_{12} and i_{13}.

When S_{21} is on and S_{12} is off, bridge B_2 is bypassed and B_1 charges the dc capacitor (see Fig. 3(b)). In this case,

$$V_{B1,b} = \overline{V}_{\rm C}, \quad V_{B2,b} = 0. \tag{2}$$

As a result of such a positive voltage injection in series with line L_{12}, current i_{12} decreases while i_{13} increases to maintain the power balance.

Conversely, a negative voltage must be inserted in series with L_{13} to increase line current i_{13}. This can be achieved by switching on both S_{12} and S_{21} (see Fig. 3(c)). During this period, the capacitor is discharged into L_{13} and

$$V_{B1,c} = 0, \quad V_{B2,c} = -\overline{V}_{\rm C}. \tag{3}$$

As shown in Fig. 4, continuous switching of S_{12} and S_{21} generates a pulsed positive voltage (V_{B1}) across the CFC terminals T_1 and T_2 and a pulsed negative dc voltage (V_{B2}) across T_1 and T_3. This increases i_{13} and also decreases i_{12}.

The average bridge voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ can be derived from (1)–(3) as follows:

$$\begin{aligned}\overline{V}_{B1} &= \frac{V_{B1,a}\cdot T_{\rm off,21} + V_{B1,b}\cdot (T_{\rm on,21} - T_{\rm on,12})}{T_{\rm s}} \\ &= \frac{\overline{V}_{\rm C}\cdot T_{\rm off,21} + \overline{V}_{\rm C}\cdot (T_{\rm on,21} - T_{\rm on,12})}{T_{\rm s}} \\ &= \overline{V}_{\rm C}(1 - D_1)\end{aligned} \tag{4}$$

$$\begin{aligned}\overline{V}_{B2} &= \frac{V_{B2,a}\cdot T_{\rm off,21} + V_{B2,c}\cdot T_{\rm on,12}}{T_{\rm s}} \\ &= \frac{\overline{V}_{\rm C}\cdot T_{\rm off,21} - \overline{V}_{\rm C}\cdot T_{\rm on,12}}{T_{\rm s}} \\ &= \overline{V}_{\rm C}(1 - D_1 - D_2)\end{aligned} \tag{5}$$

where D_1 is the duty cycle of switch S_{12}, D_2 the duty cycle of S_{21}, T_s the switching period, $T_{{\rm on},ab}$ the turn-on time of switch S_{ab}, $T_{{\rm off},ab}$ the turn-off time of S_{ab}, $D_1 = \frac{T_{\rm on,12}}{T_{\rm s}}$ and $D_2 = \frac{T_{\rm on,21}}{T_{\rm s}}$. The relationship between $\overline{V}_{B1}$ and $\overline{V}_{B2}$ with line currents i_{12} and i_{13} can be represented by:

$$\begin{aligned}P_{B1} &= P_{B2}, \\ \overline{V}_{B1}\cdot i_{12} &= \overline{V}_{B2}\cdot i_{13}\end{aligned} \tag{6}$$

where P_{B1} and P_{B2} are the powers of H-bridges B_1 and B_2, respectively.

3) Voltage Control (VC) Mode: Operation under a VC mode is achieved by disabling the line current control loop. This way, the capacitor voltage is regulated regardless of the line current value. To achieve this, the duty cycle of one switch must be set to 1 while the other switch adjusts its duty cycle so that the voltage is maintained constant. For instance, when current flows from terminal T_1 to terminals T_2 and T_3, the duty cycle of switch S_{21} must be set to 1 while switch S_{12} adjusts its duty cycle. Since S_{21} is on, the CFC takes only two switching states (see Fig. 3(b) and (c)). The VC mode usually takes place under the voltage sharing method presented in Section III. For further information on the detailed operation and control of a 2B-CFC under a VC mode, the reader is referred to [19], where a single modulation strategy is employed to achieve current control by varying the voltage across the capacitor.

B. Controller Design

A master-slave (or dual modulation) scheme [19] has been adopted to control a 2B-CFC connected with L_{12} and L_{13} (see Fig. 1). The capacitor voltage $\rm V_c$ and line current i_{13} are controlled independently by modulating switches S_{12} and S_{21}, respectively. The CFC capacitor voltage control loop is depicted in Fig. 5, where the grey rectangle encompasses the unregulated open loop dynamics. The dynamics of the dc lines are represented by transfer functions $G_{p1}(s)$ and $G_{p2}(s)$:

$$G_{p1}(s) = \frac{1}{L_{12}s + R_{12}}, \; G_{p2}(s) = \frac{1}{L_{13}s + R_{13}}. \tag{7}$$

TABLE I
SPECIFICATIONS AND PARAMETERS OF THE TEST-RIG

Devices	Specifications	Operating Rating
VSCs	Rated power	2 kW
	Rated ac voltage	140 V
	Rated dc voltage	250 V
	Topology	Two-level, Symmetrical monopole
AC inductors	L_{g1}, L_{g2}, L_{g3}	2.2 mH
DC lines	L_{12}	2.4 mH
	L_{13}	5.8 mH
	L_{23}	11.8 mH
	Equivalent R_{12}	0.26 Ω
	Equivalent R_{13}	0.78 Ω
	Equivalent R_{23}	0.98 Ω
DC capacitors	C_{g1}, C_{g2}, C_{g3}	1020 μF

TABLE II
SPECIFICATIONS AND PARAMETERS: 2B-CFCS

Devices	Specifications	Operating rating
CFC	Rated power	40 W
	Rated dc voltage	5 V
DC capacitor	C	4400 μF
Switching frequency	f_{sw}	2000 Hz

DC terminal voltages V_{DC1}, V_{DC2} and V_{DC3} are signals which affect the capacitor voltage dynamics in open loop. For control system design, these dc voltages are assumed as disturbances. By applying block diagram reduction techniques, the overall plant transfer function $G_v(s)$ relating the capacitor voltage V_C (output) to the duty cycle D_1 of switch S_{12} (input) is obtained:

$$G_v(s) = K_c \left(\frac{(L_{12}+L_{13})s + (R_{12}+R_{13})}{L_{12}s + R_{12}} \right) \cdot \cdot \left(\frac{1}{L_{13}Cs^2 + R_{13}Cs + 1} \right) \quad (8)$$

A controller $G_k(s)$ is proposed to ensure an adequate closed-loop performance:

$$G_k(s) = K \left(\frac{s+z_c}{s+p_c} \right) \left(\frac{s+z_p}{s} \right) \quad (9)$$

Controller $G_k(s)$ in (9) consists of a proportional-integral (PI) structure cascaded with a lead compensator, where z_p is the zero of the PI controller, z_c and p_c are the zero and pole of the lead compensator, and K is the overall controller gain. Such a control structure, if designed properly, is sufficient to provide high stability margins, eliminate the steady-state error and reject disturbances.

Let the parameters in $G_{p1}(s)$, $G_{p2}(s)$, and $G_v(s)$ be defined as in Tables I and II. Fig. 6 shows the open loop frequency response of $G_v(s)$. The bandwidth of the uncompensated system is 1000 rad/s and this value is kept when $G_k(s)$ is used. It can be also observed in Fig. 6 that the uncompensated system exhibits a poor phase margin ($\approx$4 deg). While the PI controller is used to achieve a zero steady-state error, the lead compensator significantly improves the phase margin to $\approx$68 deg to ensure

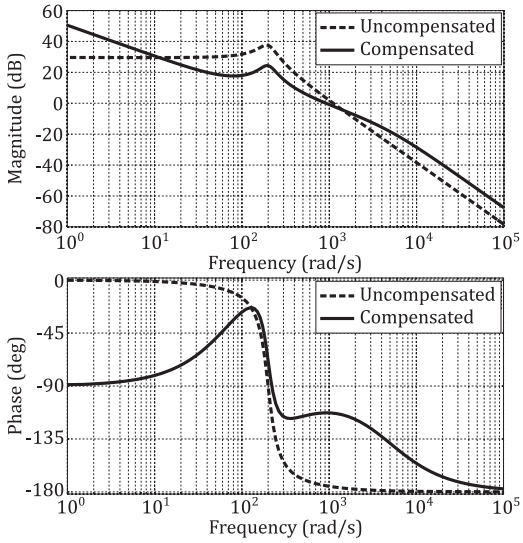

Fig. 6. System open loop frequency response (Bode plot): Uncompensated system $G_v(s)$ and compensated system $G_k(s)G_v(s)$.

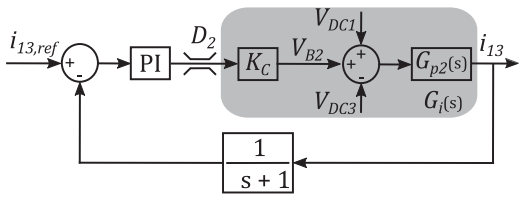

Fig. 7. Line current controller.

a good performance during transients and solid-state switching (or quadrant selection). Additionally, the CFC capacitor voltage loop considers a feedback loop with a proportional gain K_f to limit the initial overshoot in the capacitor voltage (see Fig. 5). Since the initial voltage across the capacitor is zero, the capacitor voltage controller would adjust the initial duty cycle of the controlled switch to zero. However, since line current flows through the capacitor, this is rapidly charged, which could lead to an overvoltage across its terminals. The feedback compensation provided by proportional gain K_f limits the initial overshoot by moving the duty cycle of the controlled switch towards unity.

Fig. 7 shows the line current control loop. Since plant $G_i(s)$ is a first order function, a PI controller is used. It should be highlighted that a first order filter with a cut-off frequency of 200 Hz has been employed with the voltage and current controllers to eliminate measurement noise. The control parameters can be found in the Appendix.

III. COORDINATED CONTROL OF MULTIPLE CFCS

In a complex dc grid, flexible current regulation cannot be achieved with a single CFC. This shortcoming can be relieved by installing CFCs at different locations. Under such a scenario, a centralized control scheme is essential to coordinate the operation among the devices. Fig. 8 illustrates the hierarchical control system when multiple CFCs are employed in a meshed-connected MTdc system. The control system consists of a

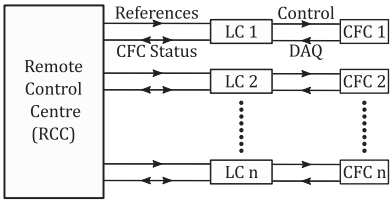

Fig. 8. CFC hierarchical control.

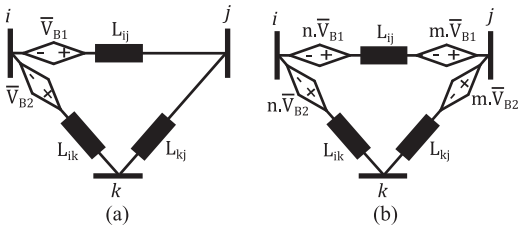

Fig. 9. Voltage sharing: (a) Single CFC; (b) multiple CFCs.

centralized remote control centre (RCC) along with multiple local controllers (LCs). Each CFC is assigned to an LC. The RCC monitors the grid power flow and calculates the required voltage and current reference values prior to scheduled power changes, energy trade or system maintenance (for instance, involving the disconnection of a dc cable). By employing a Broyden-based power flow algorithm [22], [23], the CFC with the minimum capacitor voltage will be assigned to control the line current since a small capacitor voltage implies lower power losses due to smaller ripple.

The LCs include the following control layers: system control, application control, CFC control and firing control. The system control layer establishes a secure bi-directional data transmission link with the RCC. In addition, it monitors the status of each control layer and sends this information back to the RCC. The application control layer accepts the voltage and current reference values set by the RCC and passes the reference values to the CFC control layer through a set of limiters. The CFC control layer is implemented as an array of PI controllers and control blocks. It provides the duty cycle to the firing control layer by processing the references and local measurements. The firing control layer generates the firing pulses to the individual semi-conductor valves.

A. Voltage Sharing - CFC Overloading

The operational range of a CFC can be maximized by increasing the capacitor voltage level. However, such an approach could in turn increase the device footprint and cost. This issue can be overcome by sharing the required dc voltage between multiple CFCs.

Fig. 9 shows an upgraded dc network with a single CFC and with two CFCs. If a single CFC is used (Fig. 9(a)), dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are required in series with lines L_{ij} and L_{ik} to achieve the desired current on line L_{ij}. Let $\overline{V}_{B1} > V_{C,\max}$, where $V_{C,\max}$ is the maximum voltage allowed across the CFC capacitor. For this scenario, the required line current reduction or increment cannot be achieved. However, when two CFCs are

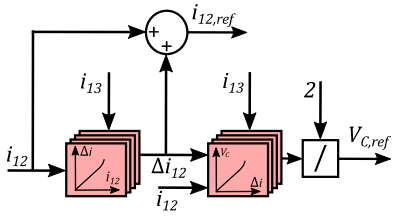

Fig. 10. Offline voltage and current reference calculation.

included into the dc network (Fig. 9(b)), the required capacitor voltage can be shared between the CFCs in an $n : m$ ratio. The relationships between the required series dc voltages and the capacitor voltage are given by:

$$n(\overline{V}_{B1} + \overline{V}_{B2}) \leq V_{C,\max},\ m(\overline{V}_{B1} + \overline{V}_{B2}) \leq V_{C,\max}, \quad (10)$$

where $n \leq 1$ and $m \leq 1$, with $n + m = 1$.

When more than one CFC is deployed in a common dc line, the control objectives must be established carefully to avoid potential conflicts. Only a single CFC in CC mode is permitted at any given load condition; however, operation of multiple CFCs in VC mode is allowed.

B. Voltage Sharing - Communication Failure

In HVdc systems, fibre optic and power line communication are widely employed for data acquisition and to dispatch control signals. As a result of technological advancements, these communication modalities have become faster and more reliable in recent years. However, a dc grid cannot just rely on wired-based communication links as they are vulnerable to natural disasters and human errors.

An MTdc grid should remain operational in case of any communication failure. Although the RCC sets the references for each CFC (and their status), the LCs should be designed to detect overloading conditions and to trigger the CFCs accordingly when communication is lost. In this case, local measurements should be employed. As highlighted previously, preassigned control objectives (i.e., modes of operation) must be established carefully among the active CFCs – with a single CFC acting in CC mode only. Current and voltage references are calculated offline using look-up tables, as shown in Fig. 10, where the dc line currents are used as inputs. For instance, if two CFCs are used, the CFC in a VC mode contributes half of the required capacitor voltage while the other half is approximately provided by the CFC in CC mode.

IV. MTdc Control and Configuration

The three-terminal meshed MTdc grid shown in Fig. 11 is used to validate the operation and control of 2B-CFCs. The VSC terminals have been arranged in a symmetrical monopole configuration and rated at $\pm$125 V and 2 kW. To establish a bipole operation, CFC modules A and B are installed in series with both the positive and negative poles of lines L_{12} and L_{13}. A master-slave control scheme for VSCs has been adopted to maintain the grid power balance [4]. It uses a classical *dq* ref-

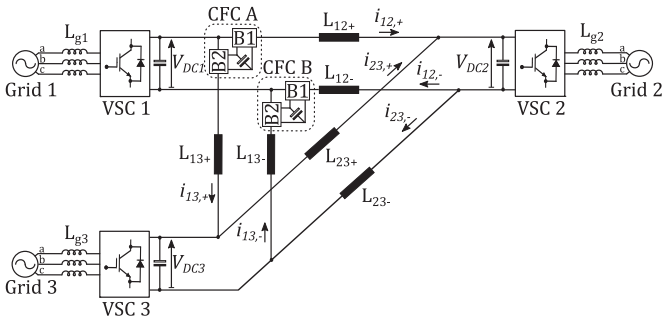

Fig. 11. Three-terminal MTdc grid with embedded CFCs.

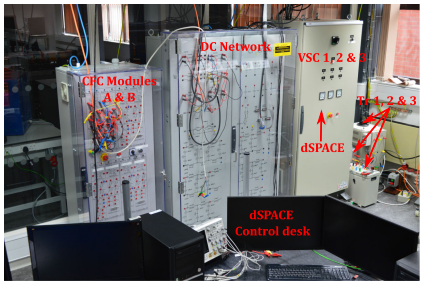

Fig. 12. Experimental setup.

erence frame scheme to regulate the dc voltage or active and reactive power.

Fig. 12 shows the experimental setup of the MTdc test-rig with embedded 2B-CFC prototypes. Each VSC is connected to an ac system through a phase reactor and a transformer. Autotransformers connected to the 415 V ac power supply represent the ac grids. A dSPACE DS1005 system is used to control the test-rig. Simulink-based real-time interface control blocks are used to implement the control scheme. Real-time operation is enabled through the ControlDesk 3.2 graphical user interface. For completeness, the specifications and parameters for the test-rig and the 2B-CFCs are provided in Tables I and II.

V. Simulation and Experimental Validation

The results reported in this section have been expressed in per unit considering the following power, voltage and current bases: 2 kW, 125 V, and 8 A. VSCs 1 and 3 are initially set to inject 0.8 and 0.2 p.u. into the MTdc grid, whereas VSC 2 has been designated as a slack busbar that maintains the grid power balance (i.e., maintains a constant dc voltage).

A. Transition to CC Mode During System Transients

A test to assess the performance of 2B-CFCs following ramp changes in power is carried out both through a simulation and with the experimental platform. To this end, the three-terminal dc grid equipped with CFCs has been modeled in Simulink/SimPowerSystems. The CFCs are placed at the positive and negative poles of lines L_{12} and L_{13}. CFC operation is coordinated using an RCC and each CFC is equipped with an LC. The RCC determines the state of each CFC by calculating the required CFC capacitor voltage to maintain the line current at a desired value.

In general, a CFC is used to maintain the line current of a given line at or below 1 p.u. However, it should be highlighted that in scaled systems such as in the experimental test-rig in Fig. 12, the forward voltage drop on the semiconductor switches affects the current flow between electrical nodes. During the capacitor charging mode of the CC mode, a maximum of two diodes, each with a forward voltage drop between 0.8–1 V, are inserted into the conduction path. The capacitor voltage required to achieve an optimum line current distribution may be very small and of a magnitude similar to the diode's forward voltage drop. Therefore, to build enough voltage across the capacitor and to demonstrate the CFC performance, a large current reduction must be achieved. In this case the current reference is set to 0.5 p.u., but this value may be just below 1 p.u. in a real system. It must be emphasized that the RCC could be used to determine the optimal CFC current references to achieve the best line current distribution in complex dc grids so that grid power losses are minimized [24].

The simulation (left) and experimental results (right) are shown in Figs. 13–15. Initially, both CFCs operate in a ZC mode, with switches Q_1 and Q_2 being turned on. At $t = 2$ s, the power reference of VSC 1 is ramped up from 0.8 to 1.4 p.u. (see Fig. 13(a)). As it can be observed in Fig. 13(b) and (c), line currents i_{12+} and i_{12-} surpass the maximum thermal current limit (of 1 p.u.). Following the overload detection, the LCs are activated to decrease the currents to 0.5 p.u. to achieve a better line current distribution. As a result, the terminal voltages of the converters have increased further to maintain the grid power balance (Fig. 13(d)). It can be observed both in simulation and experimental results that the terminal voltage of the master converter (V_{DC2}) deviates from its reference value to prevent the VSCs from entering into over-modulation.

It can be noticed that a small mismatch in the line current distribution occurs when comparing simulation and experimental results. This is due to forward voltage drops in diodes and converter power losses in the experimental platform. In the simulation, the voltage drops have been fixed to 0.8 V, with converter switching losses being neglected. Therefore, more power is injected into the dc grid in the simulation, which results in a different line current distribution compared to that in the experiment. Since the same current reference is employed for both cases, the required series dc voltage compensation is slightly higher in the simulation given that an additional current reduction is required.

Figs. 14 and 15 provide the voltage profiles of the CFCs. For the experiment, the capacitor voltages are maintained at 0.035 p.u., as shown by Figs. 14(a) and 15(a). Such voltage value is determined by the RCC. However, the required capacitor voltage is 0.004 p.u. higher for the simulation as a result of the grid's initial current distribution and voltage profile (the RCC uses instantaneous grid measurements to determine the capacitor voltage). During the CC mode, average dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are inserted in series with lines L_{12+} and L_{13+}, respectively. This is shown in Fig. 14(b). Since the line current flows in an opposite direction, the signs of the inserted dc voltages in series with L_{12-} and L_{13-} (see Fig. 15(b)) are opposite with respect to those shown in Fig. 14(b). In the ZC mode, fixed

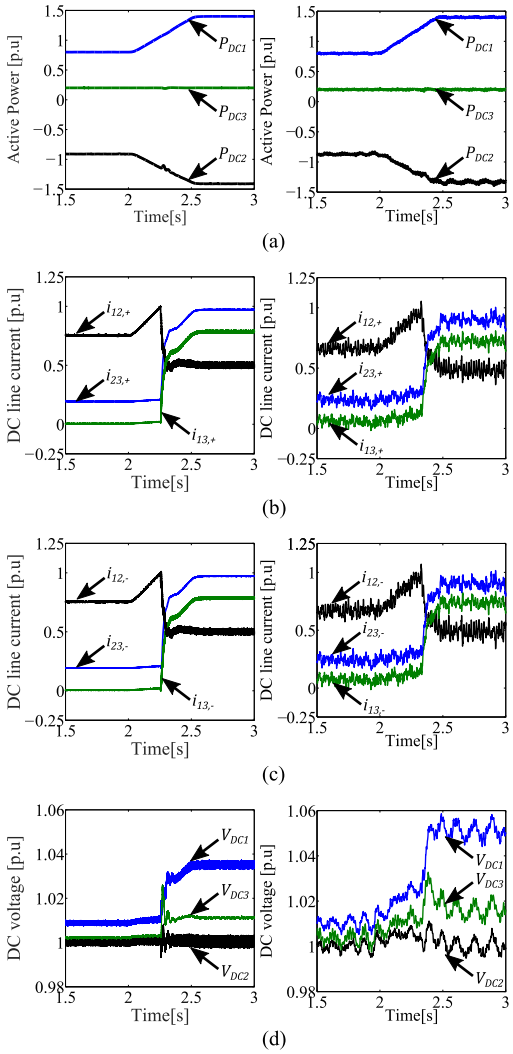

Fig. 13. DC grid response for a ramp change in power. Simulation (left) and experimental (right) results: (a) VSC active power; (b) dc line current (positive pole); (c) dc line current (negative pole); (d) dc terminal voltage.

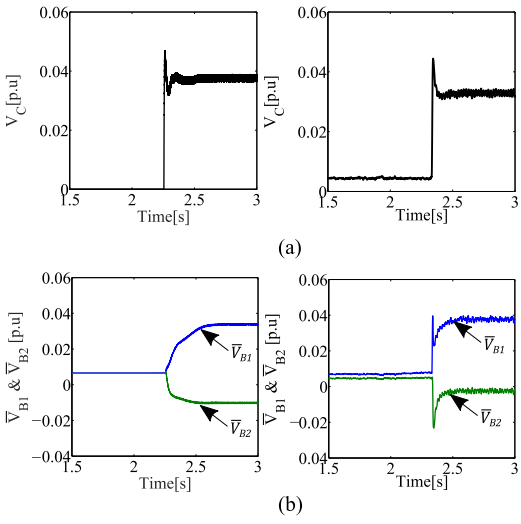

Fig. 14. Response of the CFC located at the positive pole for a ramp change in power. Simulation (left) and experimental (right) results: (a) capacitor voltage; (b) inserted average dc voltages.

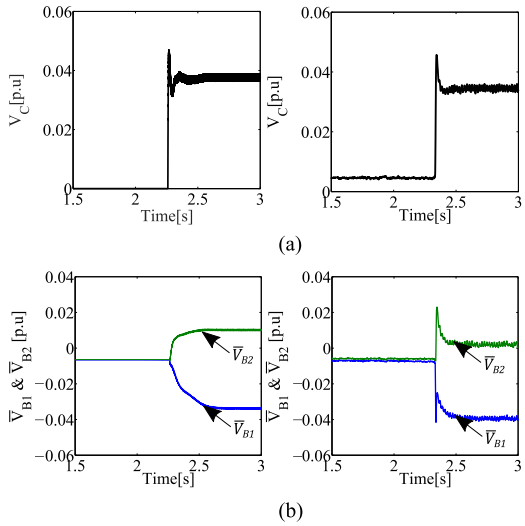

Fig. 15. Response of the CFC located at the negative pole for a ramp change in power. Simulation (left) and experimental (right) results: (a) capacitor voltage; (b) inserted average dc voltages.

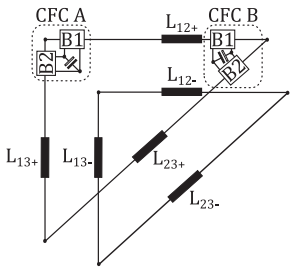

Fig. 16. DC grid with two CFCs.

dc voltages are observed across bypass switches Q_1 and Q_2 due the forward voltage drop of the diodes.

In this test case, the results have shown that a CFC can be used to protect a dc line during line overloading by controlling the line current below its thermal limit. Additionally, a CFC could be employed to reduce the amount of wind power curtailment through the rescheduling of grid power flow [24]. Another application of a CFC is to interrupt current on a specific dc line to facilitate its maintenance without interrupting the dc grid operation. Although it is expected that a CFC would incur some power losses, its benefits outweigh this shortcoming as the device can serve multiple purposes. It could be argued that the use of CFCs in dc grids may be economically feasible; however, an economic feasibility analysis is out of the scope of this paper and requires further investigation.

B. Coordinated Operation of Multiple CFCs

In this experiment, the coordination between two 2B-CFCs is examined when no communication between the LCs and the RCC exists. Fig. 16 depicts the system configuration for this test. CFC A is installed between the positive poles of lines L_{12} and L_{13}, whereas CFC B is installed between the positive poles of L_{13} and L_{23}. The voltage sharing method described in

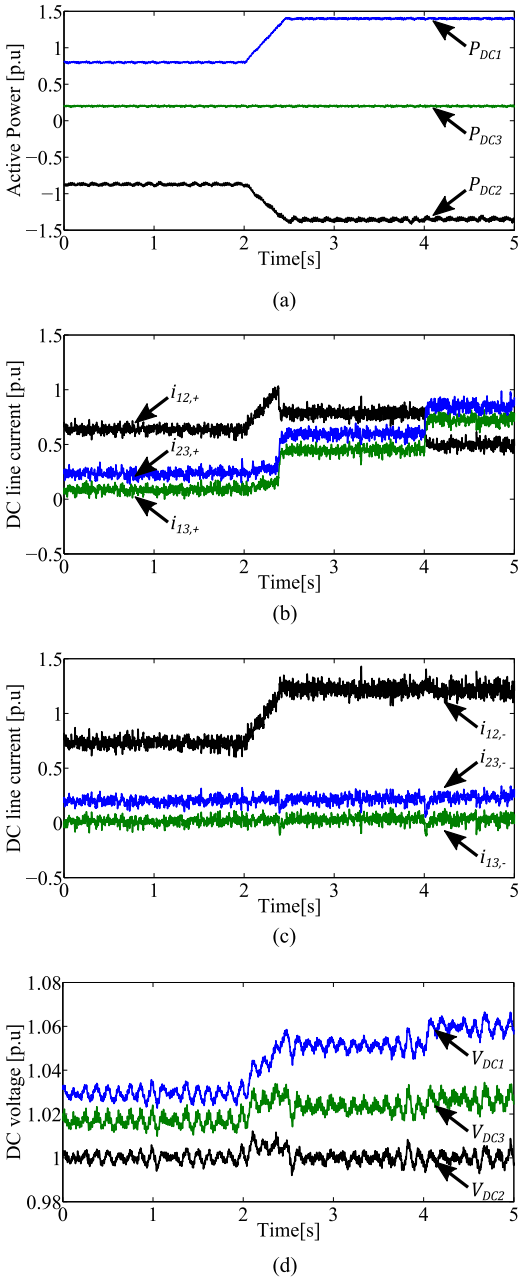

Fig. 17. DC grid response: (a) VSC active power; (b) dc line current (positive pole); (c) dc line current (negative pole); (d) dc terminal voltage.

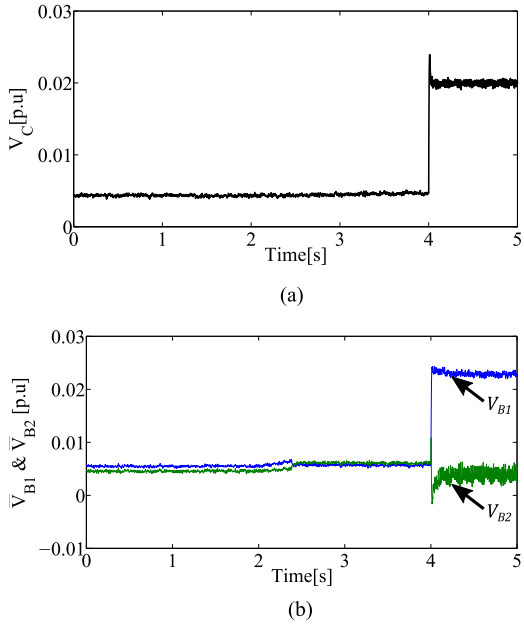

Fig. 18. CFC A response: (a) capacitor voltage; (b) inserted average dc voltages.

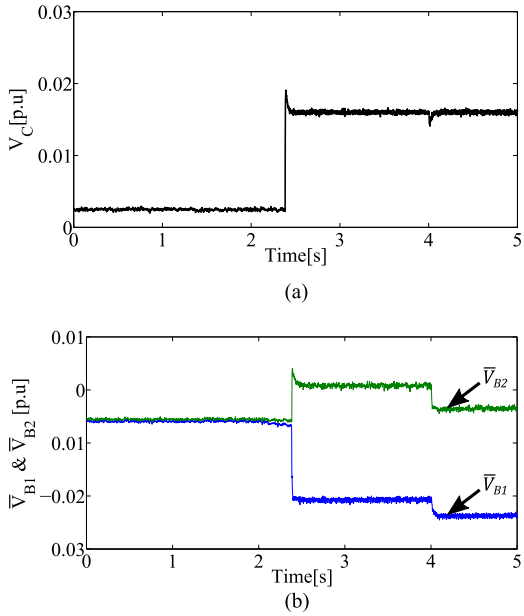

Fig. 19. CFC B response: (a) capacitor voltage; (b) inserted average dc voltages.

Section III is adopted to provide the required current control. Both CFCs are initially operated in a ZC mode. At $t = 2$ s, the power reference of VSC 1 is ramped up from 0.8 to 1.4 p.u. Since there is no communication between the CFCs and the RCC, the LCs determine the reference set-points and dictate the CFC control following the detection of an overload condition. CFC A is set to operate under a CC mode while CFC B operates under a VC mode. In CFC B, switches S_{11} and S_{22} are modulated during the VC mode as the current flows from T_2 to T_1 and T_3 to T_1. As discussed in Section II, the duty cycle of switch S_{22} is set to 1 and switch S_{11} is controlled to build up the capacitor voltage.

Fig. 17 shows the dc grid response. Following the change in set-point power (see Fig. 17(a)), L_{12+} and L_{12-} become overloaded. This is illustrated in Fig. 17(b) and (c). Once this condition is detected, CFC B is enabled to provide half of the required voltage compensation (0.016 p.u.). CFC A is enabled at $t = 4$ s to decrease i_{12+} to 0.5 p.u. so that a better current distribution is achieved. It should be emphasized that since no CFC is placed on the negative pole, L_{12-} remains overloaded. The voltage profiles of the CFCs are shown in Figs. 18 and 19. It should be recalled that two diodes are inserted in series with the

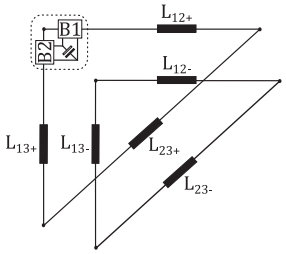

Fig. 20. DC grid arrangement under line current reversal.

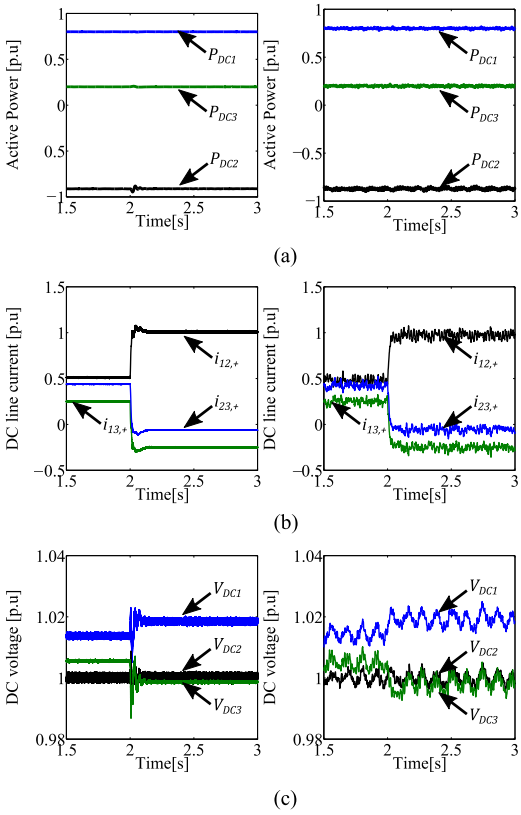

Fig. 21. DC grid response during line current reversal: (a) VSC active power; (b) dc line current (positive pole); (c) dc terminal voltage.

capacitor during a charging mode (see Fig. 3(b)). In this case, a voltage drop of 0.0065 p.u. (0.8 V) is observed across each diode. As a result, the inserted average bridge voltages $\overline{V}_{B1}$ of CFCs A (Fig. 18(b)) and B (Fig. 19(b)) are higher than their capacitor voltages. The voltage across each capacitor is nearly the same as the CFCs share the required voltage in a 1:1 ratio (see Figs. 18(a) and 19(a)).

It should be highlighted that the experiment presented in this section is an example which demonstrates the need to install a CFC in the positive and negative poles.

C. Line Current Reversal

In this experiment, a 2B-CFC is used to reverse the current flow in a dc line. Fig. 20 shows the test circuit arrangement, where the CFC is installed between the positive poles of lines L_{12} and L_{13}. Fig. 21 shows the dc grid response. Initially, the

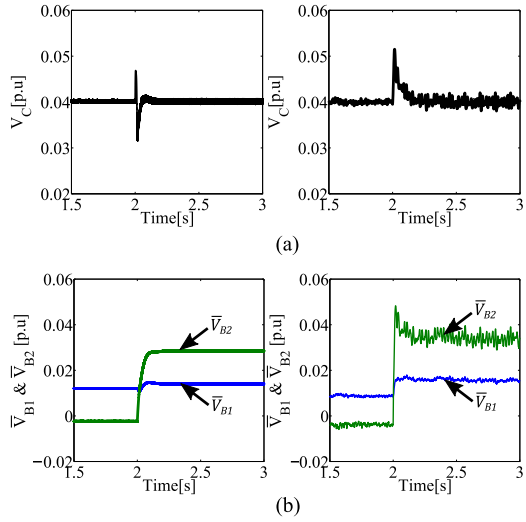

Fig. 22. CFC response during line current reversal: (a) capacitor voltage; (b) inserted average dc voltages.

CFC is in CC mode and line current i_{13+} is regulated at 0.25 p.u. During this period, switches S_{12} and S_{21} are modulated to provide independent capacitor voltage and line current control. At $t = 2$ s, the CFC is requested to reverse the current on line L_{13+} from 0.25 to -0.25 p.u. Since the active switch on each H-bridge is determined by the control objective and line current directions, switches S_{13} and S_{22} are modulated following the current reversal.

Fig. 22 shows the CFC dynamics. The capacitor voltage is regulated at 0.04 p.u. (see Fig. 22(a)). As shown in Fig. 22(b), an average dc voltage $\overline{V}_{B1}$ is inserted in series with line L_{12+} and a voltage $\overline{V}_{B2}$ with L_{13+}. Since initially the line currents are in the same direction, $\overline{V}_{B1}$ and $\overline{V}_{B2}$ have opposite polarities to maintain the power balance between bridges. A positive voltage must be inserted in series with L_{13+} to decrease the current flow. Following the reversal of i_{13+}, currents i_{12+} and i_{23+} now flow in opposite directions and, thus, $\overline{V}_{B1}$ and $\overline{V}_{B2}$ have the same polarity to maintain the power balance between the bridges.

It should be emphasized that for this example the main objective is to reverse the current flow in a dc line. Therefore, although this may not be acceptable in practice, changes on other line currents are not warranted further discussion.

D. DC Fault Performance

In MTdc grids, dc faults could lead to large transient currents due to the low dc side impedance. Therefore, the performance of a CFC under dc faults must be assessed to adequately protect the device. CFC protection is mainly determined by the fault current magnitude and the response time of bypass switches. In line with this, an experiment is carried out to evaluate the performance of a 2B-CFC under a pole-to-pole fault. As shown in Fig. 23, the fault is applied between the positive and negative poles of line L_{12}. Small-scale solid-state based DCCBs (as shown in Fig. 24) are installed at each end to interrupt the fault current. MOVs are connected across the bypass switches and the CFC capacitor to protect the device against overvoltages.

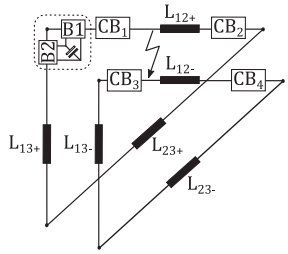

Fig. 23. Pole-to-pole fault location.

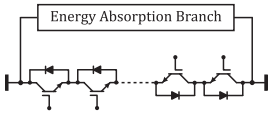

Fig. 24. Schematic of a solid-state DCCB.

TABLE III
SYSTEM STATE DURING DC FAULT

Time	System state
t_0	Pole-to-pole fault applied
t_1	Fault detected by CFC, bypass switches activated and control signals disabled
t_2	Opening of DCCBs

Among the DCCBs proposed in the literature, hybrid DCCBs exhibit high efficiency and an acceptable interruption time. With these devices, the losses during the normal operation are minimized through the use of an ultra-fast disconnector and a load commutating switch [25], [26]. However, for the experiment conducted in this section, solid-state DCCBs have been adopted due to their simplicity. Given that the main objective of the experiment is to study the performance of a 2B-CFC under a dc fault, solid-state DCCBs serve the purpose in spite of their power losses. It should be noted that a response time of 5 ms has been used to emulate that of a hybrid DCCB.

A communication-less single-ended protection strategy is used to detect the fault. The DCCBs and bypass switches are set to open and close, respectively, if the rate of change in line current is >800 p.u./s and the current magnitude is above 1.3 p.u. In addition, if the voltage across the CFC capacitor is 30% above the rated value, the CFC will be switched to a bypass mode to protect it against overvoltage. The system states during the fault are provided in Table III.

Fig. 25 shows the fault current through the CFC. During pre-fault conditions, the CFC is set to control line current i_{13} at 0.5 p.u. and capacitor voltage V_C at 0.04 p.u. (5 V). After the fault is applied at $t = t_0$, the magnitude of line current i_{12} rapidly increases and i_{13} decreases, while the CFC capacitor voltage and bridge voltages increase (Fig. 26). This occurs as the CFC tries to maintain the line current at the reference value since the fault has not been detected yet. At $t = t_1$, the fault is detected by the local protection system and the CFC transitions from a CC to ZC mode. The capacitor voltage remains constant as the H-bridges

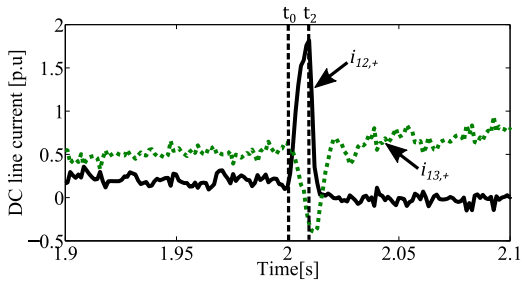

Fig. 25. Fault current through CFC.

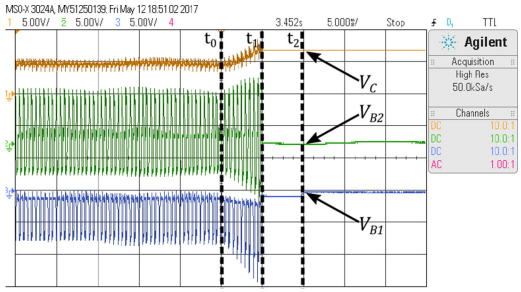

Fig. 26. CFC voltage profile.

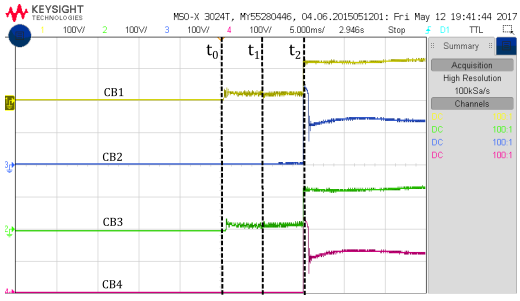

Fig. 27. DCCBs voltage profile.

are bypassed. Fig. 27 shows the voltage profiles of the DCCBs. The fault current is interrupted at $t = t_2$ by opening the DCCBs. As it can be observed, the voltage across each DCCB is equal to the pole voltage.

The results presented in this section have clearly shown that the protection of the 2B-CFC is mainly determined by the response time of the bypass switches Q_1 and Q_2 and of the DCCBs. A CFC is expected to act independently of a DCCB during a fault as no communication between them exists. In the presence of a slow DCCB, the bypass switches should have a high current rating.

It should be highlighted that a CFC can be operated in ZC mode by activating the switches of the H-bridges, but instead such an operation is implemented using external bypass switches (see Section II-A2). Although at first glance it could seem that the use of the additional switches is redundant, these are essential to ensure the correct operation of the dc grid and to protect CFC modules. Given that a CFC is a series-connected device, it should be adequately protected during fault conditions. Therefore, instead of subjecting the H-bridges of the CFC to full dc

fault currents until fault clearance, additional parallel branches with bypass switches are used instead to carry the fault current. Additionally, in the event of an internal CFC failure, the device must be bypassed to avoid any interruption to the line current flow and this is easily done with the additional switches.

VI. Conclusion

In this paper, the operation and control of 2B-CFCs have been experimentally validated in a meshed MTdc grid test-rig against simulation results. The results demonstrate that a CFC can be used to improve the grid reliability by limiting the line currents below thermal limits. A good agreement has been observed between the experimental and simulation results.

A control scheme has been proposed to achieve an effective transition from the ZC to the CC mode. Additionally, a centralized hierarchical control scheme has been presented to coordinate the operation between multiple CFCs in the MTdc grid. It has been shown that when multiple CFCs are employed, the workload of a CFC that has reached its maximum operating point can be reduced by sharing the dc voltage compensation among the other CFCs. Potential control conflicts between active CFCs can be eliminated by restricting the operation of a single CFC in CC mode and the remaining CFCs in VC mode.

For completeness, the performance of the 2B-CFC has been studied under the presence of a pole-to-pole dc fault. It has been observed that a fast protection system is required to protect the device against overvoltages and overcurrents.

Appendix

The PI controllers are represented in the form: $K(s) = K_p + K_i/s$.

Two-level VSCs: Current: $K_p = 45$, $K_i = 45000$. DC voltage: $K_p = 0.2$, $K_i = 20$. Active power: $K_p = 0.2$, $K_i = 20$. Reactive power: $K_p = 0.3$, $K_i = 10$.

2B-CFC: DC line current: $K_p = 12{\times}10^{-3}$, $K_i = 1.2$.

$$\text{Capacitor voltage: } G_k(s) = 14\left(\frac{5\times10^{-3}s+1}{2.1\times10^{-4}s+1}\right)\times\left(\frac{13\times10^{-3}s+1}{s}\right)$$

CFC Gain: $K_c = 5000$. Feedback compensation loop gain: $K_f = 0.09$.

References

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[2] D. Jovcic and K. Ahmed, *High-Voltage Direct-Current Transmission: Converters, Systems and DC Grids*. London, U.K.: Wiley, 2015.

[3] D. van Hertem, O. Gomis-Bellmunt, and J. Liang, Eds., *HVDC Grids: For Offshore and Supergrid of the Future*. Hoboken, NJ, USA: Wiley, 2016.

[4] J. Liang, T. Jing, O. Gomis-Bellmunt, J. Ekanayake, and N. Jenkins, "Operation and control of multiterminal HVDC transmission for offshore wind farms," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2596–2604, Oct. 2011.

[5] H. Wang, J. Cao, Z. He, J. Yang, Z. Han, and G. Chen, "Research on overvoltage for XLPE cable in a modular multilevel converter HVDC transmission system," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 683–692, Apr. 2016.

[6] P. Buijs, D. Bekaert, S. Cole, D. van Hertem, and R. Belmans, "Transmission investment problems in Europe: Going beyond standard solutions," *Energy Policy*, vol. 39, no. 3, pp. 1794–1801, Mar. 2011.

[7] Z. Y. Huang, J. A. Pilgrim, P. L. Lewin, S. G. Swingler, and G. Tzemis, "Thermal-electric rating method for mass-impregnated paper-insulated HVDC cable circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 437–444, Feb. 2015.

[8] C. C. Reddy, "Theoretical maximum limits on power-handling capacity of HVDC cables," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 980–987, Jul. 2009.

[9] Q. Mu, J. Liang, Y. Li, and X. Zhou, "Power flow control devices in DC grids," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, San Diego, CA, USA, 2012, pp. 1–7.

[10] E. Veilleux and B. T. Ooi, "Multiterminal HVDC with thyristor power-flow controller," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1205–1212, Jul. 2012.

[11] S. Balasubramaniam, J. Liang, and C. E. Ugalde-Loo, "An IGBT based series power flow controller for multi-terminal HVDC transmission," in *Proc. IEEE 49th Int. Univ. Power Eng. Conf.*, Cluj-Napoca, Romania, 2014, pp. 1–6.

[12] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," in *Proc. 10th IET Int. Conf. AC DC Power Transm.*, Birmingham, U.K., 2012, pp. 1–5.

[13] L. Gyugyi, K. K. Sen, and C. D. Schauder, "The interline power flow controller concept: a new approach to power flow management in transmission systems," *IEEE Trans. Power Del.*, vol. 14, no. 3, pp. 1115–1123, Jul. 1999.

[14] W. Chen *et al.*, "A novel interline DC power-flow controller (IDCPFC) for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1719–1727, Aug. 2016.

[15] M. Ranjram and P. W. Lehn, "A multiport power-flow controller for DC transmission grids," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 389–396, Feb. 2016.

[16] F. Hassan, R. King, R. Whitehouse, and C. Barker, "Double modulation control (DMC) for dual full bridge current flow controller (2FB-CFC)," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–9.

[17] H. Y. Diab, M. I. Marei, and S. B. Tennakoon, "Operation and control of an insulated gate bipolar transistor-based current controlling device for power flow applications in multi-terminal high-voltage direct current grids," *IET Power Electron.*, vol. 9, no. 2, pp. 305–315, 2016.

[18] J. Sau-Bassols, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Modelling and control of an interline current flow controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 11–22, Feb. 2017.

[19] S. Balasubramaniam, J. Liang, and C. E. Ugalde-Loo, "Control, dynamics and operation of a dual H-bridge current flow controller," in *Proc. IEEE Energy Convers. Congr. Expo.*, Montreal, QC, Canada, 2015, pp. 2386–2393.

[20] N. Deng, P. Wang, and X. P. Zhang, "Small-signal stability analysis and control system design of a meshed multi-terminal high-voltage direct current grid with a current flow controller," *Electr. Power Compon. Syst.*, vol. 44, no. 10, pp. 1126–1137, 2016.

[21] F. Hassan *et al.*, "Current flow control assembly," Patent EP 3018786 A1, May 2016.

[22] R. L. Burden and J. D. Faires, *Numerical Analysis*. Pacific Grove, CA, USA: Brooks/Cole, 2001.

[23] K. L. Lian and T. Noda, "A time-domain harmonic power-flow algorithm for obtaining nonsinusoidal steady-state solutions," *IEEE Trans. Power Del.*, vol. 25, no. 3, pp. 1888–1898, Jul. 2010.

[24] S. Wang, J. Guo, C. Li, S. Balasubramaniam, R. Zheng, and J. Liang, "Coordination of DC power flow controllers and AC/DC converters on optimising the delivery of wind power," *IET Renew. Power Gen.*, vol. 10, no. 6, pp. 815–823,7 2016.

[25] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.

[26] W. Wang, M. Barnes, O. Marjanovic, and O. Cwikowski, "Impact of DC breaker systems on multiterminal VSC-HVDC stability," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 769–779, Apr. 2016.

Senthooran Balasubramaniam (S'12) received the B.Eng. (Hons.) degree in electronic engineering from the University of Surrey, Surrey, U.K., in 2012. He is currently working toward the Ph.D. degree in electrical and electronic engineering at the School of Engineering, Cardiff University, Wales, U.K. His main research interests include HVdc technologies, power electronics, grid integration of renewable energy, and power system control and stability.

Carlos E. Ugalde-Loo (M'02) was born in Mexico City. He received the B.Sc. degree in electronics and communications engineering from Instituto Tecnológico y de Estudios Superiores de Monterrey, Mexico City, México, in 2002, the M.Sc. degree in electrical engineering from the Instituto Politcnico Nacional, Mexico City, México, in 2005, and the Ph.D. degree in electronics and electrical engineering from the University of Glasgow, Scotland, U.K., in 2009. In 2010, he joined the School of Engineering, Cardiff University, Wales, U.K., where he is currently a Senior Lecturer in Electrical Power Systems. His academic expertise includes power system stability and control, grid integration and control of renewables, HVdc transmission, modeling of dynamic systems, and multivariable control.

Jun Liang (M'02–SM'12) received the B.Sc. degree from Huazhong University of Science and Technology, Wuhan, China, in 1992, and the M.Sc. and Ph.D. degrees from China Electric Power Research Institute, Beijing, China, in 1995 and 1998, respectively. From 1998 to 2001, he was a Senior Engineer with China Electric Power Research Institute. From 2001 to 2005, he was a Research Associate at Imperial College, London, U.K. From 2005 to 2007, he was a Senior Lecturer at the University of Glamorgan, Wales, U.K. He is currently a Professor at the School of Engineering, Cardiff University, Wales, U.K. His research interests include FACTS devices/HVdc, power system stability and control, power electronics, and renewable power generation.

Tibin Joseph (S'13–M'16) received the B.Tech. and M.Tech. degrees in electrical engineering from Mahatma Gandhi University, Kerala, India, in 2008 and 2011, respectively. Since 2014, he has been working toward the Ph.D. degree in electrical engineering at Cardiff University, Cardiff, U.K., where he was also a Marie Curie Early Stage Researcher between 2013 and 2016. From 2012 to 2013, he was a Lecturer at Saintgits College of Engineering, Kerala, India. He has been a Visiting Researcher at CEPRI, Beijing, China, and at National Grid, Warwick, U.K. Dr. Joseph has been a Research Associate at Cardiff University, Cardiff, U.K., on the ANGLE-DC Project, since 2016.

Rose King (M'11) received the B.Eng. degree in electrical and electronic engineering from the University of Manchester, Manchester, U.K., in 2005, and the Ph.D degree in electrical engineering from Cardiff University, Cardiff, U.K., in 2011. She joined the National Grid Ventures in June 2017. From 2011 to 2017, she was a Lead Engineer at GE Grid Solutions. Her interests include HVdc transmission, HV cables, and power system transients. Dr. King was a member of CIGRE Working Groups B3.26 and B3.36.

Andrzej Adamczyk received the combined B.Sc. and M.Sc. degrees in electrical and engineering from the Lublin University of Technology, Lublin, Poland, in 2009, and the M.Sc. degree in power electronics and drives and the Ph.D. degree in the area of power system stability and wind power plants integration, both from Aalborg University, Aalborg, Denmark, in 2009 and 2012, respectively. Since 2013, he has been with UK Grid Solutions, a GE business, where he is currently coordinating a research group on system aspects of HVdc transmission. His field of expertise includes HVdc transmission, power system stability and control, as well as wind power technology.