A High-Reliability and Determinacy Architecture for Smart Substation Process-Level Network Based on Cobweb Topology

Xiaosheng Liu, Jiwei Pang, Liang Zhang, and Dianguo Xu, *Senior Member, IEEE*

***Abstract*—A highly reliable and deterministic process-level communication network is required to guarantee the protection switch control and data acquisition of substation automation systems (SASs), as it involves the important primary equipment in smart substations. The cobweb architecture is an artificial communication network topology based on cobwebs as they occur in nature. This study designs novel single- and dual-network architectures for process-level network for D2–1 typical smart substation based on the architecture of natural cobweb, which has structural properties that have been studied by numerical simulation and reliability theory. To demonstrate the feasibility of the process-level network based on cobweb architecture, fault tree analysis (FTA) is used to assess the reliability of the novel cobweb architecture and other traditional architectures. OPNET Modeler is used to simulate the message communication in the cobweb architecture, where the end-to-end time delay needs to conform to IEC 61850. The results of the theoretical analysis and simulation indicate that a process-level network based on cobweb architecture exhibits excellent reliability and determinacy.**

***Index Terms*—Cobweb architecture, determinacy, fault-tree analysis, OPNET modeler, process-level network, reliability, smart substation.**

I. Introduction

THE SMART substation, which is responsible for power transmission and distribution, power-flow control, and voltage adjustment, is an important foundation for power grids. IEC 61850 divides the SAS into three levels: 1) process; 2) bay; and 3) station level. Between process-level switchyard primary equipment and bay-level secondary equipment, the process-level network (which is an Ethernet-based communication network) is the only network involving primary intelligent electronic devices (IEDs) in smart substations [1]–[4]. Thus, to enhance the reliability and determinacy of SAS, the investigation of the process-level network is of great importance.

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The authors are with the School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China (e-mail: Liuxsh2004@126.com; crabpjw@126.com; xiaozhanghit@163.com; xudiang@hit.edu.cn).

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However, the process-level network is directly influenced by its topology architecture. A poorly designed network architecture limits the reliability of the network and consequently delays message delivery [5]. Available communication network architectures have already been deployed for the process-level network in many studies [6]–[9]. There are three main traditional Ethernet switch-based process level network architectures: 1) star; 2) ring; and 3) cascading topology architectures. However, these three traditional communication network architectures all have drawbacks [7], [10]: 1) for the cascading and ring architectures, end-to-end (ETE) time-delay performance for time-critical messages is nondeterministic; 2) for the ring architecture, there is a risk of a broadcast storm in the structure; 3) finally, the reliability of all three traditional architectures needs to be further enhanced. To enhance the reliability of the process level network, redundant architectures were proposed, including three derivative dual-topology architectures: dual-star, dual-ring, and dual-cascading topology architectures. However, this design concept only increases reliability through the duplication of Ethernet switch implements, without any structural changes [10]. Considering that these defects exist in traditional communication network architectures, the development of a novel and feasible communication network architecture providing high reliability and determinacy for SAS is of great interest for future investigations.

The natural cobweb, which has the advantages of spoke links and ring links in architecture, is more reliable and deterministic for the transmission of prey information than other architectures. The prominent advantage of this cobweb structure in nature is that it ensures the spider obtains prey information rapidly [11]. Based on natural cobweb structures, this study designs single- and dual-cobweb architectures of process-level networks for D2–1 typical smart substations. This novel architecture is motivated by when the main link (spoke link) is broken down, the ring links as backup would ensure the reliability and determinacy of the information transmission. Compared with the traditional architectures, the advantage of multiple backups in the cobweb architecture (redundancy links) is obvious: there are no redundancy links in the star and cascading architectures and only one in the ring architecture. To test the determinacy of each link, the OPNET modeler is used to model and simulate communication among all of the links in the cobweb architecture in this study. Furthermore, the ETE time-delay performance should conform to IEC 61850.

The objectives of this study are as follows.

1) to design a high-reliability and determinacy architecture for a substation process-level network based on single- and dual-cobweb architectures for a D2–1 typical substation;
2) to use FTA to quantitatively assess the reliability of single- and dual-cobweb architectures from the novel perspective of instrument failure and link failure and compare the reliability of traditional architectures with the novel cobweb architecture;
3) to apply the OPNET modeler to model and simulate the communication within the cobweb architecture and reflect the determinacy performance of the cobweb architecture using the ETE time-delay and other dynamic performance figures.

II. Process-Level Network Based on Cobweb Architecture

A. Process-Level Network

In a smart substation, the process-level network carries information cyclically from the primary switchyard to the human–machine interface (HMI) (e.g., voltage samples, current samples, transformer temperature, and circuit-breaker (CB) status) and from the HMI to the primary switchyard (e.g., CB tripping and closing commands) [12].

The primary switchyard is high-voltage equipment and includes busbars, CBs, isolators, power transformers, current transformers (CTs), and voltage transformers (VTs). The merging unit (MU) IED collects (from digital systems) or samples (from analog systems) the output of the CTs and VTs in the form of a sample value (SV) message [13]. The breaker IED performs the following commands: the opening/closing control of the breaker, the state and condition monitor of the CBr, and receives the trip/close command from the protect & control (P&C) IEDs. The exchange of these commands is conducted in the form of generic object-oriented substation events (GOOSE) message [14]. Hence, the messages transmitted in the process-level network are SV and GOOSE messages.

The GOOSE and SV messages are "specific communication service mappings" that can provide tangible interfaces for the abstract data model that underlies IEC 61850-based systems [15]. The GOOSE message is primarily used to transmit binary data, such as indications, alarms, and tripping signals. In contrast, the SV message is used to send instantaneous current and voltage samples from the CTs and VTs to the HMI.

B. Artificial Cobweb Architecture

The natural cobweb architecture has a spoke-ring structure, where each spoke intersects with the corresponding ring at a node and all spokes converged in the hub zone [16]. The spoke links are the main communication links that transmit prey information in a natural cobweb; however, if the main links are broken or the data flow exceeds the threshold values, this prey information can be transmitted through the ring links as a backup [17]. This special architecture is similar to the structure of modern communication networks [18]–[20]. The role of the core area in the cobweb is similar to that of the center switch in the communication network control center. Therefore, by simulating the cobweb architecture, single- and dual-layer artificial cobweb architectures were designed, as presented in Fig. 1.

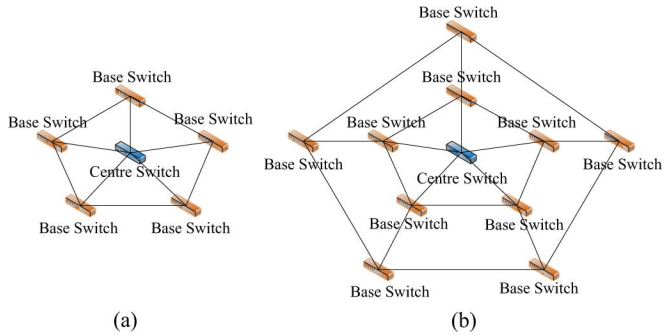

Fig. 1. Artificial cobweb architecture: (a) Single-layer cobweb architecture and (b) two-layer cobweb architecture.

According to Fig. 1, communication within the cobweb architecture is simplified based on the following hypotheses:

1) the information is first transmitted through the spoke link (a minimum number of ergodic switches);
2) the communication capacities, communication rates, and bandwidths of the spoke links and ring links are the same;
3) the switches in the architecture are of the same type;
4) the IEDs with different functions in the communication performance analysis are of the same structure.

C. Cobweb Architecture of Process-Level Network Based on a D2–1 Typical Smart Substation

1) Single-Cobweb Architecture: According to the function of the process-level IEDs, the communication connection between IEDs could be realized by Ethernet switches (ESs). The ESs in the process-level network are connected in the single-layer artificial cobweb architecture. The main connection structure of the D2–1 typical substation consists of two transformer bays (Bays T1, T2), six feeder bays (Bays F1 to F6), and one coupling bay (Bay C). Each transformer bay is composed of one MU IED, two breaker IEDs, and two P&C IEDs. The coupling bay is composed of two P&C IEDs, one breaker IED, and one MU IED. Each feeder bay is composed of one MU IED, one breaker IED, and two P&C IEDs. The process-level network is designed based on bay-oriented principles, which means that the IED in each bay connects to its own bay ES (Fig. 2). According to IEC 61850, the process-level IEDs need to exchange messages with the top network [21]. In this study, the bay and station levels are regarded as the top network.

The single-cobweb architecture is shown in Fig. 3(a). The process-level network connects to the top network through the center switch. BS and CS refer to the base and center Ethernet switches, respectively. In terms of the special structure (spoke-ring architecture) possessed by the cobweb architecture, the information is mainly transmitted through the spoke link (its own BS and CS). If the spoke link is broken, the information can be transmitted through the second-shortest ring link (neighbor BSs) as a backup to guarantee the successful transmission of the information. If the second-shortest link is also broken, the third-shortest link will be activated, and so forth. Hence, in the cobweb architecture, as long as one of the links is available, the information can be transmitted successfully. Thus, relative

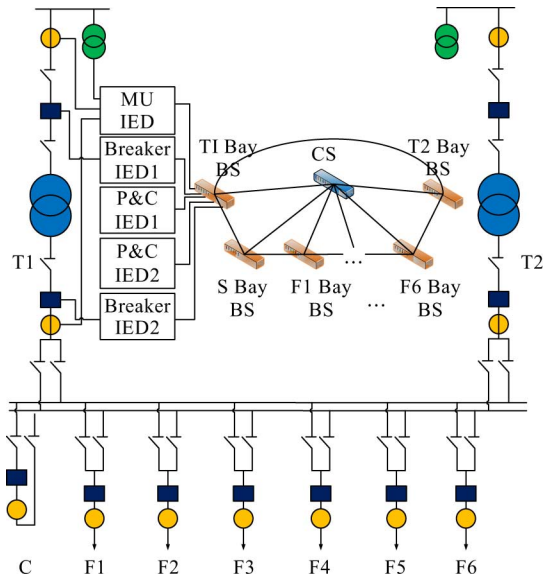

Fig. 2. Main connect structure of the D2–1 typical substation.

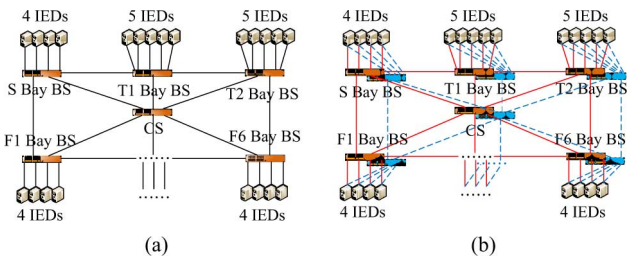

Fig. 3. Artificial cobweb architecture of the D2–1 substation process-level network. (a) Single cobweb. (b) Dual cobweb.

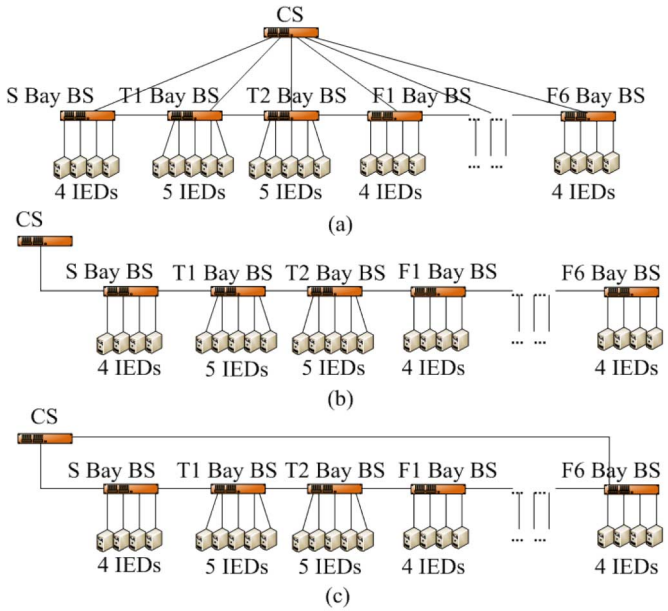

Fig. 4. Single-network architecture: (a) star architecture, (b) cascading architecture, and (c) ring architecture.

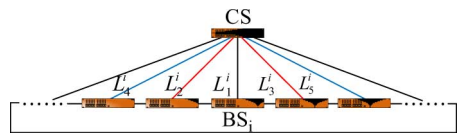

Fig. 5. Single-cobweb architecture.

to other architectures, the artificial cobweb architecture is more reliable for information transmission.

2) Dual-Cobweb Architecture: To enhance the instrument reliability of a process-level network, its architecture should include a redundancy instrument. The proposed dual-cobweb architecture, shown in Fig. 3(b), is well established based on dual-interface IEDs. Compared with the single-cobweb architecture, the dual-cobweb architecture could effectively enhance the instrument reliability of the process-level network in the structure. Fig. 3(b) shows the dual-cobweb architecture of a D2–1 substation process-level network, where the two independent cobweb architectures are marked in different colors. The two interfaces of every dual-interface IED are connected with two independent BSs.

III. High-Reliability Analysis of Cobweb Architectures

A. Reliability Analysis Based on Fault-Tree Analysis (FTA)

1) FTA: FTA is a failure-oriented method that can be used to calculate the failure degree of a substation communication system and analyze the availability and reliability of different system architectures [22]. Similar work is presented in [23], where the FTA method is applied in a large substation integration project as well as for various transmission protection architectures. The application of FTA, particularly in reliability assessment for protection systems, is presented in [24].

A communication network can be illustrated by instrument nodes (e.g., IEDs and ESs) and links, where all nodes are connected by links. The reliability of the network is decided by the reliability of the instruments and that of the links [25]. Instrument failure refers to a loss of function of the instruments that comprise the architecture; link failure refers to a failure in the communication of information in a transmission link. Previous researchers have only considered the importance of instruments (IEDs and ESs) in the architecture, neglecting the importance of links [26]–[28]. However, link failure is of the same importance as instrument failure in terms of communication failure.

Regarding link failure, there are two main aspects to be considered: 1) transmission link failure and 2) Ethernet interface failure. In smart substations, the IEDs communicate through twisted-pair Ethernet or optical fibers, and the process-level network is fixed inside the substation; thus, the probability of transmission link failure is quite low [29]. For this reason, this study only regards Ethernet interface failure (EI failure) as link failure.

The fault tree (FT) shows the logical connections between base events (BEs) with logical operators (e.g., the AND or OR operators). The top event (TE) in this study is process-level network communication failure. According to the hypotheses mentioned berfore, in this study, the FT is defined as follows:

- process-level network communication failure G;

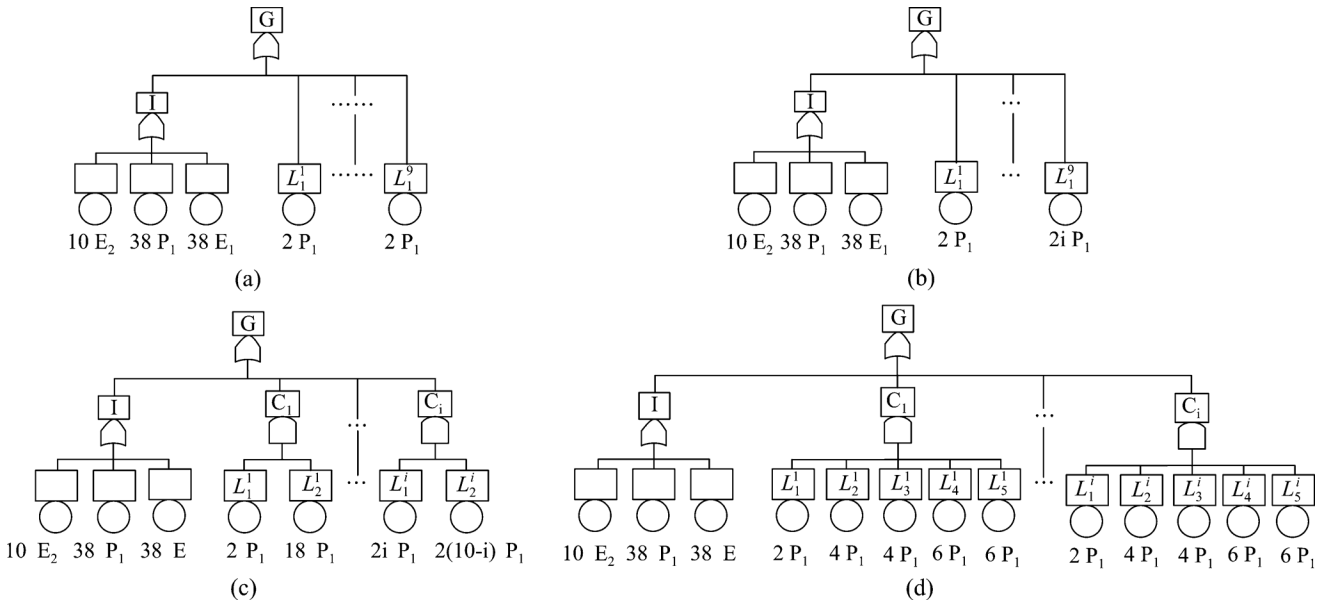

Fig. 6. FT of single-topology architectures: (a) star architecture, (b) cascading architecture, (c) ring architecture, and (d) cobweb architecture.

- instrument failure I;
- communication failure between the CS and $\mathrm{BS_i}$, C_i, where i is the number of BSs;
- link failure L_n^i, where n is the number of links connecting the CS and BS;
- IED instrument failure E_1, including MU, P&C, and breaker IEDs;
- Ethernet switch failure E_2, including the CS and BS;
- Ethernet interface failure P

where G is the OR operation result of I and every C_i.

2) Reliability Analysis Based on FTA: According to the primary structure of the D2–1 substation, the topologies of the three traditional architectures are shown in Fig. 4. There are 38 IEDs in every architecture. By connecting the same BS, all of the IEDs share the same link between the CS and BS. Each communication failure between the CS and the nine BSs would cause a process-level network communication failure; thus, i takes values from 1 to 9.

In single architectures, such as the star and cascading architectures, there is only one link between the CS and each BS (there is only one spoke link in the star architecture and one series link in the cascading architecture). n in these two architectures is $1(n = 1)$, $L_1^i = C_\mathrm{i}$. However, the differences between the star and cascading architectures are that the star architecture is symmetric about the spoke link $L_1^i = 2P$ (the communication failure between the CS and the 9 BSs is equivalent), while the cascading architecture places all of the Ethernet switches in a series $L_1^i = 2iP$ (the communication links between the CS and BSs are different).

If there is more than one link between the CS and each BS, such as in the ring architecture (two-direction cascading links) and the cobweb architecture (spoke link and ring links), communication failure is an AND operation of all C_i. In a ring architecture, there are two direction links between the CS and each BS (every C_i). The ring architecture has two links $(n = 1, 2)$, L_1^i, and L_2^i represents the communication failure of the two direction links $L_1^i = 2iP$, $L_2^i = 2(10 - i)P$.

The artificial cobweb architecture is a symmetric architecture combining the structures of the star and ring architectures. The communication between a BS and the CS is conducted through the spoke and ring links. In this study, the open shortest path first (OSPF) Dijkstra algorithm is used to select the main link and the backup links of the cobweb architecture [30]. Due to the store-and-forward working pattern of ES and the queue latency of messages in the ES, the transmission time is mainly consumed by the ESs rather than the links (in the substation, the links cannot be long enough to decide the transmission time). Thus, the fewer links through the ESs, the shorter the path [31].

According to the OSPF Dijkstra algorithm, this study chose five links for the cobweb architecture. In this cobweb architecture, n takes values from 1 to 5 $(n = 1, 2, 3, 4, 5)$. In Fig. 5, the four ring links (two symmetric ring links) are indicated by colors. The C_i includes the spoke link (L_1^i) and the four ring links (from L_2^i to L_5^i). Since the cobweb architecture is symmetric, the ring links of the same color have the same failure degree; thus, $L_2^i = L_3^i$, $L_4^i = L_5^i$. The number of P for each link is $L_i^i = 2P$, $L_2^i = L_3^i = 4P$, $L_4^i = L_5^i = 6P$. Within the analysis from before, the FT of every single-topology architecture is shown in Fig. 6.

B. Reliability Assessment

1) Reliability Assessment for Single-Network Architectures: According to the analysis from before, the reliability of the IEDs, ESs, and EIs can be designated as P_IED, P_ES, and P_EI, respectively. The process-level network communication failure degree of architecture m can be defined as $F_m(t)$, and the link failure degree of every architecture can be expressed as $F_l^m(t)$.

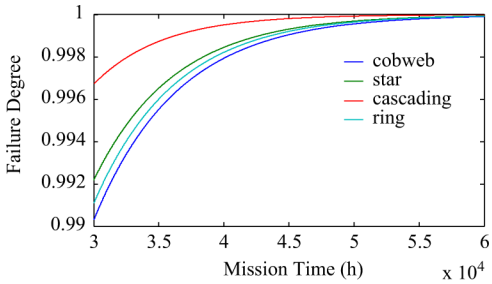

Fig. 7. Process-level failure degree versus time of single architectures.

The system failure degree of the star architecture (architecture 1) is

$$F_1(t) = 1 - P_{\mathrm{IED}}^{38}, P_{\mathrm{ES}}^{10}, P_{\mathrm{EI}}^{38}, P_{\mathrm{EI}}^{18}. \quad (1)$$

The system failure degree of the cascading architecture (architecture 2) is

$$F_2(t) = 1 - P_{\mathrm{IED}}^{38}, P_{\mathrm{ES}}^{10}, P_{\mathrm{EI}}^{38}, P_{\mathrm{EI}}^{90}. \quad (2)$$

The system failure degree of the ring architecture (architecture 3) is

$$F_3(t) = 1 - P_{\mathrm{IED}}^{38}, P_{\mathrm{ES}}^{10}, P_{\mathrm{EI}}^{38}, \prod_{i=1}^{9}[1 - (1 - P_{\mathrm{EI}}^{2i}), (1 - P_{\mathrm{EI}}^{2(10-i)})]. \quad (3)$$

The system failure degree of the cobweb architecture (architecture 4) is

$$F_4(t) = 1 - P_{\mathrm{IED}}^{38}, P_{\mathrm{ES}}^{10}, P_{\mathrm{EI}}^{38}, [1 - (1 - P_{\mathrm{EI}}^{2})(1 - P_{\mathrm{EI}}^{4})^2(1 - P_{\mathrm{EI}}^{6})^2]^9 \quad (4)$$

where $P_{\mathrm{IED}}^{38}, P_{\mathrm{ES}}^{10}, P_{\mathrm{EI}}^{38}$ decides the reliability of the instruments of the architectures, and the instrument failure for the four architectures is the same (because the number and type of the instruments are the same). The latter part of the formulas is the link reliability $1 - F_L^m(t)$, which is decided by the links of every architecture.

If the failure rate of component i is constant, the reliability of the instrument is expressed as

$$P_i(t) = e^{-\lambda_i t}. \quad (5)$$

where λ_{i} is the failure rate of instrument i.

The failure rates of the components are shown in Table I [26], [32]. According to the reliability analysis, the single-architecture system failure degree versus time is shown in Fig. 7, and the link failure degree versus time is shown in Fig. 8.

The reliability of architecture m is calculated by

$$R_m(t) = 1 - F_m(t). \quad (6)$$

Fig. 9 shows the mean time to failure (MTTF) of all architectures. The MTTF can be defined as

$$\mathrm{MTTF} = \int_0^{\infty} R_m(t)dt. \quad (7)$$

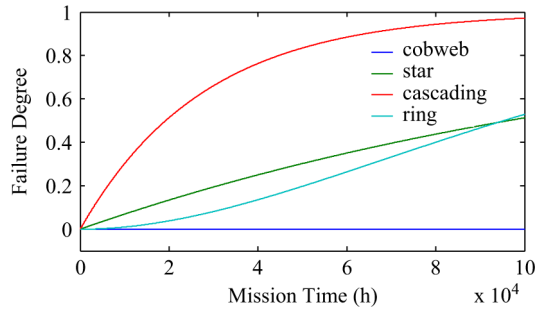

Fig. 8. Link failure degree versus time of single-network architectures.

TABLE I
APPROXIMATE UNAVAILABILITY OF PROCESS-LEVEL COMPONENTS

Component	MTTF(yr)	Failure Rate λ (multiply by 10^{-6})(h^{-1})
ES	11.5	9.9
EI	300	0.4
IED	103.5	1.1

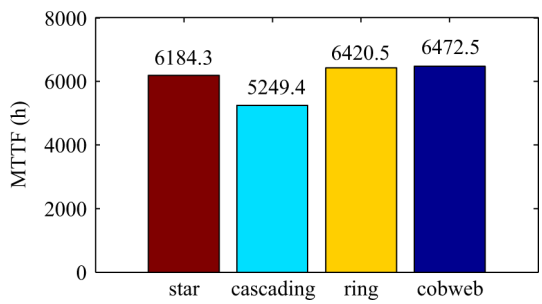

Fig. 9. MTTF of single-topology architectures.

Fig. 7 shows the process-level network communication failure degree versus time of single-network architectures. The process-level network communication failure degree of all architectures increases with the mission time. However, the increase for the cobweb architecture is the slowest, indicating that the reliability of the cobweb architecture is higher than that of the other traditional architectures.

As shown in Fig. 8, the link failure degree of the three traditional architectures increases with the mission time. However, the link failure of the cobweb architecture is still nearly 0 at a mission time of 10^5 h. This high reliability demonstrates that the redundancy links in the cobweb architecture can successfully maintain the communication transmission. Meanwhile, along with instrument failure, the link failure of an architecture would result in a process-level communication network failure. The artificial cobweb architecture can successfully solve the link failure problem; hence, the overall reliability of the process-level communication network could be enhanced.

According to Fig. 9, the reliability of the cobweb architecture is the highest, with an MTTF of 6472.5 h, followed by the ring architecture, with an MTTF of 6420.5 h. The star architecture, which has already been applied to a process-level network in a smart substation in China, has an MTTF of 6184.3 h, which is 4.66% (288.2 h) lower than that of the cobweb architecture.

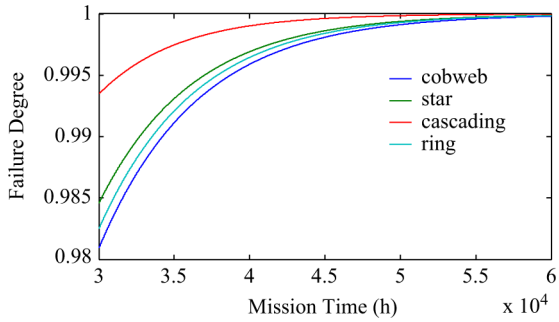

Fig. 10. Process-level failure degree versus time of dual-network architectures.

TABLE II
PROCESS-LEVEL NETWORK RELIABILITY AT 1000-h MISSION TIME

Topology architecture		Reliability
Single-network	Star architecture	85.07%
	Cascading architecture	82.65%
	Ring architecture	85.67%
	Cobweb architecture	85.69%
Dual-network	Star architecture	94.76%
	Cascading architecture	94.15%
	Ring architecture	94.88%
	Cobweb architecture	94.90%

Regarding service time, the cobweb architecture has good economic performance, maintaining the highest service time at the same cost.

2) Reliability Assessment for Dual-Network Architectures: In previous studies, dual-network architectures are used to reduce instrument failure. However, the dual-topology architecture of the process-level network is not simply the duplicate of the single-topology architecture. In the dual-topology architecture, there are two BS instruments from two independent networks connected with one set of IEDs through a dual interface [Fig. 3(b)]. The failure of the dual-topology architectures is not the square of the single failure degree; hence, from an instrument failure viewpoint, the process-level communication failure can be reduced using a dual-topology architecture. Considering the link failure in dual-topology architectures, the expression in the dual-topology architectures is the same as that in the single-topology architectures. According to the aforementioned analysis, the failure degree of the dual-topology architectures is shown

$$F_m(t) = 1 - 2 \cdot P_{\mathrm{IED}}^{38} \cdot P_{\mathrm{ES}}^{10} \cdot P_{\mathrm{EI}}^{38} \cdot F_L^m + (P_{\mathrm{IED}}^{38} \cdot P_{\mathrm{ES}}^{10} \cdot F_L^m)^2 \cdot P_{\mathrm{EI}}^{38}. \quad (8)$$

The system failure degrees of the dual-network architectures are shown in Fig. 10. Comparing the reliability of the eight architectures at a mission time of 1000 h, the reliability of the dual-network architectures is higher than that of the corresponding single-network architectures (Table II). Moreover, the cobweb architecture showed the highest reliability in the single- and dual-topology architectures: 85.67% for the single-cobweb architecture and 94.90% for the dual-cobweb architecture.

C. Discussion

1) The probability of link failure of the cobweb architecture is much lower than that of the traditional architectures. With the rapid development of complicated link architectures in smart substations [33], the exploitation of more reliable network architectures has already played an irreplaceable role in the substation communication field. As shown in Fig. 8, with increasing mission time, the link failure of the traditional architectures gradually increased. All of the traditional architectures exhibited a trend of exponential growth, whereas the link failure of the cobweb architecture remained at 0 at a mission time of 10^5 h. For example, at a mission time of 10^5 h, the failure degree of the cobweb architecture was 0, whereas that of the cascading architecture was 0.97, that of the star architecture was 0.51, and that of the ring architecture was 0.53. Hence, with the rapid development of smart substations, the cobweb architecture's high reliability is promising for practical applications.
2) The MTTF of the cobweb architecture is much higher than that of the traditional architectures. In Fig. 9, the MTTFs of single- and dual-cobweb architectures are 6472.5 h and 9217.9 h, respectively. In comparison with the MTTFs for the single- and dual-star architectures (6184.3 h and 8831.3 h, respectively), which have already been used in the construction of smart substations, the MTTFs for the single- and dual-cobweb architecture are 4.66% and 4.38% greater, respectively.
3) The cobweb architecture has more significant structure features and economic advantages than the traditional architectures. According to the cost-effective theory [35], the calculation of economic benefits for cobweb architecture is given by

$$E = \frac{\Delta WASRI}{C} \quad (9)$$

where, in this paper, $\Delta WASRI$ represents the MTTF of every architecture, and C represents the cost of building a communication network in a smart substation. In China, the star topology is widely used in communication network construction in substations, where the cost for the communication network construction is U.S.$0.5 million/smart substation [34]. The MTTFs of the single- and dual-cobweb topologies are higher than those of the single- and dual-star topology by 4.66% and 4.38%, respectively. Thus, from a service-life perspective, one smart substation can save $0.5 * 4.66\%$ U.S.$ and $0.5 * 4.38\%$ U.S.$ using single- and dual-cobweb architectures. In China, the 12th Five-Year Plan, which began in 2011, has already put forward new policies on the expansion of the number of smart substations. This plan entails the construction of 7500 smart substations within five years in China [34]. Therefore, the total savings using single- and dual-cobweb architectures will be $7500 * 0.5 * 4.66\% = 174.75$ U.S.$ million and $7500 * 0.5 * 4.38\% = 164.25$ U.S.$million, respectively, without including other annual expenses, such as maintenance costs and human costs. Hence, considering the enormously high expense, the development of a cost-efficient architecture, such as the cobweb architecture, has

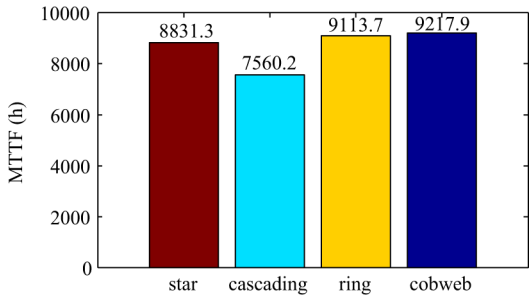

Fig. 11. MTTF of dual-topology architectures.

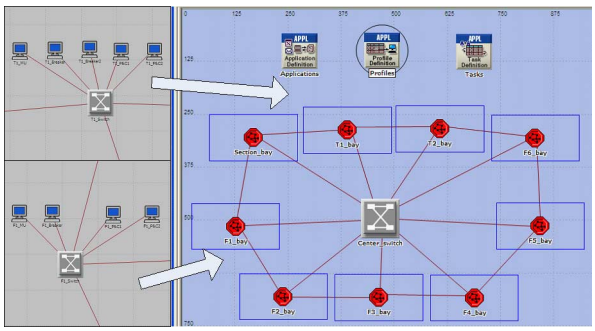

Fig. 12. OPNET modeling of the process-level network based on single-cobweb architecture.

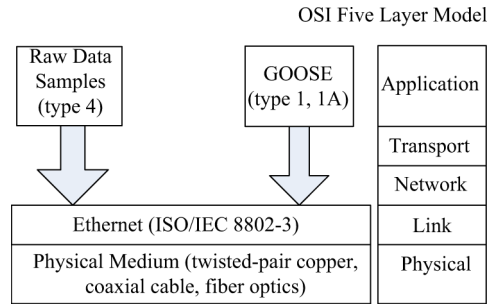

Fig. 13. Message communication stack in IEC61850.

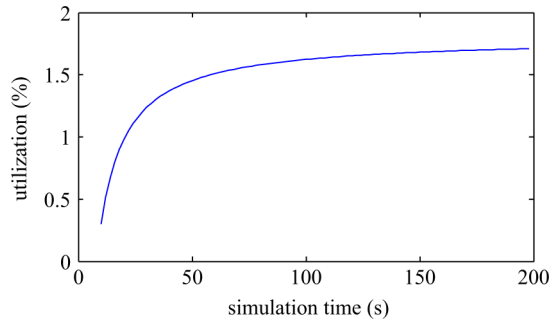

Fig. 14. Bandwidth utilization during the simulation.

become one of the most important challenges in the substation communication field.

IV. Determinacy Analysis of Cobweb Architecture With the Opnet Modeler

According to the main connection structure shown in Fig. 2, the process-level network based on a single-cobweb architecture is constructed by the project editor on the OPNET modeler according to IEC 61850 (Fig. 12). Each feeder bay, transform bay, and coupling bay is modeled into one subnet, which contains a number of breaker IEDs, MU IEDs, and P&C IEDs and one ES. In terms of the structures of the single- and dual-cobweb architectures (Fig. 1), the communication performance of the dual-cobweb architecture is the same as that of the single-cobweb architecture. Hence, in this study, the simulation for the single-cobweb architecture is presented as an example.

The ES in Fig. 12 is an Ethernet16_switch OPNET model featuring 16 interfaces with full-duplex communication at the rate of 100 Mb/s. The ESs work in a store-and-forward mode, meaning that a switch receives multiple data, stores the data, and sends each datum sequentially from one output port. This modeler node can realize the functions of the industrial ES.

As Fig. 12 shows, there are three types of IEDs in the process-level network. The functions of the IEDs are depicted above. The modeler in OPNET: the Ethernet Station can set the frame format, frame size, start time, stop time, and sequence. Hence, this study uses the Ethernet Station Modeler in OPNET as IEDs to realize sending and receiving messages. The messages sent and received by the Ethernet Station adhere to the communication stack specified in IEC 61850. According to IEC 61850, the messages transmitted through the process-level network are GOOSE message (type 1, fast speed message, 1A) and SV message (type 4, raw data message). The communication stack for the two categories of messages is shown in Fig. 13.

According to the definition and typical data field length of SV and GOOSE messages, the sizes of the SV and GOOSE messages are 58 and 162 B, respectively. The sampling rate of SV is 960 Hz, and the interarrival time of GOOSE is 0.5 ms [36].

A. Simulation of the Process-Level Network Based on Cobweb Architecture

Here, a simple operation is used as an example [14]. In this operation, one fault causes the two P&C IEDs in F1 to send GOOSE messages to the operating control breaker IED. In addition, the breaker IED sends GOOSE messages to the corresponding P&C IED. Simultaneously, the MU IED of the F1 bay continuously transmits CT and VT signals in the form of SV.

Completing the network configuration as analyzed before, the simulation time is from 10 to 200 s. The ETE time delay for these two time-critical messages is selected as a key statistic to evaluate the real-time performance of the proposed process-level architecture. The IEC 61850 sets a maximum ETE delay of 3 ms for these two messages.

B. Analysis of Simulation Results

Fig. 14 shows the bandwidth utilization of the network. The bandwidth utilization tends to increase with time, but as the messages transmitted in the process-level network are small, the total utilization of the bandwidth is limited. Fig. 15 shows the packet time delays during the simulation. At the beginning of the simulation, the IEDs send their own messages to the CS together; thus, there is a burst of messages at 10 s, and the packet time delay is nearly 0.0635 ms. As the simulation continues, the

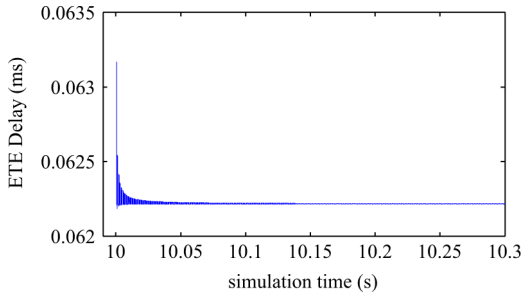

Fig. 15. ETE time delay for packets' communication during the simulation.

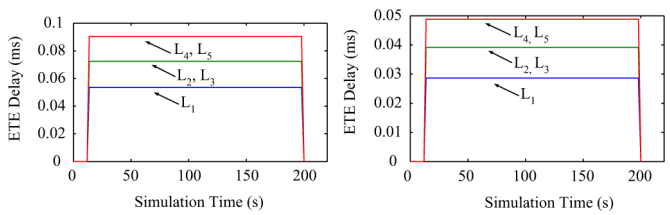

Fig. 16. ETE time delay for messages in the process-level network: (a) GOOSE message and (b) SV message.

time delay tends to remain at 0.0623 ms. The time delay after 10.3 s behaves identical to that between 10.1 and 10.3 s; therefore, this study uses the intercept data from 10 to 10.3 s. The packet time delay during the simulation is less than 3 ms, conforming to the IEC 61850 standard.

According to the reliability analysis from before, the messages can transmit through either the spoke link or the other four ring links. The simulation of these five communication links is conducted by the OPNET modeler, and the ETE time delay performances are analyzed. In the single-cobweb architecture, which is a symmetric structure based on spoke links, the ETE time delay of L_2 and L_3 and of L_4 and L_5 is the same. In Fig. 16, we can see that the spoke link (L_1) ETE time delay of an SV or GOOSE message is much less than 3 ms. As the number of Ethernet switches increases, the ETE time delay of the different ring links also increases. However, all of the ETE time delays are less than 3 ms. Hence, in this study, the real-time performance of the cobweb architecture conforms with the IEC 61850 standard. The simulation results show that the cobweb communication network topology has potential applications.

V. Conclusion

This study presents a novel process-level network architecture for a D2–1 typical substation based on cobweb in nature, including single- and dual-cobweb architectures. Compared with the traditional architectures, the reliability of the single- and dual-cobweb architectures is higher. The communication determinacy is simulated by the OPNET modeler. The conclusions obtained in this study are as follows.

1) The link reliability of the cobweb architecture is quite high compared with the traditional architectures. The special redundancy communication link structure in the cobweb architecture can guarantee the transmission of the messages with high reliability. In this special structure, as long as at least one spoke-ring link is functional, the messages transmitted in the process-level network can be successfully communicated with the SAS. At a mission time of 10^5 h, the failure degree of the cobweb architecture was 0, whereas those of the cascading, star, and ring architectures were 0.97, 0.51, and 0.53, respectively. The cobweb architecture features a markedly high link reliability. Hence, with the rapid development of smart substations, this cobweb architecture is promising for practical applications.
2) The reliability of the process-level communication network based on the cobweb architecture is higher than that based on traditional architectures. Considering the link failure and instrument failure as the comprehensive causes of process-level network communication failure, the cobweb architectures, whether single or dual cobweb, are the most reliable among the existing architectures. This cobweb architecture has been demonstrated to possess higher reliability in process-level network communication.
3) The cobweb architecture performs well in determinacy communication by the OPNET Molder. In the cobweb architecture, there are many redundancy communication links to guarantee the successful communication between the process-level network and SAS. According to the simulation results, the ETE time delay of all links conforms to the IEC 61850 standards (a maximum of 3 ms). The high-performance cobweb architecture has proven to be a safe architecture for use in protection and control applications with good determinacy performance.
4) The cobweb architecture is more economical than traditional architectures. Considering the economic factors in China, the cobweb architecture would save $U.S.174.75 and $U.S.164.25 million compared with the single- and dual-star architectures under the same MTTF. Therefore, with its higher reliability and determinacy and lower cost, the application of the cobweb architecture in process-level communication networks in smart substations is promising.

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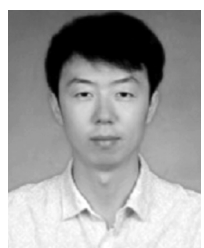
Xiaosheng Liu is a Professor in the Department of Electrical Engineering, Harbin Institute of Technology, Harbin, China. His main interests and research fields include power-line communication and its routing methods, communication networks and control technology, and information and communication of smart grids.

Jiwei Pang is currently pursuing the Ph.D. degree in electrical engineering at Harbin Institute of Technology, Harbin, China.

His main interests and research fields are smart-grid communication, communication in smart substations, and communication networking technology of smart grid.



Liang Zhang is currently pursuing the Ph.D. degree in electrical engineering from Harbin Institute of Technology, Harbin Institute of Technology, Harbin, China.

His main interests and research fields are power-line communication networking technology and communication of smart grid.

Dianguo Xu (SM'12) is a Professor in the Department of Electrical Engineering, Harbin Institute of Technology, Harbin, China. His current research interests include robotics, lighting electronics, power-quality mitigation, consumer electronics, power electronics, and motor drives.

Dr. Xu is a member of the China Electrotechnical Society and China Power Supply Society.