Power Capability Domain Analysis for M2DC-Based AC/DC/DC Multi-Port Converter

Daniele Falchi, Eduardo Prieto-Araujo, *Senior Member, IEEE*, and Oriol Gomis-Bellmunt, *Fellow, IEEE*

***Abstract*—This paper addresses the power capability domain calculation for the specific M2DC-based AC/DC/DC multi-port converter. Such a power capability domain will represent all the possible power flow scenarios (comprehensive of active and reactive power components) the converter can withstand without exceeding the physical limitations (due to the established ratings of installed components, e.g., semiconductors current and voltage). Concerning conventional two-port modular multilevel converters, the $P-Q$ power capability curve is one of the most common tools employed to track the safe operating region of the converter. However, the increased number of ports and the topology changes on multi-port converters lead to evaluating and representing the power capability domain in a non-conventional way. This article evaluates the power capability of the specific M2DC-based AC/DC/DC asymmetrical monopole converter. Moreover, internal converter asymmetries are considered in the study to express analytical voltages and current behaviour as a function of terminals powers. Then, the power capability domain is calculated and represented for a use-case scenario in which the multi-port converter interconnects High Voltage DC and Medium Voltage DC networks to the AC transmission network. The study also includes power capability domain modifications under port contingencies scenarios, such as fault and port disconnection.**

***Index Terms*—HVdc, MVdc, multi-port converters, capability curve.**

I. Introduction

POWER systems, in recent years, are facing relevant transformations, either structurally and conceptually, to include higher percentages of variable energy sources and increase interconnectivity. In order to help in stability, flexibility and footprint reduction, DC technologies are intended to be increasingly included to the system. In this direction, High Voltage DC (HVdc) technology is already mature for offering a backbone for transmission systems. Recently, also Medium Voltage DC (MVdc) technology is being considered to contribute in the expansion of the grid as depicted in references [1] and [2]. In this regard, energy island, hydrogen sector and railway applications, [3] and [4], are getting a rising interest.

In this upcoming scenario, power electronics (PE) based technologies are getting increasingly absorbed by power systems. Modular Multilevel Converter (MMC) topology, originally proposed in [5], is the state-of-the-art converter technology for High Voltage DC applications and not only [6], [7].

Nevertheless, the points mentioned above, together with the interest in keeping the system as compact as possible and avoiding redundant energy conversion stages, raise a particular interest on multi-port converter solutions interconnecting multiple networks. Recently, recognized efforts have been started on modular multilevel multi-port converter topologies studies [8], [9], [10], [11], [12], [13]. While reference [8] presents a review on the existing topologies and their possible applications, references [9], [10], [11], [12] offer more details in terms of modelling and control of several multi-port converter arrangements. Three main concepts are behind the existing multi-port AC/DC/DC converter topologies: one is the so-called F2F-based converter (derived from the Front to Front DC/DC converter [14]), that is considered a fully isolated converter. One is the so-called HVDC-AT-based converter (derived from HVDC-AT DC/DC converter [15]), where AT refers to autotransformer concept analogy, and it is a non-isolated topology. One is the so-called M2DC-based (derived from M2DC DC/DC converter [16]), where M2DC means modular multilevel direct current converter, and it is a non-isolated topology. However, due to the novel concepts behind such proposed modular multilevel based multi-port converters, open research questions are still do be addressed, one of those is the power capability domain calculation.

The power capability is a very important tool used by engineers to understand the safe possible operation regions of power equipment in power applications. The power capability allows to see where are the limits and how different key parameters influence the operation regions of equipment. Several references have explored capability curves for synchronous generators [17], [18], power converters [19] and Modular Multilevel Converters [20], [21], [22]. For multi-port converters, reference [23] addressed the power interdependency between ports, but it does not consider reactive power provision and was not including MMC based topologies. Multi-port converters capability curves, considering MMC-based topologies and reactive power provision have not been explored. In this case, the challenge of addressing the interdependency of more than two variables raises the need to go beyond 2D representation.

Manuscript received 2 October 2023; revised 5 February 2024; accepted 21 April 2024. Date of publication 14 May 2024; date of current version 25 July 2024. This work was supported by the French TSO, RTE (Réseau de Transport d'Electricité), R&D division. The work of Oriol Gomis-Bellmunt was supported by the Institució Catalana de Recerca i Estudis Avançats (ICREA), Academia Program. Eduardo Prieto-Araujo is member of the Serra Húnter programme. Paper no. TPWRD-01379-2023. *(Corresponding author: Daniele Falchi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPWRD.2024.3400951.

Digital Object Identifier 10.1109/TPWRD.2024.3400951

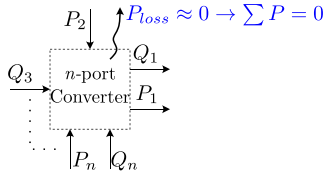

Fig. 1. Power flow representation of an n-port converter.

With the purpose of contributing in this direction, the article proposes the power capability domain calculation for the specific M2DC-based AC/DC/DC converter, introduced in [10].

Aiming to have a deeper understanding on the converter capabilities, after the power capability analysis in normal operation, it is fundamental to understand how the presence of severe disturbances as faults and port disconnection impacts on the feasible power capability of the multi-port converter. In fact, according to converter capabilities, during a contingency at one port, the converter should be able to provide continuity of operation among the other ports.

Main contributions are summarized below:

- Intrinsic asymmetric branch behaviour is considered for the proper calculation of current and voltage limits per branch. The influence of asymmetries is a non-common factor and a non-intuitive effect. In fact, for conventional AC/DC Modular Multilevel Converters, for the $P-Q$ curve calculation, upper and lower branches are mostly considered behaving symmetrically. The steady-state model presented in the article is intended to demonstrate the asymmetrical branch behaviour.
- Power capability domain obtention for the specific M2DC-based AC/DC/DC converter considering both active and reactive power components. A 3D-power capability domain is achieved. Thus, the power capability domain boundaries enclose all the possible power flow scenarios performed among the three connected systems.
- Contingencies at ports are included in the power capability domain analysis. To be specific, symmetric voltage sags at AC network, pole to ground short circuit at DC networks and port disconnections are the selected contingencies. Power capability will provide information on the converter feasibility to operate during such scenarios.

Moreover, the power capability domain allows manufacturers of multi-port converters to define the capabilities of their converters. It also allows operators to understand what they can do with converters and helps them to define specifications for future projects and include them eventually in future grid codes.

II. General Assessment on Power Capability Domains

It is necessary to establish the domain in which the power capability will be placed. The dimension of this domain strictly depends on the number of independent powers; it is worth to inform that an AC port can counts active and reactive power terms. In Fig. 1 is a representation of an n-port converter with terminals powers under the assumption that losses are negligible.

Having assumed negligible losses, Equation (1) establishes the power capability domain dimension, n_D. The (1) is intended to be valid for any converter, it does not refers to a specific converter topology or a specific application.

$$n_D = N_{dc,ports} + 2N_{ac,ports} - 1. \tag{1}$$

(1) considers that the sum of all active powers has to be zero, thus, the converter does not face any energy deviation.

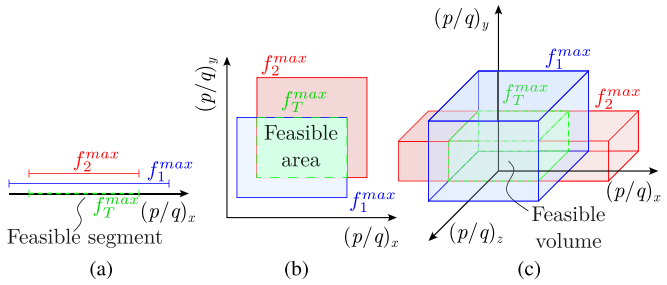

Fig. 2. Representative illustrations of power capabilities domains: 1D-feasible power segment in (a), 2D-feasible power area in (b) and 3D-feasible power volume in (c).

Fig. 2 depicts three representative illustrations of power capability domains; number of the axis is related to the number of ports and their nature (1). Fig. 2(a) represents a power capability domain placed on one axis (it can be representing the P power capability segment for a DC/DC converter). Fig. 2(b) represents a power capability domain placed on two axes (it can be representing the common $P-Q$ power capability curve for an AC/DC converter). Fig. 2(c) represents a power capability domain placed on three axes. Functions $f_1^{\max}$, $f_2^{\max}$ (*e.g.*, $v_1^{\max}$, $i_2^{\max}$) describe the feasible power operating domain based on their maximum allowable values. The function $f_T^{\max}$ represents the intersection of all the feasible operating points among the selected functions $f_1^{\max}$, $f_2^{\max}$.

Below, the study introduces two power capability domain examples referring to two two-port converters: DC/DC MMC and AC/DC MMC.

A. MMC DC/DC Converter: 1D Power Capability Domain

In literature, the most typical DC/DC converter for high voltage DC applications was proposed in [24]. Referring to the power capabilities, based on the (1), the power capability domain will be placed on one axis. That axis represents the power transferred between the two connected DC systems. Hence, current and voltage variables are calculated based on the unique power. However, the asymmetric branch DC power distribution leads the converter to use an internal AC power component component to balance such an internal energy deviation between upper and lower branches. Therefore, the branches manage DC and AC current-voltage components.

1) Current Limit Equations: For a given system, three-legs-based, as depicted in Fig. 3(a), the upper and lower branch current is function only of power exchanged between the two connected DC systems. $K_v = \dfrac{V_{2,dc}}{V_{1,dc}}$ indicates the DC voltage

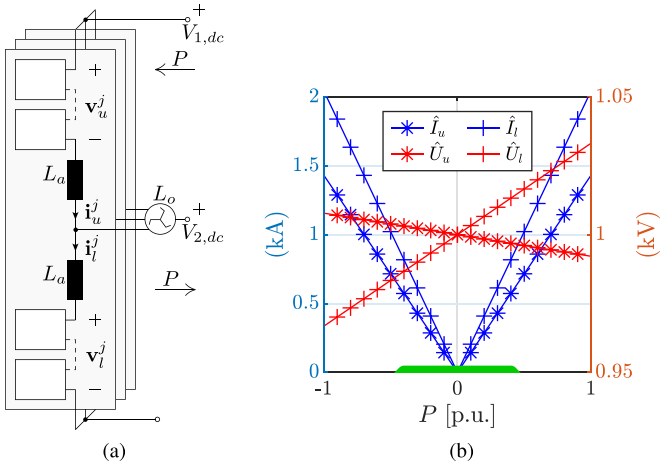

Fig. 3. MMC DC/DC converter scheme in (a) and, in (b), the power capability (green segment) respect to the upper-lower current limitations (blue lines) and upper-lower voltage limitations (red lines) at $K_v = 0.25$.

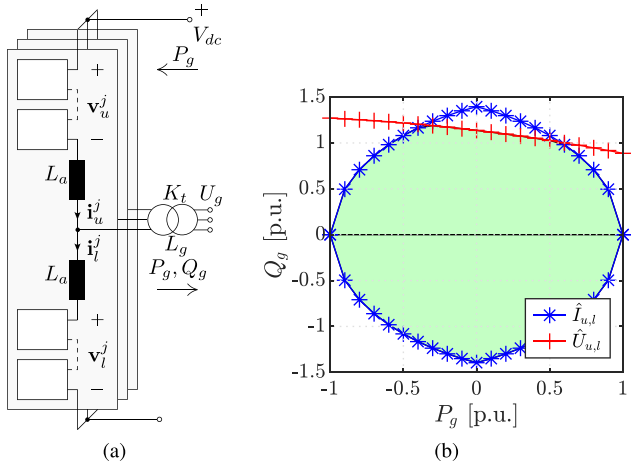

Fig. 4. MMC AC/DC converter in (a) and, the green region in (b) is the feasible power capability area considering $R_e \neq 0$.

step ratio between terminals.

$$\hat{I}_u^j = \underbrace{\frac{P}{3V_{1,dc}}}_{DC} + \underbrace{\sqrt{2}\frac{P\,(1-K_v)}{3U_{ac}}}_{AC}, \tag{2}$$

$$\hat{I}_l^j = \underbrace{\frac{P}{3V_{1,dc}}\frac{K_v-1}{K_v}}_{DC} + \underbrace{\sqrt{2}\frac{P\,(K_v-1)}{3U_{ac}}}_{AC}. \tag{3}$$

2) Voltage Limit Equations: The upper and lower branch voltage is function only of power exchanged between the two connected DC systems.

$$\hat{U}_u^j = \underbrace{V_{1,dc}\,(1-K_v) - \frac{P\,(K_v R_a + R_o)}{3K_v V_{1,dc}}}_{DC} + \underbrace{U_{ac}}_{AC}, \tag{4}$$

$$\hat{U}_l^j = \underbrace{V_{1,dc}K_v - \frac{P\,[R_o - R_a(K_v-1)]}{3K_v V_{1,dc}}}_{DC} + \underbrace{U_{ac}}_{AC}. \tag{5}$$

Where U_{ac} is typically chosen to keep the circulating AC current at minimum and reducing semiconductors stress. R_a and R_o are the branch resistance and zig-zag transformer resistance respectively. The green feasible power segment depicted in Fig. 3(b) highlights the feasible range of power that the two DC systems can exchange.

B. MMC AC/DC Converter: 2D Power Capability Domain

The section aims to briefly introduce how capability domain for a two-port AC/DC MMC looks like and, what are the variables used to depict the final capability surface of feasible operating area for given current-voltage ratings. The AC/DC MMC converter in [5], operating under balanced conditions presents upper and lower branches behaving symmetrically.

Based on (1) (losses negligible), the power capability is placed on two axis ($P-Q$). U_g represents the phase-to-phase rms voltage of the AC connected system while V_{dc} is the voltage of the DC connected system. K_t indicates the transformer winding step ratio between primary and secondary while the other parameters are defined as follow: $\gamma = X_e P_g$, $\epsilon = R_e Q_g$, $\delta = X_e Q_g$ and $\rho = R_e P_g$ with $X_e = X_g + \frac{X_a}{2}$ and $R_e = R_g + \frac{R_a}{2}$. Branch variables have been calculated keeping branches energetically stable: $P_{u,l}^{ac} = P_{u,l}^{dc}$.

1) Current Limit Equation: For a given system, three-legs-based, as depicted in Fig. 4(a), due to the symmetry, Equation (6) does express the current limitation depending on the power flow (P_g and Q_g) either for upper and lower branches for a generic phase j.

$$\hat{I}_{u,l}^j = \underbrace{\frac{P_g}{3V_{dc}}}_{DC} + \underbrace{\frac{\sqrt{2}\sqrt{3}K_t}{6U_g}\sqrt{P_g^2+Q_g^2}}_{AC}. \tag{6}$$

2) Voltage Limit Equation: Equation (7) does express the voltage limitation depending on the power flow (P_g and Q_g) either for upper and lower branches for a generic phase j.

$$\hat{U}_{u,l}^j = \underbrace{\frac{V_{dc}}{2} - R_a\frac{P_g}{3V_{dc}}}_{DC} + \underbrace{\sqrt{2}\sqrt{\left(K_t\frac{\gamma-\epsilon}{\sqrt{3}U_g}\right)^2 + \left(\frac{U_g}{K_t\sqrt{3}} + K_t\frac{\delta+\rho}{\sqrt{3}U_g}\right)^2}}_{AC}. \tag{7}$$

The diagram in Fig. 4(b) shows the typical P_g vs Q_g power capability domain for the AC/DC MMC converter. Hence, green area represents the feasible power domain for the converter.

From next section on, the article will focus on the objective of achieving the power capability domain for the specific M2DC-based AC/DC/DC multi-port converter.

III. Multi-Port Converter Description

Application-wise, the study refers to the schematic in Fig. 5: the AC transmission network is connected via the multi-port converter to two asymmetrical monopole DC lines referred to the

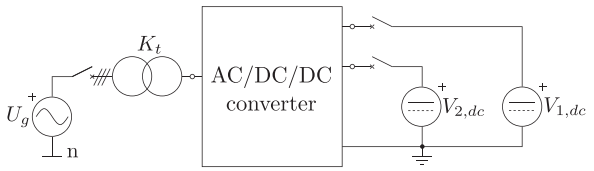

Fig. 5. One line diagram: Two asymmetrical monopole DC lines are interconnected to the AC transmission network via AC/DC/DC converter.

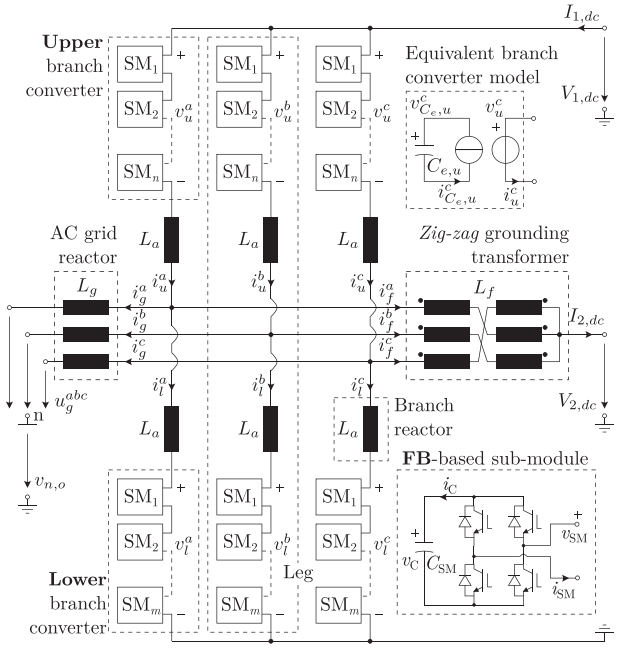

Fig. 6. M2DC-based AC/DC/DC converter (asymmetrical monopole).

same grounding pole. U_g indicates the AC voltage network, K_t represents the winding ratio between primary and secondary of the AC transformer. $V_{1,dc}$ indicates the asymmetrical monopole HVdc voltage while $V_{2,dc}$ indicates the asymmetrical monopole MVdc voltage. Furthermore, the DC voltage step ratio between DC networks is defined as: $K_v = \dfrac{V_{2,dc}}{V_{1,dc}}$.

The M2DC-based AC/DC/DC converter discussed in this work was introduced in [10] and, the circuit is depicted in Fig. 6. The AC transformer has been represented with an equivalent AC grid reactor. Each phase-leg converter is composed by two branches, upper and lower, that are composed by a series connection of Full-Bridge based sub-modules and a branch reactor L_a.

The connection to medium-low voltage DC is provided by a shunt zig-zag grounding transformer (ZGT), [25]. ZGT is designed to provide a very large positive-negative sequence impedance and a low zero sequence impedance. Hence, the positive-negative sequence current absorption from the filter is negligible. However, with a proper converter control, the ZGT windings have to deal with only DC components and, the typical zig-zag winding interconnection establishes the DC bias cancellation within the core preventing the operation in non-linear region.

In this section, the article presents the steady-state system of equations and its variables. In this analysis, the branch voltage sources are modelled as average-value model (AVM), for the AC domain only first order harmonic (fundamental) is applied.

A. Stationary Domain Analysis

In this section, the steady-state model is presented. The objective is to calculate the upper and lower branches variables in both domains, AC and DC. Regarding the AC domain, equations are described by phasor notation: each generic variable $\underline{z}$ will be expressed by a complex number in rectangular form as a composition of a real and imaginary part ($\underline{z} = a + ib = \mathrm{Re}(\underline{z}) + i\,\mathrm{Im}(\underline{z})$).

The three circuits depicted in Fig. 7 represent the three domains used to identify the steady state equations: AC positive-negative sequence in Fig. 7(a), AC zero sequence in Fig. 7(b) and DC domain in Fig. 7(c). The AC transformer and ZGT are represented by equivalent reactors. In addition, each reactor is comprehensive of an inductive and a resistive component, thus, the generic reactor impedance $\underline{Z_x}$ is expressed as: $\underline{Z_x} = R_x + i\omega L_x$).

Therefore, concerning the positive-negative sequence circuit and variables, due to the high positive-negative sequence impedance of the ZGT, the terminals connected to MVdc system are considered as equivalent open circuits (Fig. 7(a)).

For the proper operation, converter control ensures that any AC components circulate to HVdc or MVdc networks ($i_{1,ac}$, $i_{2,ac}$ in Fig. 7(b)), therefore, all AC zero sequence variables are kept equal to zero. Furthermore, the three-wire-based AC network offers no possibility for circulating homopolar components.

Finally, regarding DC domain circuit illustrated Fig. 7(c), to prevent any AC transformer saturation coming from current I_g, only homopolar DC current components are allowed to circulate in the system. Thus, current $I_{2,dc}$ is distributed homogeneously among the three phases (I_f) and, due to the three-wire based AC network, current I_g is zero.

1) Linear Equations: Referring to all the independent KVLs from the three circuits in Fig. 7. The system of equations, including the AC (positive-negative sequence) and DC domain, is summarized by (8).

$$\begin{cases} \underline{U}_g^{j+} + \underline{Z}_g^{j}(\underline{I}_u^{j+} - \underline{I}_l^{j+}) + \underline{Z}_a^{j}\underline{I}_u^{j+} + \underline{U}_u^{j+} = 0 \\ \underline{U}_g^{j+} + \underline{Z}_g^{j+}(\underline{I}_u^{j+} - \underline{I}_l^{j+}) - \underline{Z}_a^{j}\underline{I}_l^{j+} - \underline{U}_l^{j+} = 0 \\ \underline{U}_g^{j-} + \underline{Z}_g^{j}(\underline{I}_u^{j-} - \underline{I}_l^{j-}) + \underline{Z}_a^{j}\underline{I}_u^{j-} + \underline{U}_u^{j-} = 0 \\ \underline{U}_g^{j-} + \underline{Z}_g^{j-}(\underline{I}_u^{j-} - \underline{I}_l^{j-}) - \underline{Z}_a^{j}\underline{I}_l^{j-} - \underline{U}_l^{j-} = 0 \\ V_{1,dc} - V_{2,dc} - V_{u,dc}^{j} - R_a I_{u,dc}^{j} - R_f(I_{u,dc}^{j} - I_{l,dc}^{j}) = 0 \\ V_{2,dc} + R_f(I_{u,dc}^{j} - I_{l,dc}^{j}) - V_{l,dc}^{j} - R_a I_{l,dc}^{j} = 0 \end{cases} \tag{8}$$

where j indicates a generic phase a, b, c. The three-phase system, in total, counts 60 variables. From now on, since the study considers only symmetrical AC system (no negative sequence), the system of equation will be based on 36 variables.

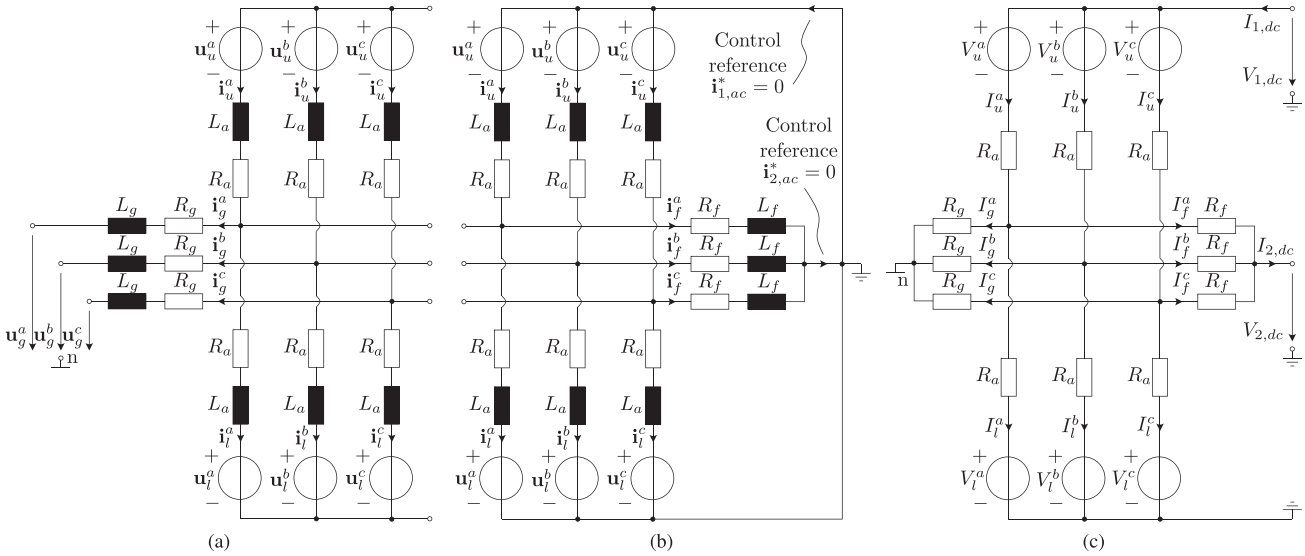

Fig. 7. AC and DC equivalent circuits: in (a) the positive-negative sequence circuit, in (b) the zero ac sequence and, in (c) the DC domain circuit.

2) Non-Linear Equations: The energy stored in a branch $E^j_{u,l}$ depends on the initial nominal energy stored $E^j_{0\,k}$ and it depends on the power across the branch p^j_k. To keep the operation of the converter energetically stable, it is fundamental to ensure that:

$$E^j_k(t) = E^j_{0\,k} + \overbrace{\int p^j_k(t)\mathrm{d}t}^{0} \tag{9}$$

where k refers to u, l upper or lower branch indicator. It means that, to solve the steady-state problem, the system of equation includes the following equation per each branch:

$$P^j_k = \mathrm{Re}(\underline{U}^j_k \underline{I}^{j*}_k)^+ + \mathrm{Re}(\underline{U}^j_k \underline{I}^{j*}_k)^- + P^j_{k,dc} = 0 \tag{10}$$

There are three more complex equations related to internal reactive power distribution among upper and lower branches:

$$\begin{aligned} Q^j_u - Q^j_l = {} & \mathrm{Im}(\underline{S}^j_u) - K_Q\,\mathrm{Im}(\underline{S}^j_l) = \mathrm{Im}(\underline{U}^j_u \underline{I}^{j*}_u) \\ & - K_Q\,\mathrm{Im}(\underline{U}^j_l \underline{I}^{j*}_l) \end{aligned} \tag{11}$$

Where the ratio $K_Q = \frac{Q^j_u}{Q^j_l}$ can be freely chosen (in the study, it is kept equal to one).

3) Port Power Equations: A further input of the system comes from the definition of the power at two ports; in this case, AC port and MVdc port are the selected ports in which the power is formulated:

$$\begin{cases} \underline{S}^j_g = P^j_g + iQ^j_g = \underline{U}^j_g \left(\underline{I}^j_u - \underline{I}^j_l\right)^* \\ P_2 = 3K_v V_{1,dc}(I^j_{u,dc} - I^j_{l,dc}) \end{cases} \tag{12}$$

4) Results: Table I summarizes all the variables and equations to solve the steady-state problem for balance operation of the multi-port converter topology. In Fig. 8(a) is presented the process to get time-domain based results and Fig. 8(b) shows

TABLE I
STEADY-STATE VARIABLES AND EQUATIONS

	AC	DC	Tot.
Variables	$\underline{I}^j_u, \underline{I}^j_l$ (6-complex) $\underline{U}^j_u, \underline{U}^j_u$ (6-complex)	I^j_u, I^j_l (6-real) $V^j_u V^j_l$ (6-real)	36
Linear eq.	Upper (3-complex) Lower (3-complex)	Upper (3-real) Lower (3-real)	18
Non linear eq.	Branches power-energy constraints (6-real)		6
Non linear eq.	Branches reactive distribution (3-im)		3
Port power eq.	$\underline{S}^j_g$ (3-complex)	P^j_2 (3-real)	9

the results for a given system data and for an established power flow scenario.

From the results, it is possible to appreciate asymmetries in current voltage variables between upper and lower branches. The asymmetric mechanism between the upper and lower branches is described below:

- Whenever a DC power flow occurs, converter branches experience a power unbalance between upper and lower side. The percentage of unbalance depends on the DC voltage step ratio between DC networks and the power demanded at ports:

$$\begin{cases} P_{u,dc} = V_{u,dc} I_{u,dc} = (V_{1,dc} - V_{2,dc})\,\dfrac{P_1}{3V_{1,dc}} \\ P_{l,dc} = V_{l,dc} I_{l,dc} = V_{2,dc}\left(\dfrac{P_1}{3V_{1,dc}} - \dfrac{P_2}{3V_{2,dc}}\right). \end{cases} \tag{13}$$

  Being, in general, $P_{u,dc} - P_{l,dc} \neq 0$, asymmetric DC power distribution among branches occurs.
- However, the AC power across the upper and lower branch must be corrected according to the following requirement:

$$\begin{cases} P_{u,dc} - P_{u,ac} = 0 \\ P_{l,dc} - P_{l,ac} = 0. \end{cases} \tag{14}$$

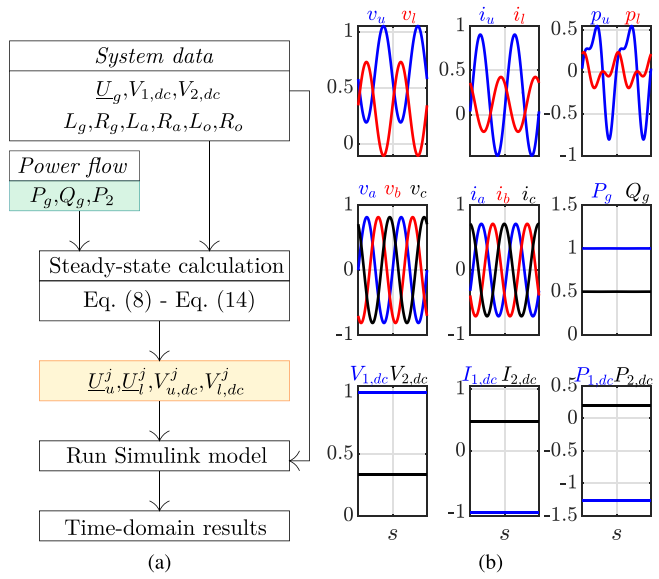

Fig. 8. M2DC-based AC/DC/DC steady-state model calculation: process to extrapolate time domain results in (a), and, an example on the results for a given system data and power flow scenario in (b).

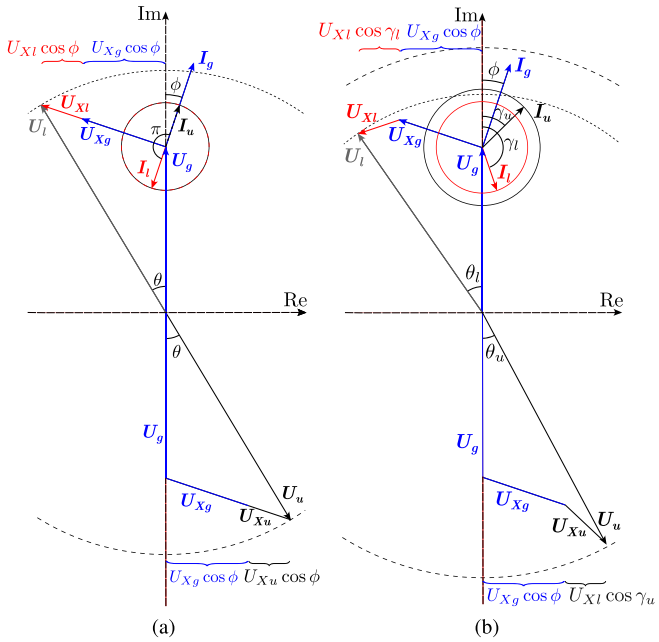

Fig. 9. Representative phasor diagram comparison: AC variables for MMC AC/DC converter (a) and AC variables for M2DC-based multi-port converter (b).

- It means that converter will establish asymmetric AC power distribution among the upper and lower branches to ensure zero energy deviation.

Fig. 9 is intended to be a representative phasor diagram highlighting the comparison between an AC/DC MMC Fig. 9(a), and the M2DC-based AC/DC/DC converter Fig. 9(b) on the branch asymmetries. The AC/DC MMC maintains the voltage and current symmetry because of symmetrical DC power flow among the branches. The M2DC-based AC/DC/DC converter, dealing with asymmetric DC power flow, it depicts asymmetries either in phase and magnitudes for branch current and voltage variables. Such asymmetries cause a non-intuitive understanding about the converter limitations. In this regard, the study proposes a method to calculate the overall capability domain of the converter considering branches asymmetries. Afterwards, the steady-state model will be apply to verify the branch variables behaviour for selected power flow scenarios indicated by the converter power capability domain.

IV. Power Capability Domain Analysis Criteria

The 3D power capability domain is formulated by introducing the established variables that limit the converter operation. In this work, the chosen variables are: maximum current $I_{\max}^j$ and maximum voltage $U_{\max}^j$ of each branch. However, due to asymmetries, it is necessary to calculate the limitations for upper and lower branches separately. Thus, four limit functions are expected to be formulated: $I_u^{\max}$, $I_l^{\max}$, $U_u^{\max}$ and $U_l^{\max}$.

Each of those limits is expressed as function of the power delivered to each port (active and reactive components). Therefore, assuming losses negligible, $P_{1,dc} = P_g + P_{2,dc}$. Then the three independent power components considered for the power capability domain are: Q_g, P_g and $P_{2,dc}$. Unbalanced conditions of the AC network is not considered in the study, hence the expression can refers to a generic phase j (a, b, c).

Once the limit functions are formulated, by mathematical manipulation, it is possible to achieve the expression of reactive powers $Q_g^{j,\max}$ as (15).

$$\begin{cases} Q^j_{g,I_u^{\max}} = f_1(P_g, P_{2,dc}, I_u^{\max}) \\ Q^j_{g,I_l^{\max}} = f_2(P_g, P_{2,dc}, I_l^{\max}) \\ Q^j_{g,U_u^{\max}} = f_3(P_g, P_{2,dc}, U_u^{\max}) \\ Q^j_{g,U_l^{\max}} = f_4(P_g, P_{2,dc}, U_l^{\max}). \end{cases} \tag{15}$$

A. Current Limit Equations

Equations (16) and (17) describe the peak current value for upper and lower branch respectively. DC and AC current components are included.

B. Voltage Limit Equations

Equations (19) and (20) describe the peak voltage value for upper and lower branch respectively. DC and AC current components are included.

According to the phasor diagram in Fig. 9, the magnitude of the voltage applied by the branch will be evaluated as: $\hat{U}_{u,l}^j = \sqrt{U_{u,l-Re}^2 + U_{u,l-Im}^2}$.

C. Zero Energy Branch Deviation

Referring to (14), current and voltage limit functions are evaluated assuming the energy equilibrium within the branches.

D. Assumptions for the Analysis

1) Sub-Module and Branches: It is assumed that branches are equipped by full-bridge based SM technology. The full blocking capability is guaranteed in case of fault contingency.

2) Reactive Power Distribution: Even though it is possible to distribute the reactive current component within two branches, Equation (11), the study considers symmetric reactive current distribution between upper and lower branches ($K_Q = 1$).

3) Maximum Current-Voltage Ratings: In this work, the same SM current rating is chosen either for upper and lower branch, so that $\hat{I}_u^j = \hat{I}_l^j = \hat{I}_{SM}$. Regarding the maximum branch voltage applied, just as an example, it has been selected a 6% over sizing on the nominal voltage value of the branch, then: $\hat{U}_u^j = 1.06\hat{U}_{u,nom}^j$ and $\hat{U}_l^j = 1.06\hat{U}_{l,nom}^j$. (16) and (17) shown at the bottom of this page, where:

$$U_r^u = \frac{R_a P_1}{3V_{1,dc}} + \frac{R_f P_2}{3V_{2,dc}}, \quad U_r^l = \frac{R_a P_1}{3V_{1,dc}} + \frac{(R_f + R_a) P_2}{3V_{2,dc}} \tag{18}$$

$$\hat{U}_u^j = \underbrace{V_{1,dc}\left(1 - K_v\right) - R_a\left(\frac{P_1}{3V_{1,dc}}\right) - R_f\left(\frac{P_2}{3K_v V_{1,dc}}\right)}_{DC} + \underbrace{\sqrt{2}\sqrt{\left(\frac{K_t}{\sqrt{3}U_g}\phi\right)^2 + \left(\frac{U_g}{K_t\sqrt{3}} + \frac{K_t}{\sqrt{3}U_g}\tau\right)^2}}_{AC} \tag{19}$$

$$\hat{U}_l^j = \underbrace{K_v V_{1,dc} - (R_a + R_f)\left(\frac{P_2}{3K_v V_{1,dc}}\right) - R_a\left(\frac{P_1}{3V_{1,dc}}\right)}_{DC} + \underbrace{\sqrt{2}\sqrt{\left(\frac{K_t}{\sqrt{3}U_g}\varphi\right)^2 + \left(\frac{U_g}{K_t\sqrt{3}} + \frac{K_t}{\sqrt{3}U_g}\sigma\right)^2}}_{AC} \tag{20}$$

where:

$$\begin{cases} \phi = X_g P_g - R_{eq} Q_g + X_a(1 - K_v)P_1 \\ \tau = R_g P_g + X_{eq} Q_g + R_a(1 - K_v)P_1 \\ \varphi = (X_g + X_a)P_g - R_{eq} Q_g - X_a(1 - K_v)P_1 \\ \sigma = (R_g + R_a)P_g + X_{eq} Q_g - R_a(1 - K_v)P_1 \end{cases} \tag{21}$$

with: $X_{eq} = X_g + X_a/2$ and $R_{eq} = R_g + R_a/2$.

E. Overall Power Capability Domain Obtention

After calculating the three-dimension limit functions for a phase j (16)–(20), the overall power capability domain is achieved by collecting all the common feasible points of operation described by the four separated power capabilities.

According to this, Fig. 10 shows the results for the four power capability domains, Fig. 10(a)–(d) depending on upper branch current, lower branch current, upper branch voltage and lower branch voltage respectively. While, Fig. 10(e) represents the region of all the feasible power flow scenarios the converter can withstand (for a chosen set of connected system data and parameters) discarding all regions where at least one of four restrictions is not satisfied.

In the next section, a detailed explanation of such a domain will be offered considering a specific use case scenario. Therefore, each generic point of operation $Q_g^{gen}(P_g^{gen}, P_2^{gen})$ has to comply with the established limits as depicted in (22).

$$\begin{cases} Q_g^{gen}(P_g^{gen}, P_2^{gen}) \le Q_{g,I_u^{\max}}^j \\ Q_g^{gen}(P_g^{gen}, P_2^{gen}) \le Q_{g,I_l^{\max}}^j \\ Q_g^{gen}(P_g^{gen}, P_2^{gen}) \le Q_{g,U_u^{\max}}^j \\ Q_g^{gen}(P_g^{gen}, P_2^{gen}) \le Q_{g,U_l^{\max}}^j \end{cases} \tag{22}$$

V. Power Capability Validation on a Use Case

Referring to the system depicted in Fig. 5, use case data in Table II are employed to calculate the power capability domain by applying (16)–(20).

The maximum current rating of the branch is: $I_{\max}^j = 1.78$ kA, and, the maximum voltage applied by each branch is: $U_{u,\max}^j$ or $U_{u,\max,BFC}^j$ for upper branches and $U_{l,\max}^j$. Where BFC indicates the full blocking fault capability case for the converter:

$$\begin{cases} U_{u,\max}^j = 1.06\left[V_{1,dc}\left(1 - K_v\right) + \sqrt{2}\frac{U_g}{\sqrt{3}}\right] \\ U_{l,\max}^j = 1.06\left(K_v V_{1,dc} + \sqrt{2}\frac{U_g}{\sqrt{3}}\right) \\ U_{u,\max,BFC}^j = 1.06\left(V_{1,dc} + \sqrt{2}\frac{U_g}{\sqrt{3}}\right). \end{cases} \tag{23}$$

With considering the SM rated voltage U_{SM}, the total amount of SMs installed by the converter topology is calculated as follow:

$$N_{SM,tot} = 3\left[\text{ceil}\left(\frac{U_{u,\max}^j}{U_{SM}}\right) + \text{ceil}\left(\frac{U_{l,\max}^j}{U_{SM}}\right)\right]. \tag{24}$$

$$\hat{I}_u^j = \underbrace{\frac{P_1}{3V_{1,dc}}}_{DC} + \underbrace{\frac{\sqrt{2}\sqrt{3}K_t}{U_g}\sqrt{\left[\left(V_{1,dc} - V_{2,dc} - U_r^u\right)\frac{P_1}{3V_{1,dc}}\right]^2 + \left(\frac{K_Q Q_g}{3(K_Q + 1)}\right)^2}}_{AC} \tag{16}$$

$$\hat{I}_l^j = \underbrace{\frac{P_1}{3V_{1,dc}} - \frac{P_2}{3V_{2,dc}}}_{DC} + \underbrace{\frac{\sqrt{2}\sqrt{3}K_t}{U_g}\sqrt{\left[\left(V_{2,dc} - U_r^l\right)\left(\frac{P_1}{3V_{1,dc}} - \frac{P_2}{3V_{2,dc}}\right)\right]^2 + \left(\frac{Q_g}{3(K_Q + 1)}\right)^2}}_{AC} \tag{17}$$

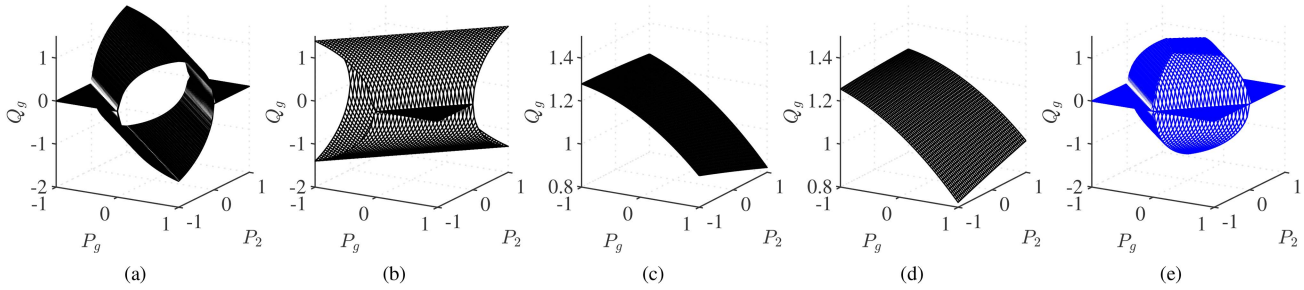

Fig. 10. 3D power capability result: upper branch current limit (a), lower branch current limit in (b), upper branch voltage limit in (c) and lower branch voltage limit in (d). (e) represents the overall feasible power capability domain (volume).

TABLE II
SYSTEM PARAMETERS

Parameter	Description	Unit	value
U_g	Phase-to-phase AC voltage	kV	160
f_g	AC system frequency	Hz	50
K_t	Transformer step ratio	-	1
S_b	Base power	MVA	500
Z_b	Base impedance	Ω	51
X_g	Per unit grid reactance	p.u.	0.1
R_g	Per unit grid resistance	p.u.	0.001
$V_{1,dc}$	High Voltage DC	kV	320
K_v	DC step ratio	-	0.5
R_f^m	Per unit filter mag. resistance	p.u.	100
X_f^m	Per unit filter mag. reactance	p.u.	100
R_f	Per unit filter resistance	p.u.	1
X_f	Per unit filter reactance	p.u.	1
X_a	Per unit branch reactance	p.u.	0.05
R_a	Per unit branch resistance	p.u.	0.01
U_{SM}	SM rated voltage	kV	2
$\hat{I}_{u,l}$	Maximum current	kA	1.78
$\hat{U}_u$	Upper voltage capability	kV	310-480*
$\hat{U}_l$	Lower voltage capability	kV	310
N_{SM}	Total number of SMs	-	925-1182*

*Full blocking capability.

Where the ceil function rounds up the values to the nearest integer.

The validation approach employs the steady-state method in Fig. 8(a) to verify that a specific power flow scenario on the boundary of the power capability domain reached the expected current and voltage limitations. The principal objective of the validation is to ensure that the branches behaviour are properly depicted by power capability domain calculation. However, it is worth to remind that, this validation approach is slightly affected by the assumption on the losses for the power capability domain calculation. In fact, while power capability domain is calculated assuming power converter losses negligible ($P_{1,dc} = P_g + P_{2,dc}$), the steady-state model provides results comprehensive of power losses. Therefore, from now on, the slight discrepancy between power capability results and steady-state time domain results lies in the power loss assumptions for calculating the power capability domain.

A. Normal Operation Scenarios

The 3D power capability domain result for the normal operation scenario is depicted in Fig. 11(a). Aiming to demonstrate the correctness of the calculated feasible power capability domain,

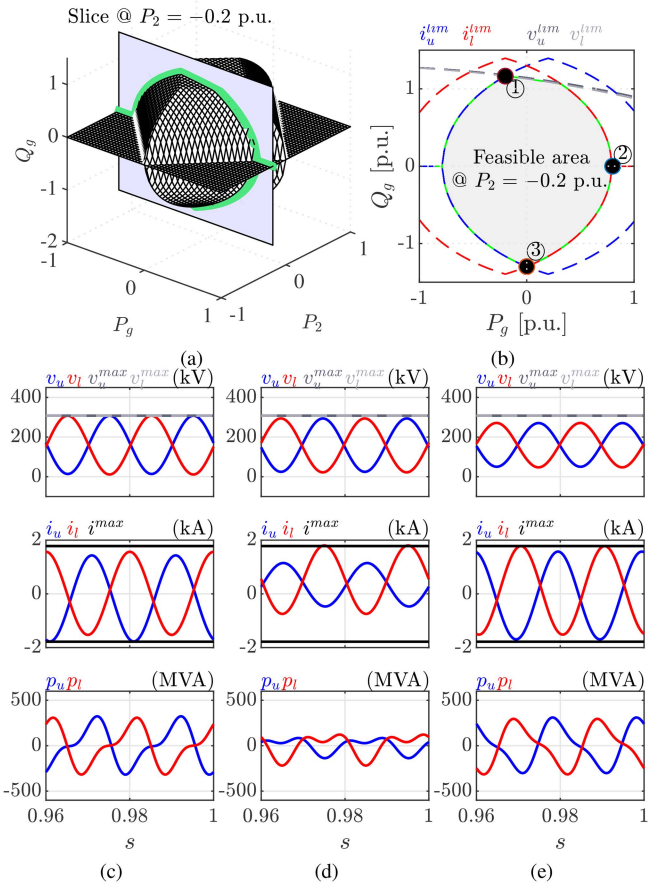

Fig. 11. 3D power capability domain validation: In (a) the feasible power domain is cut on P_2 axis at $P_2 = -0.2$ p.u., in (b) the 2D slice is depicted and (c)–(e) represent the validation by the steady-state model for the operating points located at the boundary of the feasible power capability: 1, 2 and 3.

three power flows scenarios, 1-2-3, placed on the boundary of the power capability volume have been selected, Fig. 11(b). Each selected point is defined in the 3D diagram by the power on the three axes: P_g, Q_g and P_2 (slice). The grey area, surrounded by green line represents the feasible power capability surface.

Below a description on the reached limits per each of the selected power flow scenario:

- *Power flow scenario 1:* it brings the converter to operate at the limit of voltage capability either for upper and lower branches. In terms of current capability, while upper branch

experiences the maximum established current, the lower branch maintains some margin. Running the steady-state simulation model at the correspondent power flow scenario, as proposed in Figs. 8(a), 11(c) confirms the reached limits.

- *Power flow scenario 2:* it brings the converter to operate at the limit of lower branch current capability (red dashed line). In terms of voltage capability, both upper and lower branches maintain some margin. Running the steady-state simulation model at the correspondent power flow scenario, Fig. 11(d) confirms the reached limits.
- *Power flow scenario 3:* it brings upper and lower branches to experience the maximum current rating. In terms of voltage capability, both branches have margin. Running the steady-state simulation model at the correspondent power flow scenario, Fig. 11(e) confirms the reached limits.

1) DC Voltage Step Ratio (K_v) Influence: The DC voltage step ratio between the DC terminals is one of the main parameters affecting the asymmetries between upper and lower branches. The section explores how the power capability domain will shape under different K_v values. Fig. 12 shows the results for three cases of step ratios, and, per each of them, a 2D slice is taken to highlight the limits and validate branches behaviour by steady-state solutions.

The case of $K_v = 0.5$ is illustrated in the prior section. Comparing the DC voltage step ratio cases, $K_v = 0.75$ and $K_v = 0.2$, it can be noted that branch variables invert their behaviour: for $K_v > 0.5$, power capability is mostly affected by upper voltage branch capability and, lower branches show less current capabilities compared with upper branches. For $K_v < 0.5$, power capability is mostly affected by lower branches voltage capability and, upper branches show a less current capabilities compared with lower branches.

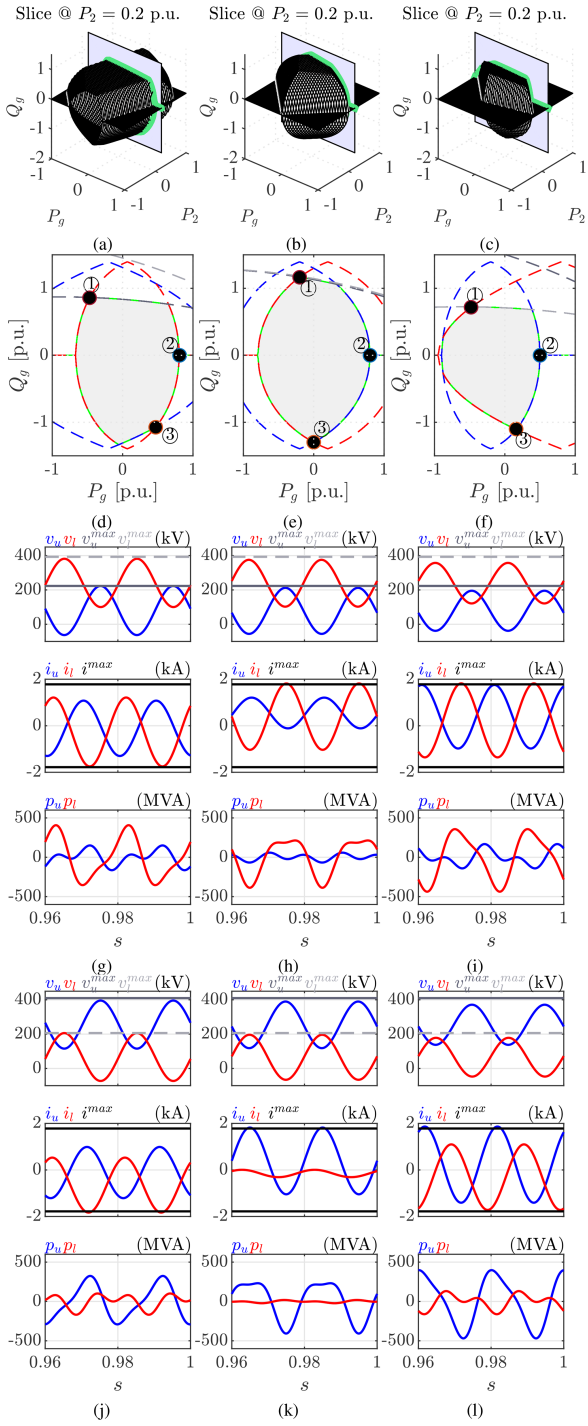

Fig. 12. K_v influence on power capability domain: $K_v = 0.75$ (a)–(d), $K_v = 0.5$ (b)–(e) and $K_v = 0.2$ (c)–(f). (g), (h), and (i) represent the steady-state variables at point 1,2 and 3 respectively of the graph depicted in (d). (j), (k), and (l) represent the steady-state variables at point 1,2 and 3 respectively of the graph depicted in (f).

B. Contingencies Operation Scenarios

As mentioned in the introduction, multi-port converter should be able to operate in contingency scenarios (e.g., fault or port disconnection). The section explores how the branch current and voltages limits need to be expressed and, how the overall converter power capability domain changes based on the specific contingency.

The contingencies scenarios representations are depicted in Fig. 13. Unless the contingency is not related to AC port, the studies have been conducted considering no current injection to the faulted port. Thus, in case of DC side contingencies, the power capability domain is placed on a 2D diagram ($P_g - Q_g$). From Fig. 13, it can be noted that the active and reactive power components managed by each branch depend on the contingency scenario.

The study on contingencies has been conducted considering a DC voltage step ratio, K_v, equal to 0.25.

1) High Voltage DC Fault (AC/DC$_2$ Operation): The HVdc fault scenario depicted in Fig. 13(a) refers to an ideal pole to ground short circuit. During such a contingency, the converter will actively interact between the healthy two ports (AC and MVdc). Upper branches deal with reactive power only. The total active power is processed by lower branches.

In addition, upper branches apply a negative DC voltage (according to the MVdc network voltage) to prevent fault energization.

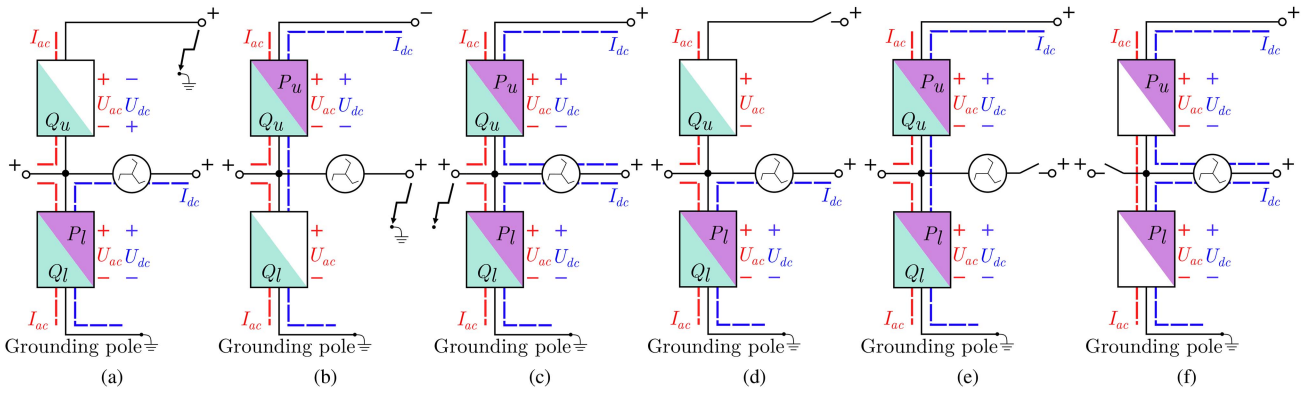

Fig. 13. Contingencies scenarios: HVdc fault (a), MVdc fault (b), AC fault (c), HVdc port disconnection (d), MVdc port disconnection (e), and AC port disconnection (f).

The upper-lower current and voltage limits expressions in (16)–(21) must be evaluated substituting $P_1 = 0$ and $P_2 = P_g$.

The power capability domain results are depicted in Fig. 14(a). It is clear that upper branch current limitation depends only on the maximum reactive power capability. The lower branch current capability is affected by active and reactive power components. Therefore, upper branches are not suffering voltage limitation due to the lower DC voltage application to block the fault. On the other side, lower branch voltage capability still is affected by active and reactive power capability.

2) High Voltage DC Disconnection (AC/DC$_2$ Operation): The equations related to HVdc pole disconnection, Fig. 13(d), are close to the previous fault case scenario expressions.

Lower branch current and voltage capabilities do not change compared to HVdc fault case scenario.

Still, upper branches do not process any active power component. However, being positive HVdc pole disconnected, upper branches could achieve higher AC voltage capability.

Due to the close similarities to the HVdc fault scenario, the power capability domain representing HVdc disconnection scenario is depicted in Fig. 14(a).

3) Medium Voltage DC Fault (AC/DC$_1$ Operation): The MVdc fault scenario depicted in Fig. 13(b) refers to an ideal pole to ground short circuit. It assumed that upper branches are designed to sustain the full HVdc voltage.

The converter will actively interact between the healthy two ports (AC and HVdc). Lower branches deal with reactive power only. The total active power is processed by upper branches.

Even though, lower branches apply a null DC voltage (according to the MVdc network voltage) to prevent fault energization, lower branch DC current is not zero.

The upper-lower current and voltage limits in (16)–(21) must be evaluated substituting $P_2 = 0$, $P_1 = P_g$ and $V_{dc,2} = 0$. Therefore, the overall power capability in depicted in Fig. 14(b). Lower branch current capability depends either from reactive and active transmitted powers.

4) Medium Voltage DC Disconnection (AC/DC$_1$ Operation): This contingency, Fig. 13(e), in terms of operation, makes the lower branches able to process active power; in fact since the MVdc port is disconnected, the lower branch are free to apply

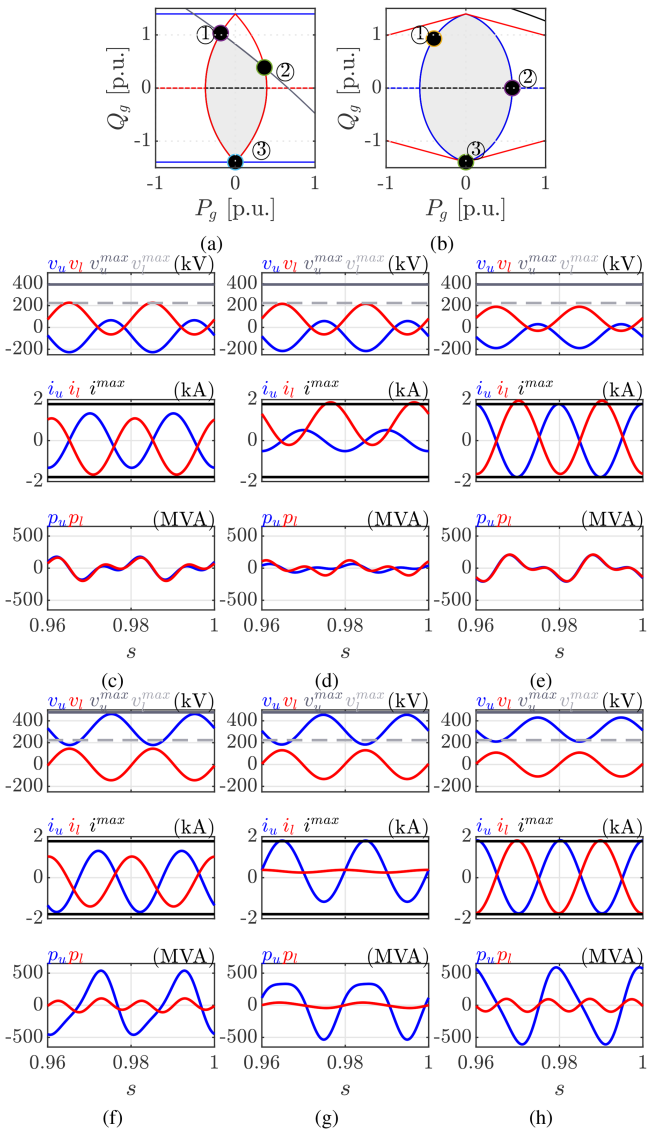

Fig. 14. HVdc fault operation (or HVdc disconnection) in (a) and 1-2-3 points in (c)–(e) respectively. MVdc fault operation (b) and 1-2-3 points in (f)–(h) respectively.

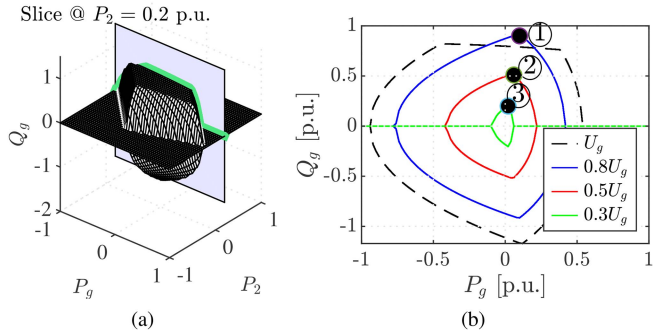

Fig. 15. Power capability modifications under different AC symmetrical voltage sag scenarios: (a) U_g at 1 p.u. nominal condition, (b) represents the 0.8 p.u., 0.5 p.u. and 0.3 p.u. voltage sags taking slices at $P_2 = 0.2$ p.u.

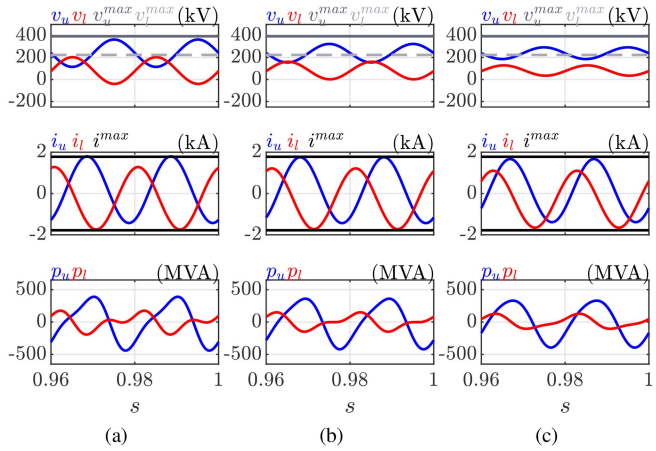

Fig. 16. Steady-state variables representation at points 1 (a), 2 (b), and 3 (c) depicted in Fig. 15.

a DC voltage component. The upper-lower current and voltage limits in (16)-(21) must be evaluated substituting $P_2 = 0$ and $P_1 = P_g$.

5) AC Symmetric Fault (AC/DC/DC Operation): Referring to the representation in Fig. 13(c) the section aims to illustrate how the power capability changes based on different level of symmetrical voltage sags at AC network. Differently from DC faults, during such a contingency the converter is assumed to perform between the three systems. Active and reactive power components to the AC faulted port are considered to be enabled.

Describing this contingency scenario, Equation (16)-(21) do modify based on the voltage sag coefficient K_{sag}; $U_g = K_{sag}U_g^{nom}$, where K_{sag} refers to the percentage of voltage drop.

Nevertheless, while branch voltage capability increases with the AC voltage sag severity, the branch current capability decreases. In overall, Figs. 15 and 16 clearly shows how the increasing of the voltage sag severity strongly impacts on the feasible domain due to branch current limits.

6) Zero AC Network Voltage (DC/DC/i_g Operation): Based on AC symmetric faults, the paragraph explores the worst case scenario: AC voltage network equal to zero. Then, this scenario leads to any active or reactive power being transferred to the AC network ($P_g = Q_g = 0$), however, the converter can only inject current, i_g, to the AC network.

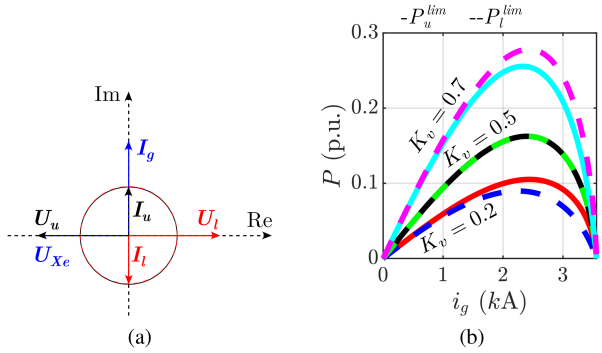

Fig. 17. Zero AC voltage scenario: phasor representation in (a) and branch power capability vs injected current i_g depending on the DC voltage step ratio K_v in (b).

Therefore, the DC/DC operation is negatively affected by this contingency: the power transfer among DC ports ($P_{DC/DC}$) strictly depends on the amount of current delivered to AC network (I_g). The analysis considers impedances to be predominantly inductive.

As illustrated in the steady-state operation of the converter, whenever the converter experiences a DC power flow, the AC power component must be enabled to establish energetic stability among converter branches.

However, since AC network voltage is zero, whenever the converter applies an AC voltage to the AC terminals, it produces a current injection to AC grid.

The voltage applied by the branches is approximatively equal to the voltage drop on the equivalent inductance $U_{u,l}^{AC} = \omega L_{eq} I_g$. Increasing the AC voltage, the AC grid current injection also increases. The converter may increase the DC/DC power transfer while decrease current capability. Due to this cross connection between the two effects, the 2D ($P_{dc} - i_g$) power capability increases until the maximum branches current capability is reached (comprehensive of both AC and DC components).

Equations (25)–(28) depict the branch current and voltage limit functions and Fig. 17(a) shows a representative current-voltage phasor diagram.

$$\hat{I}_u^j = \underbrace{\frac{P}{3V_{1,dc}}}_{DC} + \underbrace{\sqrt{\left(\frac{P(1-K_v)}{3X_{eq}i_g}\right)^2 + \left(\frac{i_g}{2}\right)^2}}_{AC} \tag{25}$$

$$\hat{I}_l^j = \underbrace{\frac{P(K_v-1)}{3K_vV_{1,dc}}}_{DC} + \underbrace{\sqrt{\left(\frac{P(K_v-1)}{3X_{eq}i_g}\right)^2 + \left(\frac{i_g}{2}\right)^2}}_{AC} \tag{26}$$

$$\hat{U}_u^j = \underbrace{V_{1,dc}(1-K_v)}_{DC} + \underbrace{\omega L_{eq} i_g}_{AC} \tag{27}$$

$$\hat{U}_l^j = \underbrace{K_v V_{1,dc}}_{DC} + \underbrace{\omega L_{eq} i_g}_{AC} \tag{28}$$

Fig. 17(b) shows the resulting $P_{dc} - i_g$ capability curve considering different K_v ratios: the lower the step ratio the lower power transfer converter capability. If K_v decreases, the

branches requires more AC power to compensate the power unbalancing. Vice-versa, when the step ratio increases, there is more margin for DC power transfer since the required AC power is reduced.

7) AC Disconnection (DC_1/DC_2 Operation): The AC disconnection contingency scenario brings the converter to operate as the DC/DC above mentioned in the introduction. The AC voltage network does not influence the power capability. The converter establish as AC voltage in order to minimize the circulating AC current without a significant power de-rating. Under this specific contingency, the current-voltage limits are depicted in (2)–(5) and the power capability representation can refer to the 1D diagram in Fig. 3(b).

VI. Conclusion

This work proposes a methodology for calculating the overall power capability domain for the specific M2DC-based AC/DC/DC asymmetrical monopole converter. In particular, the study aims to depict all the feasible power flow scenarios the converter can perform without exceeding current and voltage ratings.

To achieve the objective, the study primarily defines the power domain based on the number of independent powers the converter is able to manage at the terminals, and consequently, it evaluates the power capability based on the established voltage and current limitations. To properly capture the feasible power domain, the intrinsic asymmetric behaviour between converter branches, as well as the branch energy balancing, are considered in the calculations.

Furthermore, to explore multi-port AC/DC/DC converter flexibilities, studies on power capability domain changes due to contingencies scenarios are presented. In specific, symmetric faults at ports and port disconnections are treated in the article.

Finally, to aid the understanding about the power flow scenarios at the boundaries of such a power capability domain, and to validate such a feasible domain calculation, steady-state model simulations are performed at the correspondent maximum feasible power flow scenarios.

Acknowledgment

The authors would like to thank Xavier Bourgeat and Olivier Despouys for their support.

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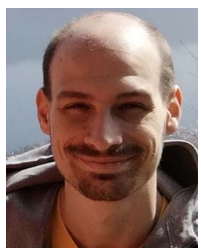

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