Interleaving Clusters of Submodules to Enhance Scalability of Modular Multilevel Converters for High-Voltage Applications

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***Abstract*—This article presents a practical architecture for fully exploiting the scalability of modular multilevel converters (MMC) by clustering the submodules (SMs) and interleaving these clusters. The proposed architecture enables scalability and flexibility for various high-voltage applications by dividing the computing tasks of an arm controller among each cluster control iteration, interleaving the output voltages of each cluster to maintain the desired voltage quality without structural changes, and balancing the cluster energy to ensure stable control performance. One noteworthy aspect of the proposed architecture is its implementation of distributed cluster control using a single controller, which eliminates the need for inter-controller synchronization and utilizes hardware resources cost-effectively. The article provides design guidelines for clustering the SMs through theoretical analysis and numerical examples. The validity and performance of the proposed interleaving scheme for the clusters of SMs are demonstrated through hardware-in-the-loop simulation (HILS).**

***Index Terms*—Flexibility, high-voltage dc (HVDC), modular multilevel converter (MMC), nearest level control (NLC), scalability.**

I. Introduction

MODULAR multilevel converters (MMC) have been well-accepted and widely deployed solution for medium and high voltage dc (HVDC) applications [1]. The dynamics, modeling, and control of MMC have been revealed by the efforts of academic and industrial pioneers [2], [3], [4], [5], [6], [7], [8]. Modularity enabling scalability, high-efficiency, and control performance are often featured as salient technical advantages over two- or three-level voltage-sourced converter (VSC) solutions [9]. However, achieving MMC scalability extended to high voltage applications, while not compromising the efficiency and control performance objectives, is never a straightforward task in practice. Computational complexity of controls and communication becomes a serious technical constraint and remains challenging in high-voltage applications [10], [11]. So does the computation burden to execute modulation and submodule (SM) capacitor voltage balancing tasks in such a way that all time-critical tasks meet their specified deadlines as illustrated in Fig. 1 where the red dotted arrow indicates that the growing execution time for balancing even beyond the chosen hardware constraint as the target voltage (i.e., number of SMs) increases. The modulation and SM balancing should perform at a sufficiently high sampling frequency to ensure the desired voltage quality [11]. This becomes challenging for high-voltage (or high-level)

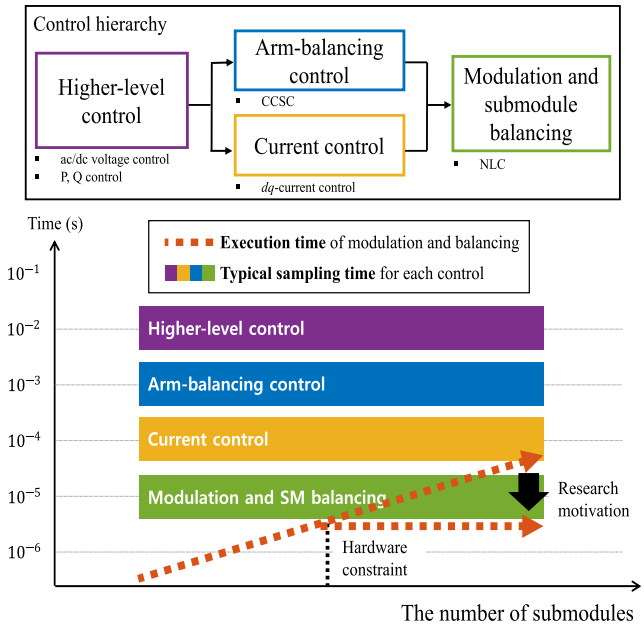

Fig. 1. Typical sampling times for MMC control functions and increase in execution time of the modulation and SM balancing with the number of SMs.

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operations given the practical constraints in designing the controllers cost-effectively, which is the research motivation of this article.

Various modulation methods have been developed for multilevel converters such as pulse width modulation (PWM), space vector modulation (SVM), selective harmonic elimination (SHE), nearest vector control (NVC), and nearest level control (NLC) [1], [12]. Those carrier-based PWM methods [12], [13], [14], [15] have been employed especially for low and medium voltage applications because of the complexity and heavy computational burden for high voltage applications with a large number of SMs. The NLC method [16], [17] has been thus prevailing for the high-voltage or high-level MMC applications owing to its simplicity and high efficiency. However, there is still a critical design consideration in practice to implement NLC for high-level HVDC due to the computation complexity of modulation process, i.e., SM capacitor voltage balancing, data communication, and data reading/writing.

The industry has investigated decentralized control architectures to advance scalability and streamline the system design efforts as addressed in [10], [18], [19], [20], [21], [22], [23], [24]. Among these efforts, reduced communication burden through distributed control schemes was highlighted in [18]. A daisy-chained distributed control system was presented in [19]. An example of an industry implementation of distributed control scheme was discussed in [20]. However, these decentralized control schemes or distributed SM controllers require sophisticated synchronization methods to avoid harmonics, voltage waveform distortions, and control conflicts [21], [22]. Decentralized control structures using groups of SMs with NLC were presented in [10], [23], [24] for large-scale MMC-HVDC systems. In a prototype of decentralized control scheme [23], control tasks were assigned in the central and valve-group control units. A decentralized control scheme for the SM capacitor voltage balancing and switching was proposed in [24]. However, these decentralized structures did not investigate the synchronization between groups in [23], [24]. It is noteworthy that synchronization between groups of SMs can significantly improve the voltage quality although it is not as essential as in the case of PS-PWM requiring the synchronization of the hundreds of phase-shifted carriers. It is also worth noting a scale-up method by configuring sets of SMs [10] similar to the cluster of the proposed architecture in this article. However, this method generates a fixed number of stepped output voltage waveforms by identical sampling timing between group controllers without specifying the desired number of SMs, which should vary with the voltage levels and applications. It did not fully exploit the sets to further improve the voltage quality as this article does.

Motivated by the aforementioned technical challenges in designing the modulation and SM energy balancing schemes for high voltage MMC, and persistent needs to improve scalability, this research presents clustering and interleaving schemes. The concept of the standard cluster set with a fixed number of SMs and time-interleaving voltage output was initially introduced in the authors' earlier works [25], [26], [27]. Building upon this groundwork, the advanced clustering architecture divides these modulation loads to each cluster control iteration; and, cluster voltage output is interleaved by faster sampling time. The clusters, a group of SMs, are designed to be identical, running with the same sorting and balancing logic for modularity. Time-interleaving these clusters achieves even higher voltage quality than the conventional distributed control schemes provide. A synchronization method is not required because there is only one cluster controller, executing the same control for each cluster iteratively, as shown in Fig. 2. Therefore, the proposed scheme certainly helps enhance the scalability of the MMC and ensures the desired control performance with hardware constraints for various voltage levels while fully exploiting the advantages of NLC in a cost-effective manner. There should be voltage unbalance between clusters caused by the remainders when we divide the reference signal with the number of clusters, as observed in [28]. This article thus develops a practical algorithm for balancing the cluster voltages as well.

The outline of this article is as follows. The MMC structure, control methods, NLC method, and analysis of MMC harmonics are described in Section II. Section III presents the proposed clustering and interleaving schemes and cluster voltage balancing control. The proposed scheme is validated for a test system built for Yangju MMC-HVDC project in Korea through Hardware-in-the-loop simulation (HILS) in Section IV. Finally, conclusions are drawn in Section V.

II. Principle of MMC Operation

A. Structure of MMC

The three-phase MMC consists of six arms with N SMs and an arm reactor as shown in Fig. 3: Note that the illustrated MMC is based on the proposed clusters, incorporating a carefully determined number of SMs as depicted in the boxes of Fig. 3 and detailed in Section III. The upper and lower arms comprise a single leg, a phase unit. The SM is a half-bridge circuit with two switches: S_1 and S_2. Each SM includes a capacitor for stiff output voltage. The SM output voltage is determined by the switching states of the SM. When S_1 is turned on and S_2 is turned off, the SM reaches an inserted state where the SM capacitor is connected to the arm circuit and charges or discharges the SM capacitor depending on the arm current direction. On the other hand, the SM reaches a bypassed state when S_1 is turned off and S_2 is turned on and the voltage of the SM capacitor remains constant. A cluster, i.e., a group of SMs within the arm consists of a fixed number of SMs (N/N_{cs}), and builds another modularity layer. v_{cs}^{i}, called cluster voltage, denotes the sum of capacitor voltage in a cluster.

Practical MMC-HVDC systems are designed to have redundant SMs for reliability. This research incorporates this practice as well and adopts, namely, voltage-sharing method where all of the SMs including the redundant ones participate in the modulation and switching, i.e., shaping of dc or ac voltages [8].

B. Control Method of MMC

Fig. 1 presents a block diagram of a typical MMC control system. The higher-level control includes active and reactive

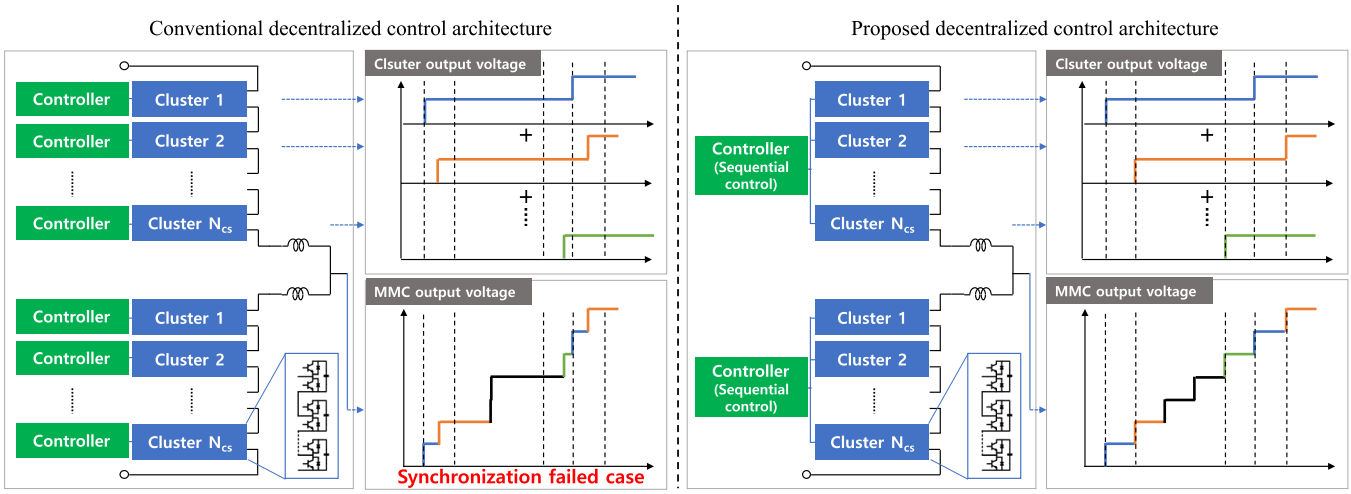

Fig. 2. Diagram of clustering and interleaving schemes: Time-interleaved clusters of SMs with nearest level control for high-level MMC.

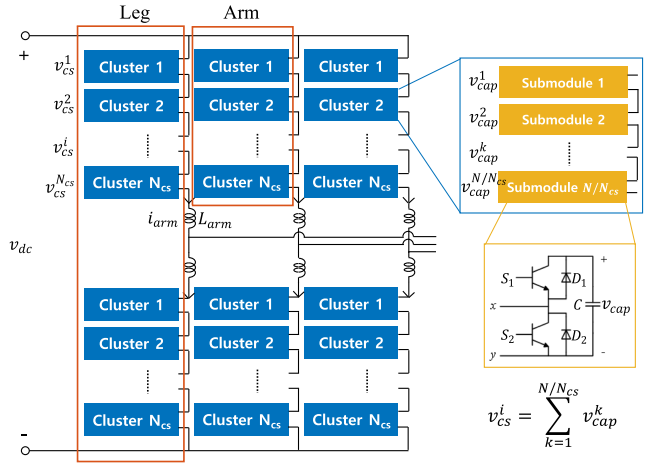

Fig. 3. Structure of MMC with clusters of SMs.

power controls, DC-bus voltage control, and power synchronization control. Current control should be the primary control of any grid-connected VSC applications for which decoupled dq current control method is widely used to control active and reactive powers independently. In particular, MMC requires specialized modulation and capacitor voltage balancing method. The arm-balancing control includes circulating current suppression control (CCSC) and total capacitor voltage control. The conventional dq current control method and CCSC are implemented for the MMC under study in this article.

C. NLC Method Reviews

The principle of NLC approximates output voltage reference with the nearest available level with high-frequency sampling. This approximation can be formulated by applying the round function. Thus, the output voltage reference is converted to an integer level that looks like a staircase. The NLC method requires a sorting algorithm to balance the SM capacitor voltage. The sorted index of capacitor voltages is updated every 800 μs to highlight the benefit of the proposed method and avoid the impact of the balancing scheme on the results.

In NLC, the sampling frequency needs to be high enough to avoid steps exceeding one level for the best voltage quality. Then, the minimum requirement of sampling frequency for all SMs to equally participate in the fundamental frequency modulation can be calculated as follows:

$$f_{s,\min} = \pi N f_0 \tag{1}$$

where f_0 and N are the fundamental frequency and the number of SMs per arm, respectively [11]. Note that the minimum sampling frequency above is determined solely based on the fundamental frequency. In practice, control signals and oscillations caused by such as CCSC, third harmonic injection, measuring errors, delays, need to be incorporated into the modulation signals. Thus, it is not uncommon to observe that NLC with $f_{s,\min}$ results in two- or three-level voltage steps at the steepest slope of the reference. However, for a typical large number of submodules (e.g., $N > 40$), $f_{s,\min}$ should be a useful reference and is thus adopted in this research especially because the improvement in the harmonic performance is not noticeable by increasing the frequency beyond $f_{s,\min}$ as well discussed in [11]. The detailed harmonic analysis is discussed in Section II-D.

D. Harmonic Analysis of NLC Method

The harmonics of an output voltage through the NLC can be represented by Fourier series expansion [29]. The output voltage is basically a summation of square waves, as shown in Fig. 4. The Fourier series expansion of the ith single square wave is stated in (2).

$$V_i(\omega_0 t) = \frac{4V_{dc}}{\pi N} \sum_{h=1,3,5\cdots}^{\infty} \frac{1}{h} \cos(h\alpha_i) \sin(h\omega_0 t) \tag{2}$$

where V_{dc}, h, α_i, and ω_0 are dc voltage, harmonic order, the phase of square wave, and the fundamental frequency in radian, respectively. The square wave can be created when the round value of turn-on reference (n_{ref}) at nth time step is increased

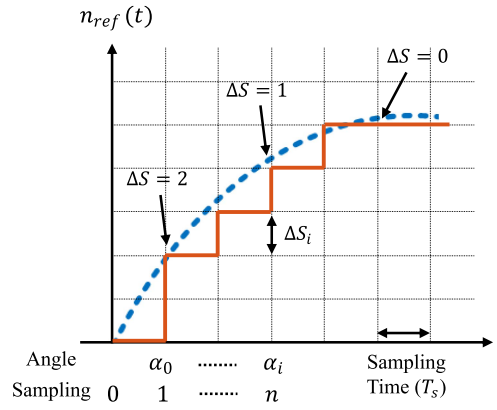

Fig. 4. The output voltage of the NLC method for harmonic analysis.

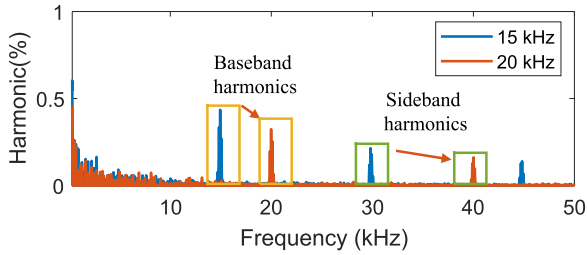

Fig. 5. Harmonic spectrum of 15 kHz and 20 kHz sampling frequency.

or decreased. The switching phase α_i is found from the change of n_{ref} at given sampling time as follows:

$$\Delta S(n) = \text{round}(Nm\sin(\omega_0 nT_s)) - \text{round}\left(Nm\sin\left(\omega_0(n-k)T_s\right)\right) \quad (3)$$

$$\alpha_i = \begin{cases} \text{does not exist} & \text{if} \Delta S(n) = 0 \\ \omega_0 nT_s & \text{if} \Delta S(n) \neq 0 \end{cases} \quad (4)$$

where T_s, m, and k are the sampling time, modulation index, and a positive integer that starts with one and increments by one each sampling time when α_i does not exist. Therefore, the output voltage is the sum of all square waves with existing α_i, as shown in (5).

$$V_{out}(\omega_0 t) = \frac{4V_{dc}}{\pi N} \sum_{h=1,3,5\cdots}^{\infty} \frac{1}{h} \left[\sum_{i=0}^{M} \Delta S_i \cos(h\alpha_i)\right] \sin(h\omega_0 t) \quad (5)$$

where M and ΔS_i are the number of square waves in a quarter fundamental period and the value of ΔS in (3) when α_i exists, respectively. This harmonic calculation method incorporates contribution of the third harmonic injection by counting the α_i when ΔS is a negative number. More accurate analytical results compared to the conventional method [29] are shown.

Based on the (5), the harmonic components spectrum and the total harmonic distortions (THD) along with the sampling frequency (reciprocal of the sampling time) can be calculated and plotted in Figs. 5 and 6: V_{dc}, N, and m are 240 kV, 108, and 1.0, respectively. As expected, it demonstrates that the baseband and sideband harmonic magnitude of the MMC output voltage is

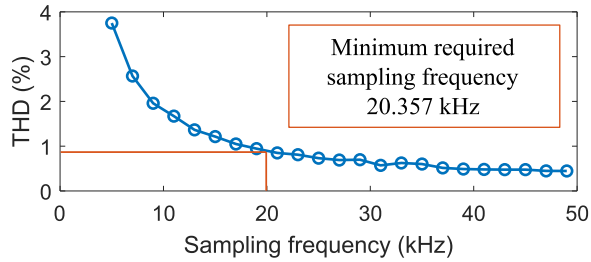

Fig. 6. The total harmonic distortion of output voltage over the sampling frequency.

proportional to T_s (inverse proportional to f_s). To make the most of the MMC, one may develop a criterion that all SMs should participate in voltage shaping for fundamental frequency modulation and then calculate the minimum requirement of sampling frequency based on (1), which turns out to be 20.357 kHz for the MMC under study. If the sampling frequency satisfies this requirement, THD meets the recommendation of IEEE standard for HVDC terminal [30] and guarantees THD lower than 1%. However, the higher dc voltage and level of the MMC-HVDC system, the more difficult it becomes for modulation processes to satisfy the minimum sampling frequency.

III. Clustering and Interleaving Schemes

A. Clustering and Interleaving Schemes

We propose the clustering and interleaving schemes as a practical framework to fully utilize scalability of high-level MMC for voltage quality. The computing processes for modulation of MMC (e.g., sorting, balancing, and data reading/writing) take time to perform in proportion to the number of SMs. Therefore, achieving the desired control sampling time in a high-level MMC-HVDC system becomes challenging because the larger number of SMs requires a longer control period to execute all the tasks, as shown in Fig. 1. The time-interleaving of the clusters relieves this critical constraint for high-voltage MMC applications. Interleaving of the cluster output voltage is achieved by faster iteration of a single cluster controller. The functional roles of the conventional arm controller are played through iteration of the controller, as shown in Fig. 7. The master controller handles higher-level control, arm-balancing control, and current control, and generates reference signals for the cluster controller. The reference signal is transmitted at the beginning of each master sampling time. The cluster controller performs cluster voltage balancing control, SM voltage balancing control in clusters, and gate signal generation tasks per one sampling time ($1/N_{cs}$) of the master controller sampling time.

No change in the hardware is required for designing the cluster controller. Modest change in the arm control architecture enables the design flexibility and scalability of MMC for various voltage levels cost-effectively. In addition, the proposed scheme eliminates the inter-controller synchronization, which is often difficult to achieve in the real world due to communication errors, by using a single controller, as shown in Fig. 2; thus, the proposed scheme enables the extension of the level of MMC in a more efficient compared to the prior methods [10], [23], [24]. For

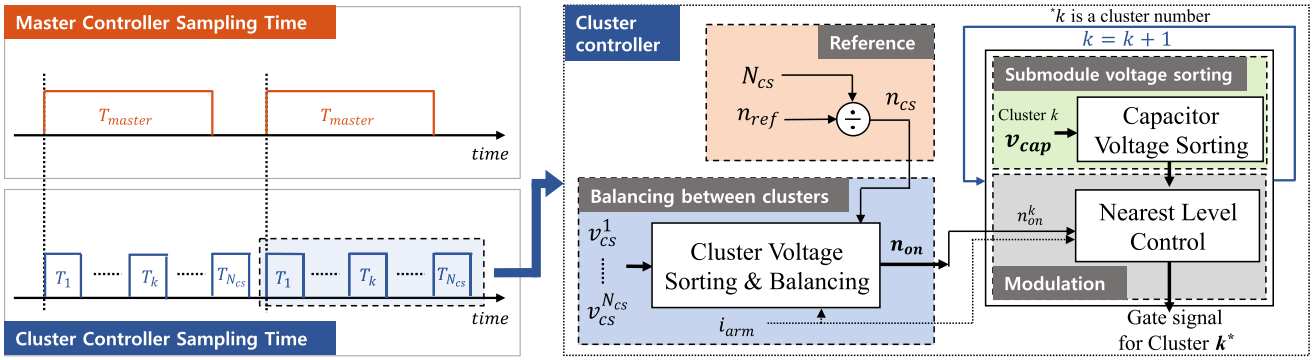

Fig. 7. Block diagram of the cluster controller.

cluster voltage balancing, the proposed method uses a prevalent sorting process similar to [23]. The equally time-shifted square waveform of voltage, i.e., the main feature of the proposed method, enables the desired performance of voltage quality through a high-level MMC.

B. Determination of Number of Clusters

The number of clusters (N_{cs}) is an essential design parameter of the cluster-based MMC-HVDC system. Unnecessarily large N_{cs} may impose an additional computing burden for cluster voltage balancing, shading the functional benefits of clustering and interleaving schemes. On the other hand, if N_{cs} is not sufficient, we cannot exploit the expected benefits. This article thus provides a theoretical and practical guideline to select N_{cs} by investigating the boundary conditions. It is advised to set the number of clusters (N_{cs}) to be a divisor of the number of SMs (N) in the design stage for the best performance. However, redundancy and cluster balancing schemes can handle contingency, e.g., SM fault, leading to clusters with different number of operating SMs as investigated in Section IV-D.

The upper limit of the execution time is a reciprocal of the minimum sampling frequency as expressed in (1).

$$T_{s,\max} = \frac{1}{f_{s,\min}}. \tag{6}$$

The execution time per cluster (T_{exe}) absorbs the communication time (T_{com}), sorting and data reading time (T_{sort}), balancing and data writing time (T_{bal}), and should allow for some computation margin. T_{com} indicates the time taken to receive the modulation index from the master controller (higher-level control, arm-balancing control, and current control) through communication (i.e., Aurora protocol in this article). T_{sort} represents the time that DSP reads the sorting result from FPGA through direct memory access (DMA). T_{bal} indicates the time for DSP to determine the firing pulses according to the sorting results and writes the digital information back to the memory so that the FPGA can read it. This execution time is the lower limit of sampling time.

$$T_{exe} = T_{com} + T_{sort} + T_{bal} + T_{margin}. \tag{7}$$

The available sampling time of each cluster controller (T_{avl}) should be chosen in a way that it lies in the range between the minimum execution time per cluster and the upper limit of execution time as expressed in (8).

$$T_{exe} < T_{avl} < T_{s,\max}. \tag{8}$$

TABLE I
EXECUTION TIME OF THE CONTROL FUNCTIONS IN THE EXPERIMENT

The number of SMs per cluster	27	54	108
T_{com}	6 μs	6 μs	6 μs
T_{sort}	5 μs	11 μs	22 μs
T_{bal}	6 μs	7 μs	8 μs
T_{exe}	25 μs	36 μs	54 μs

Table I shows the execution time of each control function per cluster. These are measured from the control board for the HILS study by varying the number of SMs. A parallel bubble sort algorithm was implemented in the control board with heterogeneous architecture digital signal processor (DSP)/field programmable gate array (FPGA). T_{margin} was set to be 50% of other execution time ($T_{com} + T_{sort} + T_{bal}$). Obviously, T_{exe} increases with number of SMs. Based on Table I, $T_{s,\max}$ and T_{exe} can be plotted as shown in Fig. 8(a) for varying number of SMs. This article investigates three cases of T_{exe} (i.e., 1, 2, and 4 clusters) to see how clustering changes the execution time. The subscript number of T_{exe} then indicates the number of clusters. The execution time per cluster is measured to be 54 μs, 36 μs, and 25 μs as the number of clusters increases. The first case operating with a single cluster could be considered as the conventional architecture. Note that the upper limit of execution time, $T_{s,\max}$, reaches 49.12 μs based on (6) for the target MMC with 108 SMs, advising that the given hardware resources with the conventional architecture cannot satisfy this constraint as T_{exe} was measured to be 54 μs. However, the proposed clustering can reduce T_{exe} to a value less than $T_{s,\max}$. The benefits should grow further for higher voltage applications where the desired level of MMC needs to be increased, implying further decrease in $T_{s,\max}$.

For the MMC under study, the (8) is visualized as in Fig. 8(b). If N_{cs} is set to be two, the sampling time can be selected in the range from 36 μs to 49.12 μs. If N_{cs} is chosen to be four, the sampling time can be selected in the wider range from 25 μs to 49.12 μs. However, note that the rate of change in T_{exe} decreases as the number of clusters increases because of the additional voltage balancing computation burden for cluster

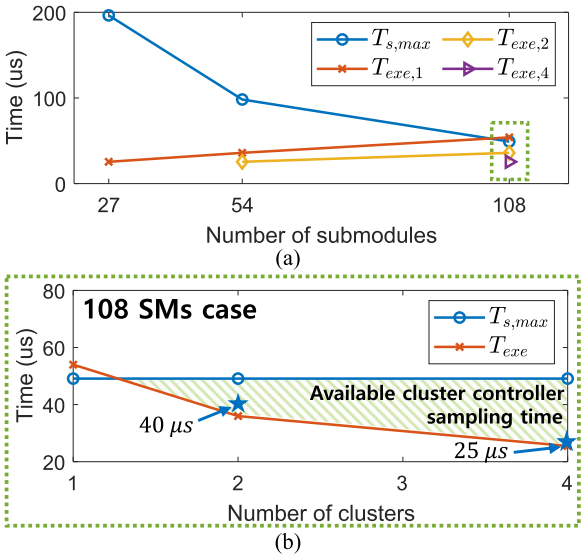

Fig. 8. The upper limit of execution time and the execution time of cluster controller according to (a) the number of SMs and (b) the number of clusters for 108 SMs. The blue star indicates the sampling time selected in the experiments.

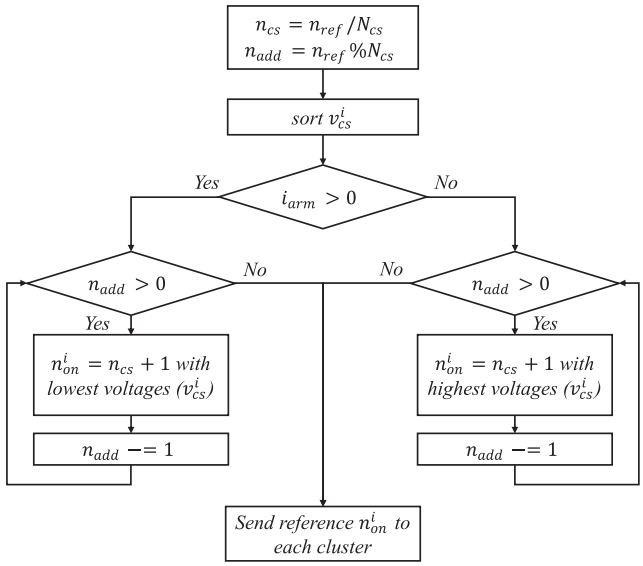

Fig. 9. Flow chart of cluster voltage balancing algorithm.

voltage balancing control (See Section III-C for more detailed discussion). Moreover, as the number of SMs decreases, T_{exe} and the sampling period of the staircase waveform ($T_{cluster}$) decrease as well. However, due to the single controller strategy, the total execution time for the modulation of the entire arm increases, as shown in (9). This increase in execution time specifies the desired time constants for other controls, which impacts the master controller's sampling time. Typically, the master controller's sampling time falls within operable range when the cluster controller's sampling time is determined using the proposed method. Thus, we do not set any constraints on the master controller. We have concluded that two clusters are sufficient for the target system. However, results with four clusters are additionally shown in the HILS study to further demonstrate the performance of the proposed method. Incidentally, the HILS study encountered no issues in the case with 4 clusters (25 μs). This is because the time constant of the current control (i.e., the fastest control of the master controller) is 2 ms, which is 20 times greater than 100 μs.

$$T_{master} = T_{cluster} \times N_{cs}. \tag{9}$$

Taking clusters greater than the minimum extends the feasible range of cluster controller sampling time as long as the hardware supports. Engineers may program the control sampling frequency in this range to accommodate the grid needs. For example, if the system is prone to harmonics or control stability issues, the sampling time could be adjusted to avoid them. Section IV-C demonstrates the flexibility in choosing the control sampling frequency with two scenarios: using two clusters with a sampling time of 40 μs (corresponding to a sampling frequency of 25 kHz), or four clusters with a sampling time of 25 μs (corresponding to a sampling frequency of 40 kHz). The execution time should also account for a fixed time for communication and modulation. The optimal number of clusters and sampling time should be selected based on specific project requirements for grid interconnection and control performance.

C. Cluster Voltage Balancing Control

The master controller calculates n_{ref} to generate the appropriate output voltage. However, n_{ref} is not always an integer multiple of N_{cs}, so there must be the remainder. This remainder at every time step induces an error in the sum of capacitor voltages in clusters and causes the imbalance. The clustering and interleaving schemes need to compensate for the error due to the remainder and balance the cluster voltages, referred to as cluster voltage balancing in the following.

According to the arm current direction, n_{ref}, and v_{cs}^i (sum of capacitor voltage for the i_{th} cluster), the cluster controller determines how many SMs should be inserted in each cluster for the sake of balancing their sum of SM voltages. Its principle is illustrated in Fig. 9 as a flowchart and is summarized as follows:

1) Calculate the quotient and remainder of n_{ref} divided by N_{cs}.
2) Sort the v_{cs}^i of every cluster.
3) The reference values of the clusters were adjusted by incorporating the error due to the remainder using the same principle as NLC.

The proposed method is computationally efficient as it involves sorting only a small number of cluster voltages, thereby limiting the calculation burden. Furthermore, the method ensures accurate generation of the desired output voltage since all remainder SMs are utilized to shape the output voltage.

IV. Hardware-in-the-Loop Simulation Results

A. System Configuration

Fig. 10 shows a half-bridge MMC-HVDC system configuration for the HILS study. This $\pm$120 kV HVDC system transfers 200 MW power from the rectifier to the inverter through a

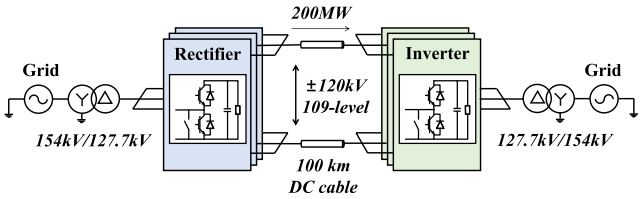

Fig. 10. Diagram of MMC-HVDC system for HILS.

TABLE II
STUDY CASES FOR HILS

Number of clusters		Sampling time	
Rectifier	Inverter	Rectifier	Inverter
2	4	40 μs	25 μs

TABLE III
CIRCUIT PARAMETERS FOR HILS

Parameters	Value
Grid voltage	154 kV
Fundamental frequency	60 Hz
Short circuit ratio (SCR)	5
Transformer ratio	154 kV/127.7 kV
Transformer leakage reactance	0.138 p.u.
Rated power	213.6 MVA
SM capacitance	7000 μF
Arm inductance	25 mH (0.1235 p.u.)
Number of SM per arm (N)	108 (including 8 redundant SMs)
DC bus voltage	$\pm$120 kV
Rated SM capacitor voltage	2.22 kV

100 km dc cable. The number of clusters and sampling time are presented in Table II. The rectifier has two clusters (54 SMs per cluster) architecture with 40 μs sampling time for cluster controller. The inverter has four clusters (27 SMs per cluster) architecture with 25 μs sampling time for cluster controller. The steady-state control performance analysis validates that the proposed schemes successfully perform with conventional MMC controls. Also, the simulation studies demonstrate that all SMs participate in fundamental frequency voltage shaping, fully exploiting the advantages of the high-level MMC to improve the voltage quality. The detailed circuit parameters are shown in Table III. It is worth noting that the simulation parameters for the cluster (e.g., the number of clusters and cluster sampling frequency) are determined by (8) in Section III-B. The target grid strength is specified with the short circuit ratio (SCR), i.e., the ratio between short circuit MVA at the point of common coupling (PCC) of the HVDC and grid.

Fig. 11 shows a photo of the entire HILS equipment. The MMC-HVDC system is modeled in the RTDS and investigated with a simulation time step of 45 μs. Each leg of the MMC system is emulated on a Xilinx VC707 FPGA board with a simulation time step of 2.8125 μs. Each MMC system requires three FPGA units for the converter model. The ac sides of both MMCs are modeled in the NovaCor RTDS hardware. Fiber optic cables are required to connect the FPGA unit with the cluster controllers. The control board includes a measurement board, master control board, and cluster control board. All controllers have the same hardware specifications, including both DSP and

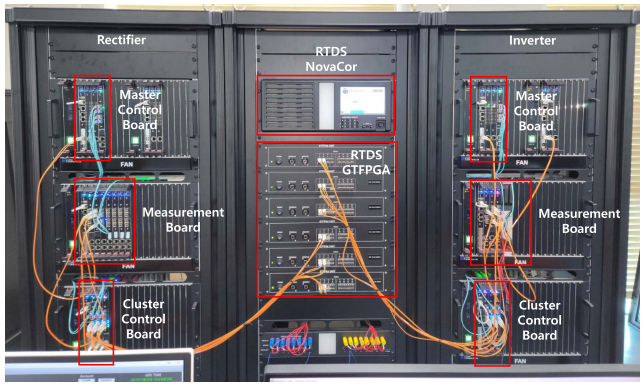

Fig. 11. Equipment for HILS: RTDS and controllers.

FPGAs; ADSP-TS201SABP (Dual-core DSP), Xilinx Spartan-6 FPGA, and two Kintex-7 FPGAs. The measurement board reads the grid and converter information. The master control board is designed for controlling the dc voltage, active power, reactive power, and current control. The cluster control board is designed for each of the three legs.

B. Steady-State Control Performance Analysis Without SM Fault

The performance of the proposed clustering and interleaving schemes is validated through various studies. The steady-state operations of the rectifier (two clusters with 40 μs) (a) and inverter (four clusters with 25 μs) (b) are shown in Fig. 12. The steady-state condition is 200 MW active power transfer with power factor 1. The secondary ac output voltages, output currents, circulating currents, and SM capacitor voltages of each cluster are all stable. The ac output voltage contains 15% of third harmonic due to third harmonic injection in the control system. Furthermore, the cluster voltage balancing control performs as desired without causing any imbalance, as shown in Fig. 12(4) which provides the capacitor voltages of 8 SMs from the upper arm of phase a.

Fig. 13 shows the sampling time of output voltage is identical to the sampling time of the cluster controller, satisfying design criteria or philosophy one can set up for the MMC. Furthermore, Fig. 13(a) and (b) illustrate how the slope of a reference signal can be influenced by various MMC control components. Specifically, the slope is affected by the fundamental component, the third harmonic injection component, the second harmonic component due to CCSC, and the oscillation component caused by communication delays and measurement errors. The fundamental and third harmonics typically result in a steeper slope, which can be 1.45 times that of $f_{s,\min}$. Additionally, the second harmonics of CCSC and other components can cause further increments or decrements in slope. As a result, instantaneous slopes of 1 step per 25 μs (40 kHz) can occur, as illustrated in the zoomed-in Fig. 13(b).

C. Harmonic Performance Analysis

The improved voltage quality owing to the proposed schemes is analyzed with fast Fourier transform (FFT) on the number of

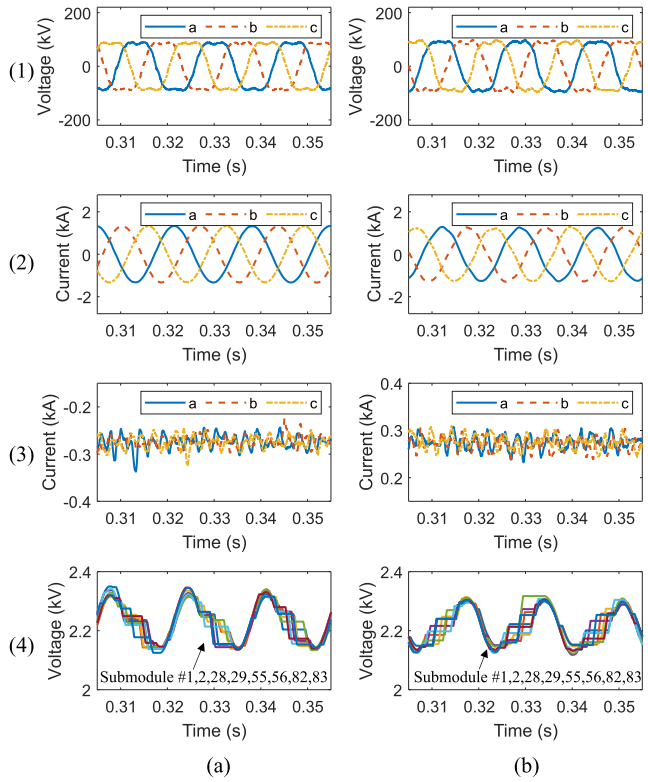

Fig. 12. HILS results at the steady state: (a) Rectifier, (b) Inverter, (1) secondary ac output voltages, (2) ac output currents, (3) circulating currents, (4) capacitor voltages.

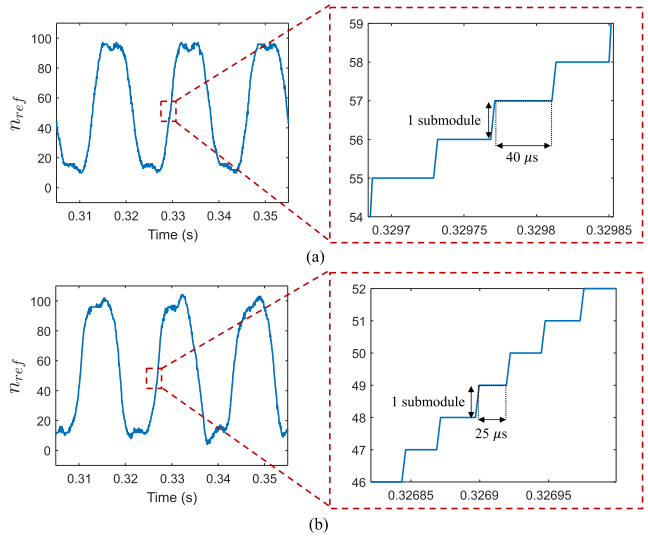

Fig. 13. The number of turn-on SMs of upper arm of (a) rectifier (b) inverter at phase A.

turn-on SMs as shown in Fig. 14. The reason for conducting harmonic analysis on the number of turn-on SMs, when the power transfer is zero, instead of output voltage is to compare the measurements with the theoretical results calculated from ideal square waveform.

Fig. 14(a) and (c) show theoretical harmonic analysis results based on (5) for two cases: two clusters with 40 μs sampling

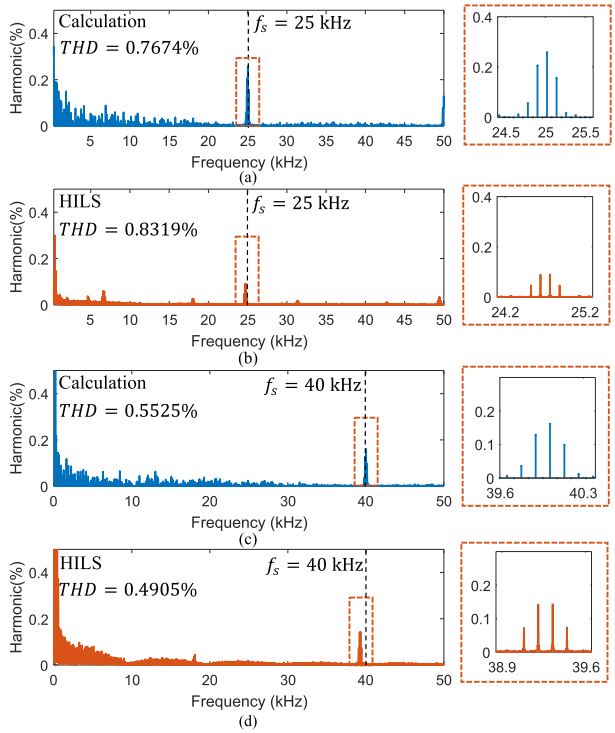

Fig. 14. Harmonic components of the number of turn-on SMs of upper arm at phase A: (a) theoretical results and (b) FFT results of inverter with 25 μs sampling time, (c) theoretical results and (d) FFT results of rectifier with 40 μs sampling time.

time; four clusters with 25 μs, respectively. As can be seen from the theoretical results, the 40 μs case shows the harmonic component at 25 kHz and the 25 μs case shows the harmonic component at 40 kHz. The THD of 25 μs case is lower than THD of 40 μs case. In addition, the clustering and interleaving schemes can shift problematic harmonics to the desired frequency band, and thus help avoid potential harmonic stability concerns.

Fig. 14(b) and (d) show the FFT results of n_{ref} when the controller sampling time are 40 μs and 25 μs, respectively. The HILS study results confirm the theoretical observation that the characteristic harmonic component varies with the sampling frequency of the cluster controller. It is noteworthy that the harmonic frequency of the 25 μs case is slightly different from the theoretical result as shown in Fig. 14(d), because 25 μs is not completely divisible by the substep time of RTDS, i.e., 2.8125 μs, leading to a slight error in the step size of the square waveform. These HILS results for the $\pm$120 kV MMC-HVDC with 109 levels under planning in Korea demonstrate the efficacy and feasibility of the proposed method.

D. Steady-State Control Performance Analysis With SM Faults

The response of the proposed method for the SM failure is shown in Fig. 15. There are two assumptions: the faulty SMs are bypassed by a protection system and the active redundancy method is voltage-sharing method. The faulty SMs (No.28 and No.29) of upper arm is bypassed at $t_1 = 0.05$ s and reconnected at $t_2 = 0.35$ s. Fig. 15(a) and (b) show MMC-HVDC maintains normal operation when submodule faults occur. It is worth

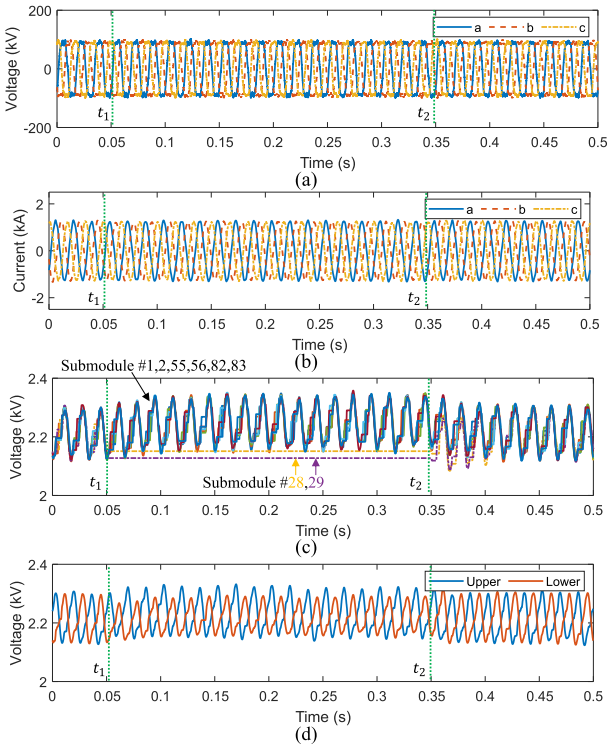

Fig. 15. HILS results of inverter at the SM faults state: (a) secondary ac output voltages, (b) ac output currents, (c) capacitor voltages of upper arm, (d) average capacitor voltages of upper and lower arm.

noting that Fig. 15(c) shows that the capacitor voltages of upper arm SMs are increased, and SMs do not lose their balance in the arm by voltage-sharing method. Fig. 15(d) illustrates that the upper arm and lower arm average capacitor voltage lose their balance during the fault. However, since eight redundant SMs are assumed, the voltages of each SM are still within the normal operating range. The voltage balance is restored immediately after fault is cleared.

V. Conclusion

This article investigated a practical architecture for modular multilevel converters (MMC) to enhance their scalability and flexibility for high-voltage direct current (HVDC) applications. Salient features and contributions of the proposed method are summarized as follows:

- Clustering submodules (SMs) of the MMC and iterative cluster control to resolve high computational burden of the modulation and balancing process for high-voltage transmission applications
- Interleaving clusters of SMs uniformly phased over the output voltage of each cluster to enable the desired voltage quality
- Exploiting functional benefits of the nearest level control (NLC) running on a single cluster controller without a sophisticated synchronization process.
- Cluster voltage balancing scheme to avoid the cluster energy imbalance and ensure reliable operation of clusters.

Practical design guidelines for determining the number of clusters and sampling time based on numerical examples were presented for implementation. The validity and efficacy of the proposed scheme were demonstrated through HILS studies for $\pm$120 kV MMC-HVDC with 109 levels. The proposed architecture has the potential to serve as a unifying control framework across various MMC applications.

References

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[2] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1538–1547, Jul. 2012.

[3] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316–324, Jan. 2011.

[4] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[5] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[6] H. Kim, S. Kim, Y.-H. Chung, D.-W. Yoo, C.-K. Kim, and K. Hur, "Operating region of modular multilevel converter for HVDC with controlled second-order harmonic circulating current: Elaborating P-Q capability," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 493–502, Apr. 2016.

[7] G. T. Son et al., "Design and control of a modular multilevel HVDC converter with redundant power modules for noninterruptible energy transfer," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1611–1619, Jul. 2012.

[8] J. Kang et al., "On exploiting active redundancy of a modular multilevel converter to balance reliability and operational flexibility," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2234–2243, Mar. 2019.

[9] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, 2003, vol. 3, pp. 1–6.

[10] M. Alharbi and S. Bhattacharya, "Scale-up methodology of a modular multilevel converter for HVDC applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4974–4983, Sep./Oct. 2019.

[11] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. Hoboken, NJ, USA: Wiley, 2016.

[12] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *Proc. 4th IEEE Conf. Ind. Electron. Appl.*, 2009, pp. 3399–3404.

[13] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[14] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[15] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[16] J. Rodriguez, J. Pontt, P. Correa, P. Cortes, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 834–839, Aug. 2004.

[17] J. Rodriguez, L. Moran, P. Correa, and C. Silva, "A vector control technique for medium-voltage multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 882–888, Aug. 2002.

[18] S. Yang, Y. Tang, and P. Wang, "Distributed control for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5578–5591, Jul. 2018.

[19] Y. Koyama and T. Isobe, "Current control of modular multilevel converters with phase-shifted PWM using a daisy-chained distributed control system," *IEEJ Trans. Elect. Electron. Eng.*, vol. 14, no. 7, pp. 1095–1104, 2019. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/tee.22905

[20] T. Heath, P. R. Green, M. Barnes, and D. Kong, "Design, construction and testing of a modular multilevel converter with a distributed control architecture," in *Proc. 15th IET Int. Conf. AC DC Power Transmiss.*, 2019, pp. 1–6.
[21] S. Yang, S. Liu, J. Huang, H. Su, and H. Wang, "Control conflict suppressing and stability improving for an MMC distributed control system," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13735–13747, Dec. 2020.
[22] H. Wang, S. Yang, H. Chen, X. Feng, and F. Blaabjerg, "Synchronization for an MMC distributed control system considering disturbances introduced by submodule asynchrony," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12834–12845, Dec. 2020.
[23] Y. Zhou, D. Jiang, P. Hu, J. Guo, Y. Liang, and Z. Lin, "A prototype of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3267–3278, Jul. 2014.
[24] B. Xia et al., "Decentralized control method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5117–5130, Jun. 2019.
[25] C. Kim, C. Park, and J. Kim, "Level selection algorithm with fixed sampling frequency for modular multilevel converter," in *Proc. IEEE 18th Int. Power Electron. Motion Control Conf.*, 2018, pp. 987–992.
[26] C. Kim, S. Sim, C. Park, and J. Kim, "Virtual group control algorithm for modular multilevel converter," in *Proc. Int. Conf. Smart Grid*, 2018, pp. 234–239.
[27] C.-K. Kim, S.-I. Moon, K. Hur, J.-M. Kim, and G. Jang, "HVDC Transmission +1," 2020, doi: 10.1142/11607.
[28] J. Na, H. Kim, S. Kim, C.-K. Kim, and K. Hur, "Cluster voltage balancing control for modular multilevel converter with cluster phase-shifted nearest level control," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2020, pp. 1–5.
[29] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 298–306, Jan. 2011.
[30] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Standard, 519-2014, pp. 1–29, 2014, doi: 10.1109/IEEESTD.2014.6826459.

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