An Experimental Methodology for Modeling the Voltage-Dependent Capacitance and Resistance of Varistors: Implications on the Estimation of the Power and Energy Dissipation at Low Frequencies

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***Abstract*—In this work, a mathematical formulation is presented for estimating current conduction as well as power and energy dissipation in varistors. An experimental approach is introduced for time-domain modeling of varistors under AC voltages that considers their voltage-dependent capacitance and resistance. An application is made for 120 V zinc-oxide varistors stressed with AC voltages generated by a variable-frequency high-power supply; the voltage at the varistors' terminals is recorded along with the current for a low frequency (60 Hz -1000 Hz) and amplitude (50 μA – 1 A) range. The predicted current conduction through ATP-EMTP simulations is in very good agreement with experimental records, in contrast to the simplified (constant-capacitance) modeling approach that underestimates power and energy dissipation. The effectiveness of the proposed macroscopic modeling approach in the low-frequency range is investigated with emphasis given to 400 Hz, commonly employed in aviation systems; the applicability of the proposed model in the high frequency and current range has been evaluated and discussed with the aid of impulse voltage and current experiments.**

***Index Terms*—ATP-EMTP, frequency-dependent response, temporary overvoltages, time-domain modeling, voltage-dependent impedance.**

I. Introduction

METAL oxide varistors, commonly integrated in surge protective devices (SPDs), are essential in modern-day electrical grids, as they protect sensitive electronic equipment against impinging overvoltages [1], [2]; thus, varistor-based SPDs are vital for the reliable and economical operation of power distribution and telecom networks [3]. As a result, academic and industrial research is focused on zinc-oxide (ZnO) varistors and SPDs performance [4], [5], [6], [7] and their effectiveness in protecting electronic and electrical equipment that is vulnerable to overvoltages [3], [8]. The fast response time and zero follow current of varistor-based SPDs makes them ideal for surge protection of power systems.

The physical mechanisms of current conduction through ZnO-based varistors are well described by the Double Schottky Barrier Defect Model [9], [10], [11], [12]. During varistor manufacturing, double Schottky barriers are formed at the grain boundary interfaces of adjacent ZnO grains, that are separated by extremely thin interfacial layers, and the current conduction through the grain boundaries is controlled by the voltage-dependent potential barrier. When a voltage is applied across a grain boundary, the energy bands bend and the potential barrier decreases; unoccupied interface states are dynamically filled under such conditions, and charge accumulates at the interface preventing the lowering of the potential barrier [2], [13], [14]. At higher voltages, the extremely high fields produced at the top of the barrier generate energetic electrons that create holes through impact ionization. The positive hole charge accumulates at the interface and reduces the net negative charge; thus, the potential barrier is lowered and more electrons flow through the barrier leading to the creation of more holes that in turn lower the potential barrier further, and an avalanche effect takes place [1], [2]. The voltage-dependent potential barrier along with the charge trapping and de-trapping processes that take place in the interface is responsible for the varistor's apparent nonlinear voltage-dependent resistivity. The charge trapping and de-trapping processes cause the relationship between charge and voltage to be nonlinear and voltage-dependent [15], [16]; this effect can be considered by employing a voltage-dependent permittivity [17], [18], [19], [20], [21] that leads to a voltage-dependent varistor capacitance.

Although the microscopic conduction mechanisms of ZnO varistors, under a steady state DC, are thoroughly investigated [1], [2], the calculation of the varistor response under large AC voltages is a very challenging task still under investigation [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], since the dynamic, time-dependent charge trapping and de-trapping processes at the interfaces must be taken into account at any time instant [1], [2]. As explicitly stated in CIGRE technical brochure 696 [20] and the recent book [2] a commonly accepted procedure for the estimation of low-frequency conduction and power losses

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is still missing. Several studies and models can be found in the literature focusing on the transient response of metal-oxide varistor-based surge protective devices and surge arresters, under impulses of various frequency and energy content [27], [28], [29], [30], [31], [32], [33], [34], [35]. However, these models focusing on the high-frequency transient response, cannot fully describe varistors response under low-frequency AC large signal voltages, since they do not consider a voltage-dependent capacitance or a dynamic voltage-current characteristic that can reflect the dynamic processes at the interfaces under AC voltages [1], [2], [21]. Recent studies aim to mathematically describe the nonlinear voltage-dependent behavior of varistors and micro-varistors, model their response under applied AC large signal voltages, and explain the phenomena taking place at the grain boundaries on physical grounds [18], [19], [21], [23], [26]. Nevertheless, the models proposed in these studies, some developed for finite element method simulations [18], [23], are difficult to be implemented in electromagnetic transient simulation programs as they are complicated to adapt or/and require physical parameters that cannot be easily experimentally derived and are not provided by manufacturers [21], [23], [26]. In light of the above, the transient response and energy handling capability of varistors under AC and DC temporary overvoltages (TOV), and impulse currents, although studied for the last 30 years [36], [37], still attract the interest of the scientific and engineering community [1], [2], [38], [39], [40], [41].

This work presents a novel mathematical formulation of ZnO varistor current conduction as well as power and energy dissipation under low-frequency AC voltages up to 1 kHz; this mathematical treatment allows for a straightforward application to electromagnetic transient software. An experimental methodology for determining the voltage-dependent capacitance and resistance of varistors is introduced that employs a variable frequency high-power supply to stress varistors with AC voltages of various frequencies (60-1000 Hz) and amplitudes; the voltage at the varistor terminals is recorded along with the current so as to capture the non-linear behavior. An application of the proposed methodology is made for 120 V ZnO varistors that are commonly integrated into SPDs installed in the USA and the varistors' electrical characteristics variation with voltage and frequency is presented. A time-domain model is developed in ATP-EMTP software [42], [43], [44] and is validated against experimental results; simulation results are in very good agreement with experimental data in contrast to the simplified (constant-capacitance) modeling approach that underestimates power and energy dissipation. The applicability of the proposed model in the low-frequency range is investigated with emphasis given to 400 Hz, commonly employed in aviation systems. The proposed macroscopic modeling approach can be an effective tool for reproducing in the time-domain the nonlinear conduction via ZnO varistors and can thus be employed in studies where the power dissipation and energy stress are of interest. The applicability of the proposed model in high frequency and current range has been evaluated and discussed with the aid of impulse voltage and current experiments presented in the Appendix.

Fig. 1. (a) Varistor employed as device under test. (b) Varistor circuit diagram.

II. Mathematical Modeling

A. Current Division and Power Losses Calculation

Under a time-varying electric field, $E(t)$, the varistor (Fig. 1) current density is described as [45]:

$$J(t) = J_R(t) + J_C(t) = \\ = \frac{E(t)}{\rho(E(t))} + \frac{dD(t)}{dt} = \frac{E(t)}{\rho(E(t))} + \frac{d(\varepsilon(E(t)) \cdot E(t))}{dt}, \tag{1}$$

where $J_R(t)$ is the resistive and $J_C(t)$ is the capacitive current density, $\rho(E(t))$ is the varistor's apparent field-dependent resistivity, and $\varepsilon(E(t))$ is the varistor's apparent field-dependent permittivity.

Considering that:

- the electric field and current density can be written as:

$$E(t) = \frac{V(t)}{d}, \tag{2}$$

$$J(t) = \frac{I(t)}{S}, \tag{3}$$

  where d is the disk varistor thickness, and S is the disk varistor surface area (Fig. 1),
- the disk varistor voltage-dependent resistance, $R(V(t))$, and capacitance, $C(V(t))$, are given as:

$$R(V(t)) = \frac{\rho(V(t)) \cdot d}{S}, \tag{4}$$

$$C(V(t)) = \frac{\varepsilon(V(t)) \cdot S}{d} = \frac{\varepsilon_S \cdot S}{d} \\ + \frac{\varepsilon_d(V(t)) \cdot S}{d} = C_S + C_d(V(t)), \tag{5}$$

  where ε_s is the static component of the permittivity, $\varepsilon_d(V(t))$ is the dynamic component of the permittivity, C_S is the static component of the capacitance, and $C_d(V(t))$ is the dynamic component of the capacitance associated with the voltage-dependent charge accumulation at the grain boundary interface.

By substituting (2)–(5) in (1), the current conduction through the varistor, $I(t)$, can be formulated as:

$$I(t) = I_R(t) + I_C(t) = \frac{V(t)}{R(V(t))} + \frac{d(C(V(t)) \cdot V(t))}{dt} = \\ = \frac{V(t)}{R(V(t))} + \frac{d(C(V(t)))}{dt} \cdot V(t) + C(V(t)) \cdot \frac{d(V(t))}{dt}. \tag{6}$$

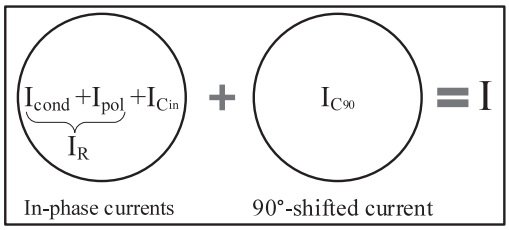

Fig. 2. Schematic diagram of the division of the current flowing through the varistor in terms of the phase shift with respect to varistor voltage.

The current, *I(t)*, can thus be separated into a resistive component, $I_R(t)$, as:

$$I_R(t) = \frac{V(t)}{R(V(t))}, \tag{7}$$

that includes the conduction current, $I_{cond}(t)$, and currents due to polarization losses, $I_{pol}(t)$ [46], [47], and a capacitive component, $I_C(t)$, as:

$$\begin{aligned} I_C(t) &= \frac{d(C(V(t)) \cdot V(t))}{dt} = \\ &= \frac{d(C(V(t)))}{dt} \cdot V(t) + C(V(t)) \cdot \frac{d(V(t))}{dt} \\ &= I_{Cin}(t) + I_{C90}(t). \end{aligned} \tag{8}$$

$I_C(t)$ as evident from (8) can be further separated into an in-phase with the voltage component:

$$I_{Cin}(t) = \frac{d(C(V(t)))}{dt} \cdot V(t), \tag{9}$$

that is associated with the dynamic flow of charge at the barriers due to the time-dependent charge trapping and de-trapping processes that take place in the interface [1], [2], and a 90°-shifted with respect to the voltage component:

$$I_{C90}(t) = C(V(t)) \cdot \frac{d(V(t))}{dt}, \tag{10}$$

that is associated with the displacement current. A summary of the current conduction processes is schematically presented in Fig. 2.

The varistor power losses over time, *P(t)*, are associated with the current component which is in-phase with the voltage, $I_{in\text{-}phase}(t)$, that is calculated based on (7)–(9) as:

$$I_{in-phase}(t) = \left[\frac{1}{R(V(t))} + \frac{d(C(V(t)))}{dt}\right] \cdot V(t), \tag{11}$$

and *P(t)* is given as:

$$P(t) = I_{in-phase}(t) \cdot V(t) = \left[\frac{1}{R(V(t))} + \frac{d(C(V(t)))}{dt}\right] \cdot V(t)^2. \tag{12}$$

(12) can be re-written as:

$$P(t) = \frac{1}{\frac{1}{R(V(t))} + \frac{d(C(V(t)))}{dt}} \cdot V(t)^2 = \frac{V(t)^2}{R_{eff}(V(t))}, \tag{13}$$

where $R_{eff}(V(t))$ is the effective resistance of the varistor.

B. Determination of Varistor Resistance and Capacitance

Varistor resistance and capacitance can be determined by the following procedure.

First by rewriting (6) as:

$$\begin{aligned} I(t) = I_R(t) + I_C(t) &= \frac{V(t)}{R(V(t))} + \frac{d(C(V(t)) \cdot V(t))}{dt} = \\ &= \frac{V(t)}{R(V(t))} + \frac{d(C(V(t)) \cdot V(t))}{dV(t)} \cdot \frac{dV(t)}{dt}, \end{aligned} \tag{14}$$

the varistor resistance, *R(V)*, can be estimated as:

$$R(V) = \left.\frac{V(t)}{I(t)}\right|_{\frac{dV(t)}{dt}=0} = \left.\frac{V(t)}{I_R(t)}\right|_{\frac{dV(t)}{dt}=0}. \tag{15}$$

By applying AC voltages of increasing amplitude and measuring the current along with the voltage at the varistor when the voltage derivative is zero, $(dV(t)/dt = 0)$, the varistor voltage-current characteristic, $V\text{-}I_R$, and consequently its resistance can be obtained; $V\text{-}I_R$ can be mathematically described by an n[th] degree polynomial series of $Log(I_R)$ [24], [25] and can be calculated by:

$$\begin{aligned} V(I_R) = a_3 \cdot [Log(I_R)]^3 + a_2 \cdot [Log(I_R)]^2 \\ + a_1 \cdot Log(I_R) + a_0, \end{aligned} \tag{16}$$

where a_0, a_1, a_2, and a_3, are coefficients that provide the best-fitting of the experimental data. Thus, the resistance of the varistor can be formulated as:

$$\begin{aligned} &R(I_R(t)) \\ &= \frac{a_3 \cdot [Log(I_R(t))]^3 + a_2 \cdot [Log(I_R(t))]^2 + a_1 \cdot Log(I_R(t)) + a_0}{I_R(t)}. \end{aligned} \tag{17}$$

Then, the resistive current, $I_R(t)$, can be calculated by (7), and the capacitive current can be derived by subtracting the resistive current from the total current:

$$I_C(t) = I(t) - I_R(t). \tag{18}$$

Next, by rewriting (8) as:

$$I_C(t) = \frac{d(C(V(t)) \cdot V(t))}{dt} = \frac{d(C(V(t)) \cdot V(t))}{dV(t)} \cdot \frac{dV(t)}{dt}, \tag{19}$$

an equivalent capacitance, $C_{eq}(V(t))$, that is assumed to follow a double exponential variation with the voltage that is convenient for mathematical manipulation and in line with experimental evidence, can be calculated as:

$$\begin{aligned} C_{eq}(V(t)) &= \frac{I_C(t)}{dV(t)/dt} \\ &= \frac{d(C(V(t)) \cdot V(t))}{dV(t)} \\ &= c_1 \cdot e^{(c_2 V(t))} + c_3 \cdot e^{(c_4 V(t))} + c_5, \end{aligned} \tag{20}$$

where, c_1, c_2, c_3, c_4, and c_5 are coefficients that provide the best-fitting of the experimental data. It must be noted that there is no physical significance behind C_{eq}, and it is employed only as

TABLE I
ELECTRICAL CHARACTERISTICS OF THE VARISTOR UNDER STUDY

Maximum continuous operating voltage, U_C (V)	150
1 mA DC Voltage, U_{1mADC} (V)	250
Nominal operating voltage, U_N (V)	120
Nominal discharge current, I_n (kA), 8/20 μs	10
Long-duration (2 ms) withstand capability for 20 times I_{rect} (A)	500

an intermediate step for the estimation of the actual capacitance C.

Finally, by integrating (20) and dividing with, $V(t)$, the varistor voltage-dependent capacitance, is calculated as:

$$C_{eq}(V(t)) = \frac{d(C(V(t)) \cdot V(t))}{dV(t)} \Rightarrow C(V(t)) = \frac{\int C_{eq}(V(t))dV(t)}{V(t)}$$

$$\Rightarrow C(V(t)) = \frac{c_1 e^{(c_2 V(t))}}{c_2 V(t)} + \frac{c_3 e^{(c_4 V(t))}}{c_4 V(t)} + c_5. \quad (21)$$

It is noted that for relatively low voltages, $< V_C/2$, where V_C is the varistor maximum continuous operating voltage, the capacitance of the varistor can be assumed as constant, C_s; this is justified by the fact that at low voltages charge accumulation at the interface is low due to the interfacial charge relaxation process under AC fields [21]. The static component of the capacitance, C_S, can be determined at the time instant, t_0, of zero voltage, $V(t_o) = 0$, where only the last term of (6) remains:

$$C_S \approx C(V(t_0)) = \frac{I(t_0)}{dV(t)/dt|_{t=t_0}}. \quad (22)$$

The process for determining the varistor resistance and capacitance under AC voltages is summarized in the flowchart of Fig. 3. The experimental methodology shown in the flowchart is general and valid for varistors from different manufacturers with different specifications.

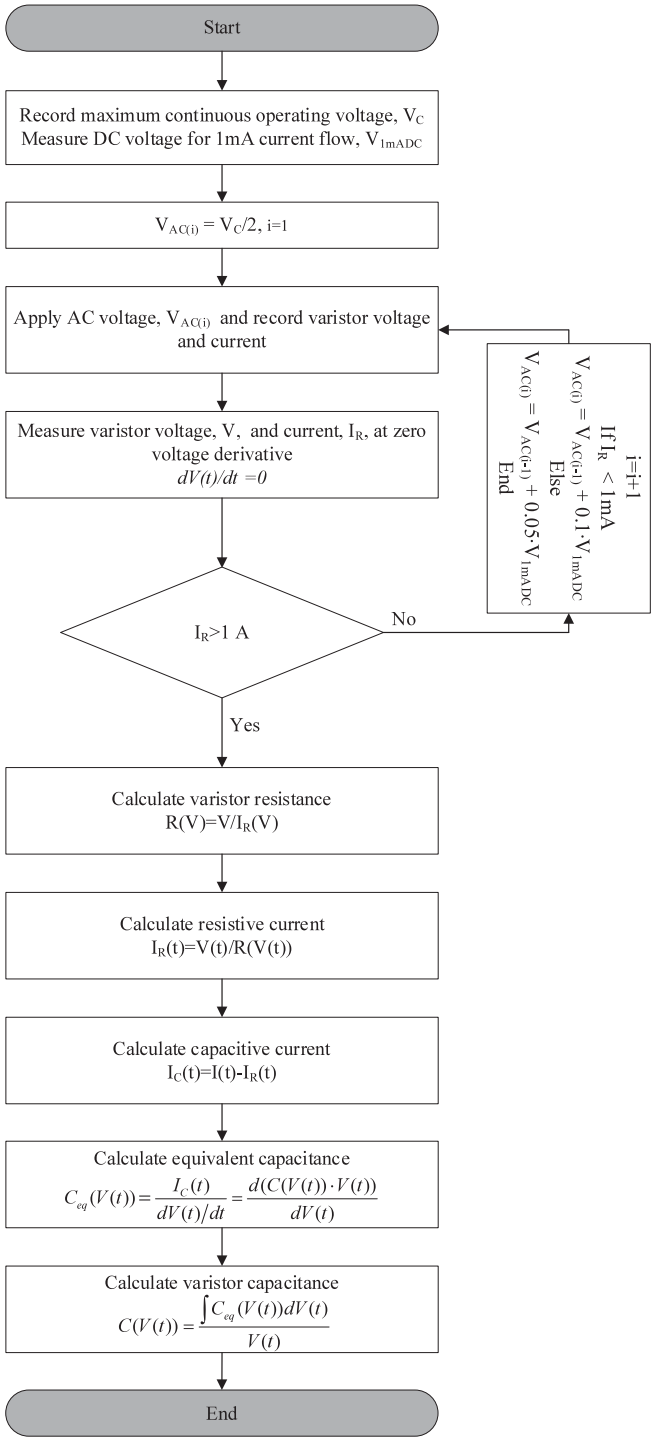

Fig. 3. Flowchart of the process for determining the varistor resistance and capacitance under AC voltages.

III. APPLICATION OF THE PROPOSED METHODOLOGY

The above mathematical analysis and methodology for calculating the varistor voltage-current characteristic, resistance, and capacitance, are implemented on disk varistors of 2.5 mm thickness, d, and 42 mm diameter corresponding to a surface area, S, of 1385 mm^2 (Fig. 1(a)), that are commonly employed in 120 V rms power systems operating at 60 Hz (electrical characteristics presented in Table I). The varistors are stressed with gradually increasing AC voltages (60 Hz) with a maximum value up to about 1.3 times their V_{1mADC}, that is the DC voltage at which 1 mA current flows through their body, by employing the experimental arrangement presented in Fig. 4; current conduction under this AC stress is found up to ~1 A (~75 mA/cm^2).

A 4.8 kVA variable-frequency, programmable AC power supply (Agilent 6843A) was employed that produces AC sinusoidal voltages up to 300 V rms (45 Hz up to 1 kHz), and the current was measured by high-power, low-inductance resistors, R_I. The voltage across the resistors was measured by a 100 MHz differential voltage probe (Tektronix P5205A) and the varistor voltage was recorded by a 500 MHz voltage probe (LeCroy PP008 500). All measurements were recorded with the aid of a 600 MHz digital oscilloscope (Tektronix TDS 3064B) and were acquired 100 ms after voltage application to avoid transient effects as

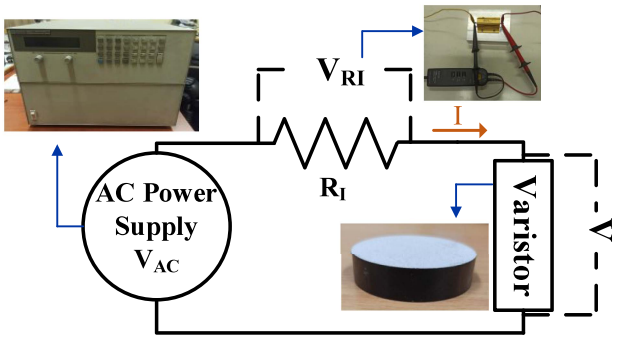

Fig. 4. Experimental arrangement.

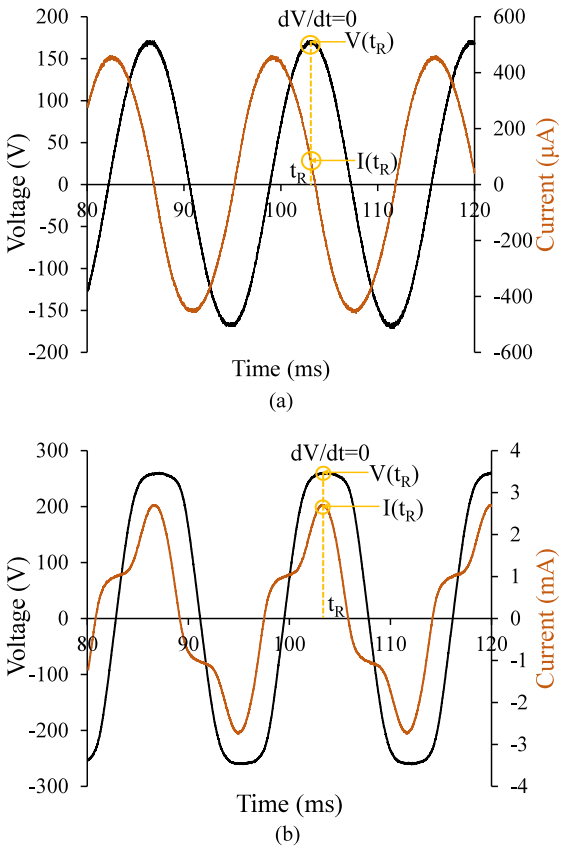

Fig. 5. Typical varistor voltage and current measurements under 60 Hz AC voltages. (a) pre-breakdown region $I(t_R) = 83$ μA and (b) breakdown region $I(t_R) = 2.8$ mA.

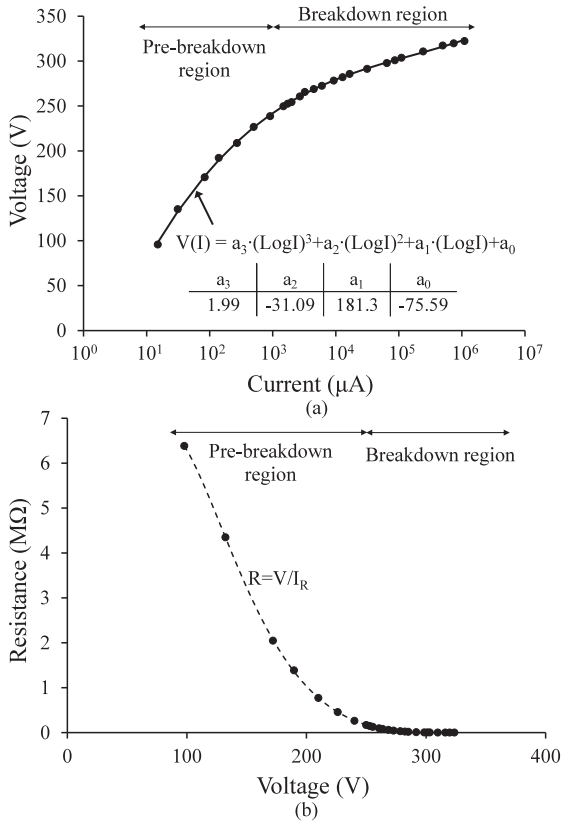

Fig. 6. (a) Varistor voltage-current characteristic. (b) Varistor resistance variation with voltage at varistor terminals.

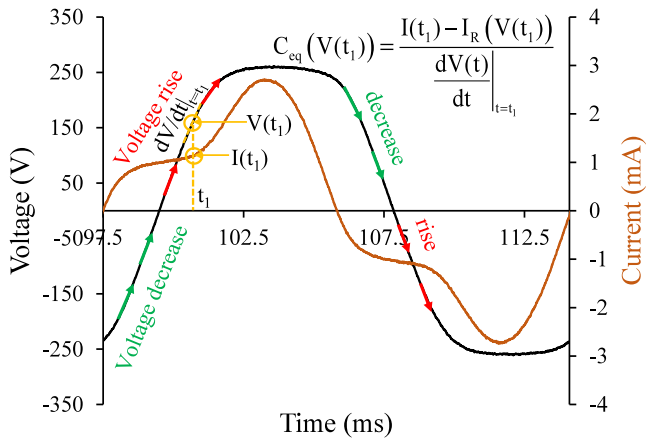

Fig. 7. Calculations of equivalent capacitance at t_1.

well as to have a constant time frame since varistor response is known to vary over time [26]; the ambient temperature was maintained constant at 20 °C during the experiments. Typical measurements of the varistor voltage and current are presented in Figs. 5(a) and (b) when the varistor is in the pre-breakdown and breakdown regions, respectively, depicted in Fig. 6.

By gradually increasing the applied voltage and measuring the voltage and current at t_R (Fig. 5) where $dV(t)/dt = 0$, the voltage-current characteristic, V-I_R, (Fig. 6(a)) and the varistor resistance (Fig. 6(b)) were acquired, as described in Section II. Employing the voltage-current characteristic to calculate $I_R(t)$ and using (18) and (20), the equivalent varistor capacitance, C_{eq}, is derived (Fig. 7). Fig. 8 shows C_{eq} variation with voltage, derived from multiple experiments under AC voltages (60 Hz) of different amplitudes, and Fig. 9 depicts the varistor capacitance, C, variation with voltage calculated by (21), (22).

As evident from Figs. 8 and 9, both C_{eq} and C, increase as the voltage at the varistor terminals, V, increases, with the rate of rise, dC/dV, being generally higher during the rise of the voltage. This can be attributed to the voltage-dependent charge

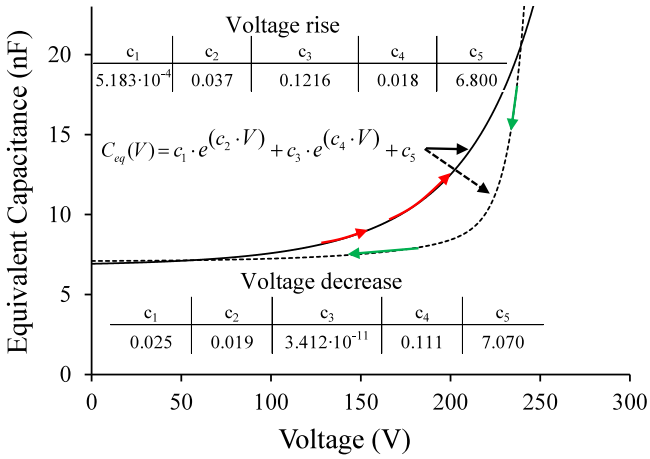

Fig. 8. Equivalent varistor capacitance, C_{eq}, variation with varistor voltage.

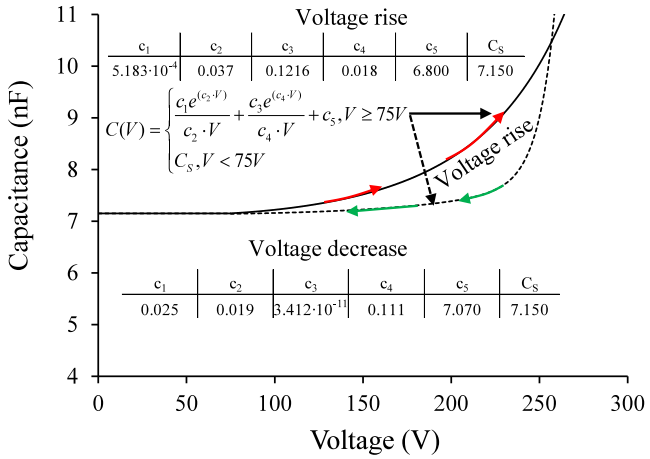

Fig. 9. Varistor capacitance, C, variation with varistor voltage.

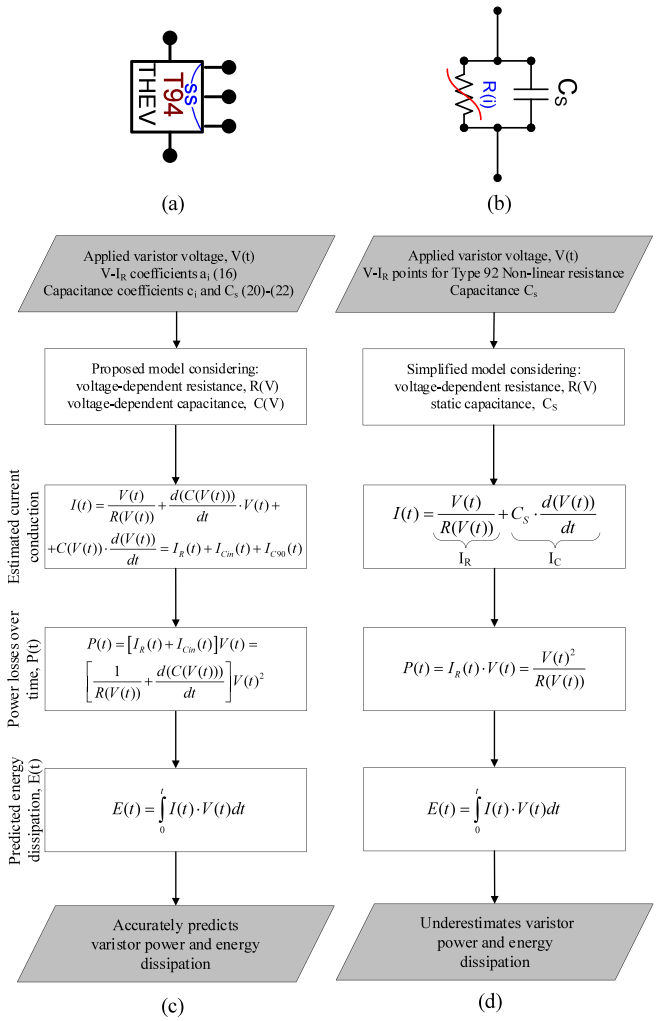

Fig. 10. (a) Proposed model that considers a voltage-dependent capacitance, (b) simplified model with static capacitance. Procedure for estimating varistor dissipation (c) for the proposed model (d) for the simplified model.

trapping and de-trapping, which becomes faster at higher voltage levels as the interface relaxation times decrease [21]. The charge accumulation at the interface during voltage rise is slow and the capacitance rises gradually as the charge increases, while during voltage decrease the charge is released faster, at higher voltages, and the capacitance drops sharply to an almost steady value. Approaching the breakdown region, (voltages higher than ~250 V) where the resistive currents become dominant, and the capacitive currents start to be insignificant, the capacitance can no longer be derived accurately; this is the reason that the curves in Figs. 8 and 9 do not coincide and the region beyond 250 V is considered as unexplored. It is noted that the small signal capacitance of varistors at the breakdown region drops even to negative values when the hole charges begin to predominantly modulate the interface charge [2].

IV. Developed Model and Validation

A simulation model is developed in the electromagnetic transients software ATP-EMTP [42], [43], [44], employing a Thévenin type-94 circuit component and MODELS programming language [48], [49], [50]. When a Thévenin type-94 circuit component is employed in ATP-EMTP, the software computes a Thevenin equivalent of the circuit as seen from the related type-94 component at each timestep. The current, $I(t)$, flowing through the component, along with the voltage across it, $V(t)$, are computed using the Thevenin equivalent as input along with (6). To reach the solution the software iteratively solves the following system of equations at each timestep:

$$V(t) = V_{th}(t) - I(t) \cdot R_{th}, \tag{23a}$$

$$I(t) = \frac{V(t)}{R(V(t))} + \frac{d(C(V(t)))}{dt} \cdot V(t) + C(V(t)) \cdot \frac{d(V(t))}{dt}, \tag{23b}$$

where, V_{th} and R_{th} are the Thevenin equivalent circuit voltage and resistance, respectively. A similar modeling approach employing the type-94 component in ATP-EMTP can be found in literature for modeling the non-linear phenomenon of leader development [51], [52], [53].

The proposed model (Fig. 10(a)) considers a voltage-dependent resistance and capacitance (Sections II and III) and

is compared with a simplified commonly applied model, where a constant capacitance is considered (Fig. 10(b)) in terms of accurately predicting current conduction, energy dissipation, and power losses over time (Figs. 10(c) and (d)).

All the input parameters of the proposed model (Figs. 10(a) and (c)) can be experimentally determined based on the generalized procedure described in Section II.B (Fig. 3) and thus the model can be employed for different varistors types. The coefficients, a_i, (Fig. 6(a)) are employed for the determination of the varistor voltage-current characteristic, *V-*I_R, by employing (16), and the coefficients, c_i along with the static varistor capacitance C_S, (Figs. 8 and 9) are employed for the calculation of, C_{eq}, and C during voltage rise by using (20) and (21); following an engineering approach, C_{eq}, and C are considered constant and equal to the static capacitance C_S, during voltage decrease, since both drop sharply to an almost steady value during voltage decrease (Figs. 8 and 9). The varistor resistance for each voltage is determined by employing linear interpolation on the voltage-current characteristic for numerical stability purposes.

Using the proposed model (Fig. 10(a)), a very good agreement is found between simulation and experimental results concerning the current conduction through the varistor (Fig. 11(a)), while employing the simplified model, the current during voltage rise, where the effect of the voltage-dependent capacitance is more pronounced, is underestimated (Fig. 11(a)), since the in-phase capacitive current, I_{Cin}, associated with the dynamic flow of charge at the barriers is omitted (Fig. 11(b)). This causes the simplified model, as well as other models of varistor-based devices employing constant (voltage-independent) capacitance, to underestimate the power losses over time (Fig. 11(c)) and the absorbed energy (Fig. 11(d)). Concerning the former, while both simulation models compute the same P_{max}, when calculating the root mean square value of *P(t)*:

$$P_{RMS} = \sqrt{\frac{1}{T}\int_{t}^{t+T} P^2(t)dt}, \tag{24}$$

a deviation of up to ~3% is found, while in the absorbed energy, a deviation of up to about 7% is calculated. Although the two models yield relatively small differences, such deviations can be important in simulations where the energy handling capability of ZnO varistors under prolonged temporary overvoltages is investigated.

For example, the energy dissipation of 1 kJ is reached 2 minutes earlier than expected by the simplified model based on the simulation scenario of Fig. 11, which could be critical for the guaranteed safe failure mode of varistor-based SPDs, in terms of the response of the integrated thermal disconnector as well as the estimated time to failure and failure-rate of varistor based SPDs, which are exposed to TOV conditions, such as those installed in wind turbine and PV installations [54], [55].

V. Effect of Frequency

A. Voltage-Current Characteristic and Capacitance

The effect of frequency on the varistor response was examined by applying gradually increasing AC voltages of variable frequency up to 1 kHz, employing the experimental arrangement

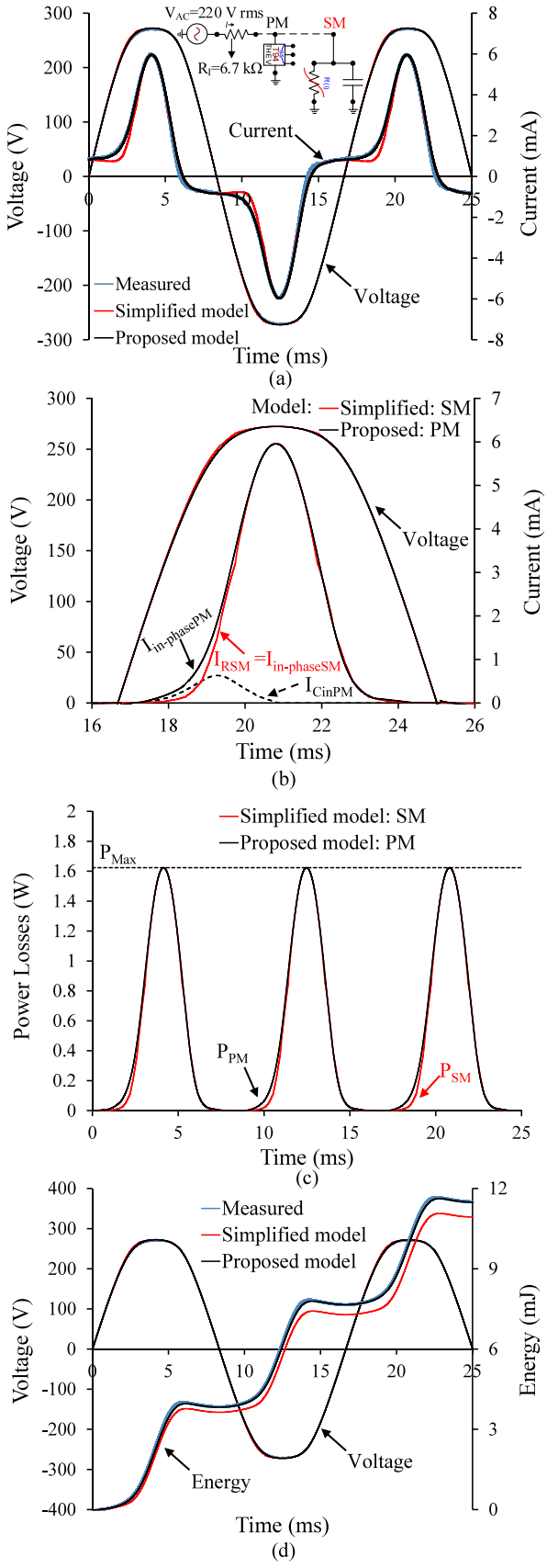

Fig. 11. (a) Measured and simulated varistor voltage and current; inserted simulation circuit including the voltage source and measuring resistance, R_I, of Fig. 4, (b) simulated in-phase currents, (c) simulated power losses over time, and (d) measured and simulated energy absorption.

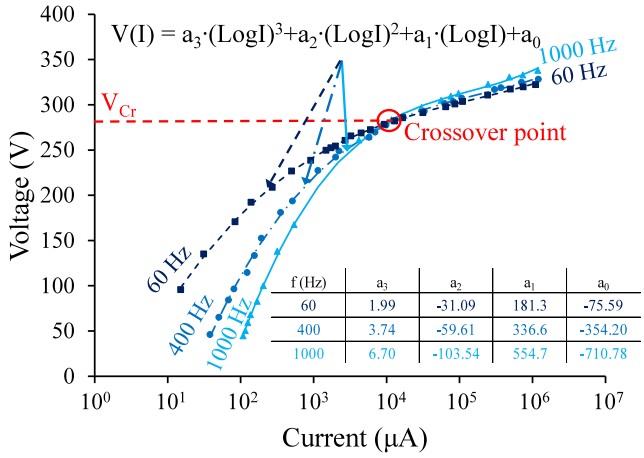

Fig. 12. Varistor voltage current characteristic, *V-I*$_R$, variation with frequency.

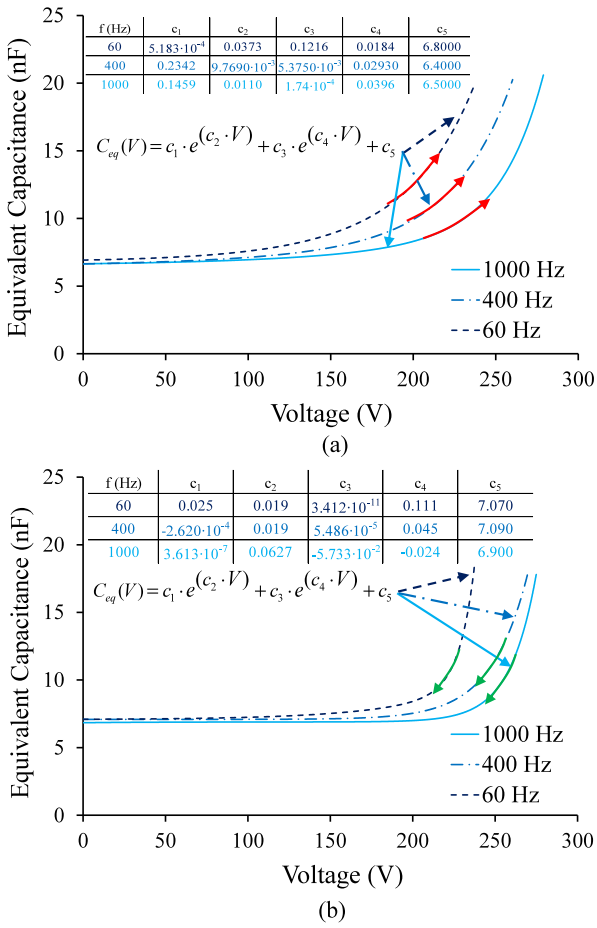

Fig. 13. Equivalent varistor capacitance, C_{eq}, variation with voltage and frequency. (a) Voltage rise and (b) voltage decrease.

presented in Fig. 4. The *V-I*$_R$ characteristic, C_{eq}, and *C* were calculated at each frequency, as presented in Sections II and III. Due to the time-dependent charge trapping and de-trapping, and the relaxation processes during charge accumulation at the grain boundary interfaces, that ultimately affect the potential barrier height, and thus current conduction through the varistor,

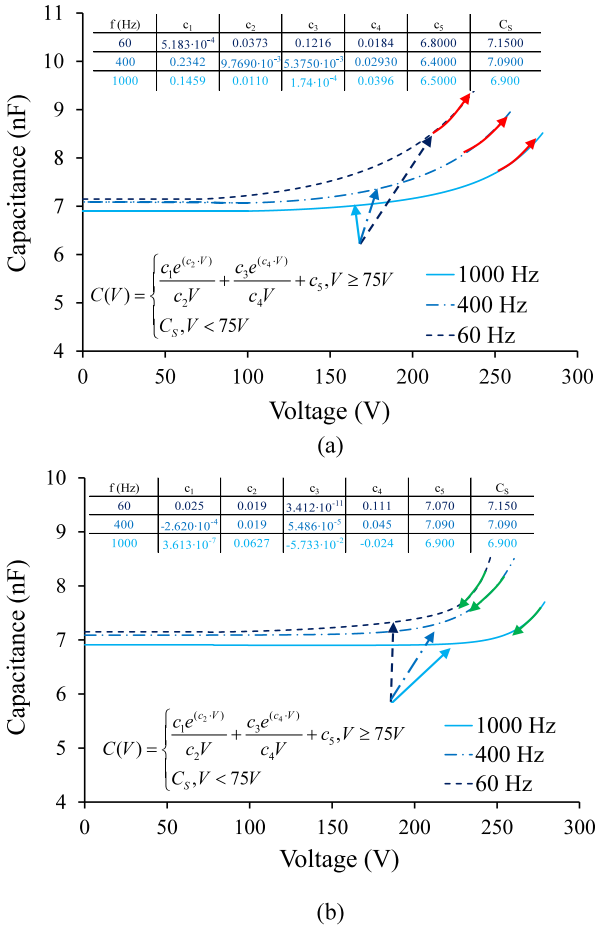

Fig. 14. Varistor capacitance, *C*, variation with voltage and frequency. (a) Voltage rise, (b) voltage decrease.

both the voltage current, *V-I*$_R$, characteristic, and the varistor voltage-dependent capacitance vary with applied voltage frequency (Figs. 12–14).

Fig. 12 shows the voltage-current characteristic variation with frequency. As evident, for voltages up to about V_{1mADC}, for a given voltage, the resistive current rises as frequency increases, while for higher voltage levels the opposite is true. At higher voltages (V>1.1·V_{1mADC} – right from the crossover point in Fig. 12), as hole creation and recombination with the negative interface charge starts to play a more dominant role, in higher frequencies there is less time for minority carriers to travel to the interface and lower the potential barriers, and thus less current flows through the varistor at 1000 Hz than at 60 Hz for a given voltage level (Fig. 12). On the other hand, the low voltage behavior (V<1.1·V_{1mADC} - left from the crossover point) is mainly attributed to the dynamic response of the interface and partially to polarization currents that rise with frequency [46], [47]. As frequency increases, less charge, Q_i, is accumulated in the interfacial layers at the grain boundaries pinning the potential barriers, and more current flows through the varistor. The same effect is also seen in C_{eq}, and *C* variation with frequency (Figs. 13 and 14), that both decrease with increasing frequency and attain their peak value at higher voltage levels. The applicability of

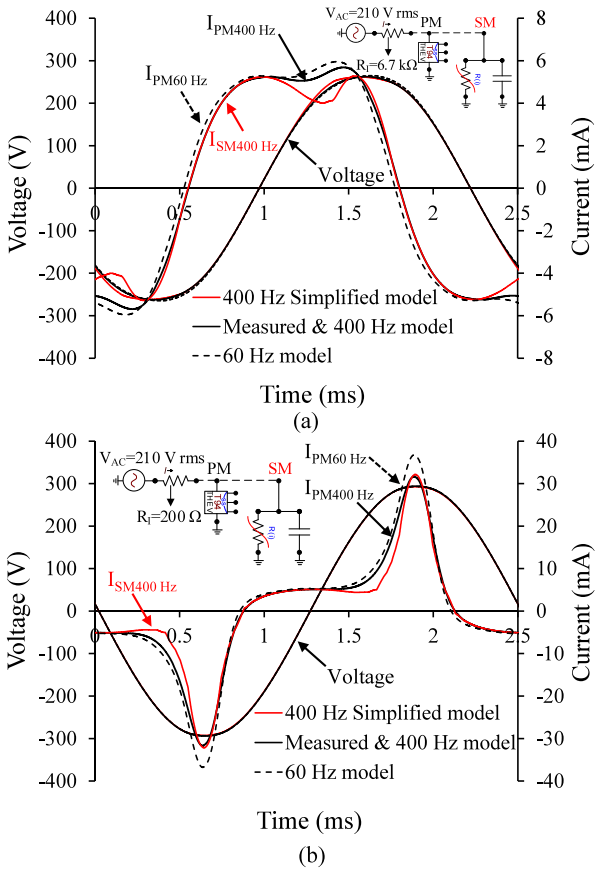

Fig. 15. Measured and simulated varistor voltage and current at 400 Hz applied voltages (a) 210 V_{rms} $R_I = 6.7\,k\Omega$, (b) 210 V_{rms} $R_I = 200\,\Omega$; inset figures in (a) and (b) depict the simulation circuit including the voltage source and measuring resistance, R_I, of Fig. 4.

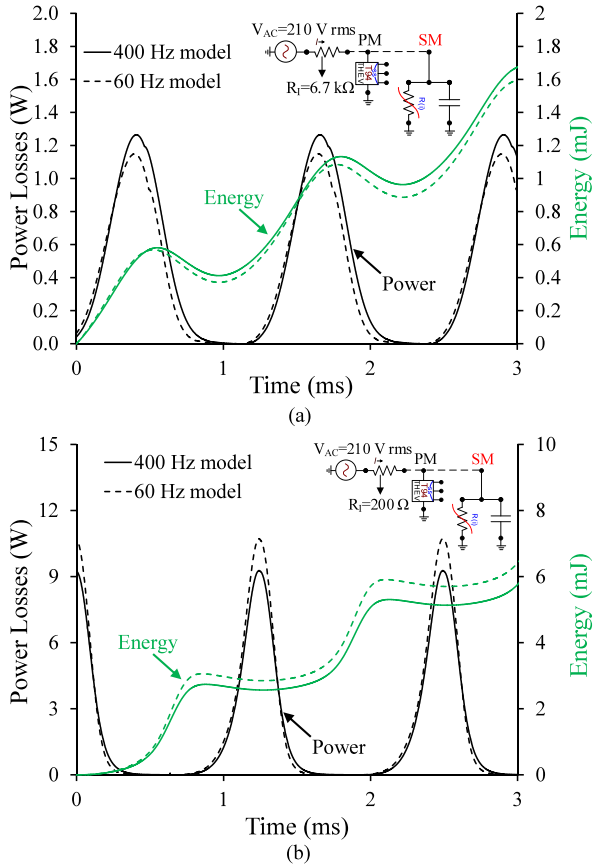

Fig. 16. Measured and simulated varistor energy and power dissipation at 400 Hz applied voltages (a) 210 V_{rms} $R_I = 6.7\,k\Omega$, (b) 210 V_{rms} $R_I = 200\,\Omega$; inset figures in (a) and (b) depict the simulation circuit including the voltage source and measuring resistance, R_I, of Fig. 4.

the proposed experimental approach at higher frequencies corresponding to transient effects is discussed in the Appendix.

B. Proposed Model

To examine the accuracy of the developed 60 Hz model at different frequencies, simulation model results are compared with experimental records of varistor response under 400 Hz voltages, commonly employed in aviation.

As evident from Fig. 15, the 60 Hz model leads to a miscalculation of varistor current conduction under 400 Hz. Discrepancies can be attributed mainly to the variation of the resistive current (Fig. 12) and secondarily to the variation of the dynamic capacitance of the varistor at different frequencies. Thus, to accurately reproduce the varistor response under alternating voltages of different frequencies, the proposed model input parameters (a_i, c_i, C_S) must be calculated at the corresponding frequency (Figs. 12–14) following the flowchart of Fig. 3. Otherwise, the adoption of the power frequency model for higher frequency applications underestimates the power and energy dissipation at nominal voltages and overestimates power and energy dissipation at temporary overvoltages ($V > V_{1mADC}$). The applicability of the model at higher frequencies corresponding to transient effects is discussed in the Appendix.

VI. Conclusion

In this work, a novel mathematical formulation has been presented for estimating the varistor current conduction allowing for a straightforward application to electromagnetic transient software. Based on this mathematical treatment, a generalized experimental methodology is proposed for determining the voltage-current characteristic and voltage-dependent capacitance of varistors and their variation with frequency. An application to a ZnO varistor employed in 120 V power systems at a low-frequency range has shown that:

- The current flow through the varistors can be separated into three components. A resistive component associated with the motion of free charges (resistive current), an in-phase with the voltage capacitive component, associated with the dynamic flow of charge at the barriers and the corresponding currents, and a 90°-shifted with the voltage component, associated with the variation of polarization charges (displacement current).
- The voltage-current characteristic of varistors is frequency dependent in the pre-breakdown and breakdown regions, and the effect of frequency reverses at about V_{1mADC}. For lower voltages as frequency increases and thus less charge is accumulated in the interfacial layers at the grain boundaries, pinning the potential barriers, the resistive

current rises for a given voltage. For higher voltages as hole creation and recombination with the negative interface charge, starts to play a more dominant role, the resistive current decreases with increasing frequency.

- Varistor capacitance rises with voltage and the rate of rise, during a half-voltage wave, depends on whether the voltage is rising or decreasing. During voltage rise, at lower voltages, the charge slowly accumulates at the grain boundary interfaces, and the capacitance rises gradually, while during voltage decrease, at higher voltages, the charge is released faster, and the capacitance drops sharply to an almost static value.
- Varistor capacitance decreases with increasing frequency and attains a peak value at higher voltage levels, as less time is allowed for the time-dependent charge trapping and de-trapping processes to take place and less charge is accumulated at the grain boundaries; a constant-capacitance approach may be acceptable in high-frequency transients.

An experimental approach for time-domain modeling of varistors has been introduced that considers their voltage-dependent capacitance and resistance and a generalized model has been developed in the electromagnetic transient simulation program ATP-EMTP. The model has been validated against experimental measurements and compared with the simplified model that considers a constant capacitance. Comparison of simulation results with experimental records for 120 V varistors has shown that:

- The proposed model can accurately reproduce the varistor response under alternating voltages while employing the simplified (constant-capacitance) model commonly employed in the surge protection industry leads to underestimation of current conduction, mainly during voltage rise of temporary overvoltages, leading to an underestimation of the dissipated power and energy.
- The adoption of the proposed power-frequency (60 Hz) model for higher frequency applications, such as those employed in the aviation industry (400 Hz), underestimates the power and energy dissipation at nominal voltages, and generally overestimates power and energy dissipation at temporary overvoltages.
- The simplified (static-capacitance) model can satisfactorily reproduce the varistor response under nominal voltages and overvoltages lower than the maximum continuous operating voltage of the varistor or high-frequency transients.

In light of the above, the proposed macroscopic modeling approach can be an effective tool for reproducing in the time-domain the nonlinear conduction via ZnO varistors and can thus be employed in studies where the power dissipation and energy stress are on focus. Future work calls for integration into the proposed model of the effects of temperature, defects, and degradation of the varistors.

APPENDIX

To examine the efficiency of the proposed model in the high-frequency range, simulation results are compared with experimental records obtained with the aid of the experimental arrangements of Fig. 17. The capacitance variation with voltage (Fig. 18(a)) and voltage-current characteristic (Fig. 18(b)) have been calculated following an analogous procedure to the flowchart of Fig. 3.

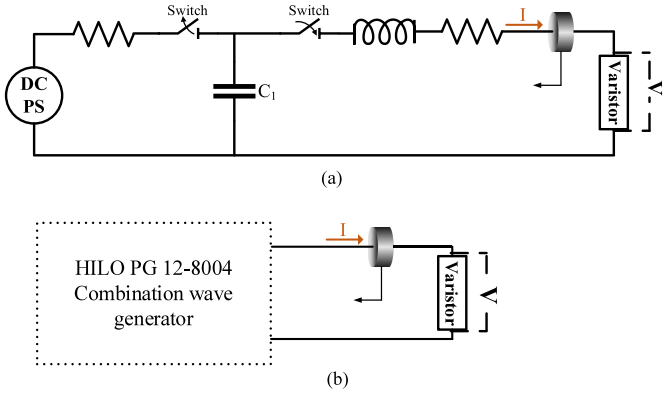

Fig. 17. Experimental arrangements for evaluating the high-frequency response of varistors. (a) Low impulse voltage/current, (b) high impulse voltage/current.

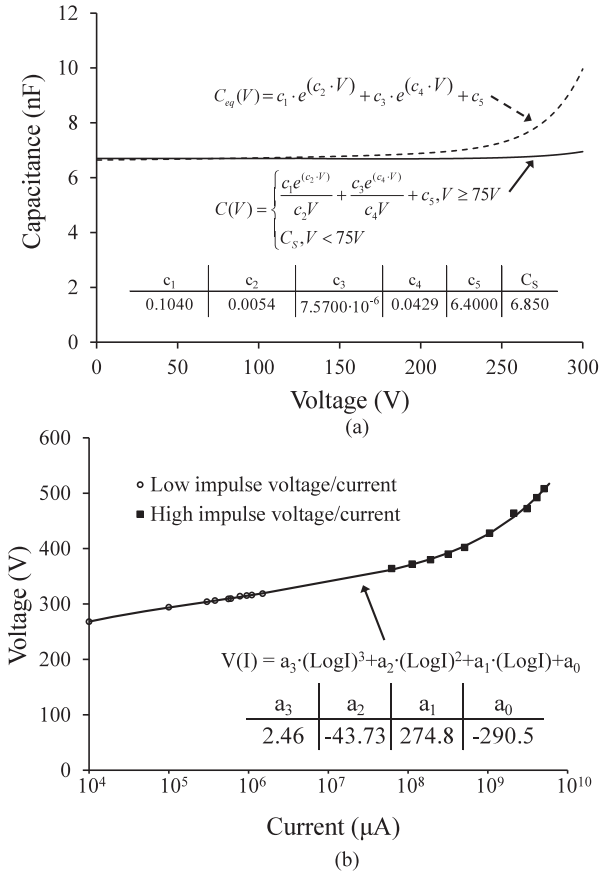

Fig. 18. (a) Equivalent capacitance, C_{eq}, and capacitance, C, variation with voltage based on the experimental arrangement of Fig. 17(a). (b) Voltage-current characteristic, V-I_R based on the experimental arrangements of Fig. 17.

The proposed model can quite accurately predict the varistor response under low impulse voltage/current (Fig. 19(a)) and high impulse voltage/current (Fig. 19(b)). It is important to note that

in such short-duration events since the varistor capacitance variation with voltage is minimal (Figs. 18(a)), the simplified model and other models considering a constant voltage-independent capacitance such as [29], [34] can also adequately reproduce the varistor response. This applies also to high impulse currents (Fig. 19(b)), especially with fast-front times, since the inductive-like effects of the varistor, due to the time needed for the holes to travel to the grain boundary interface and lower the potential barrier, are way more important to consider than the capacitive behavior [2].

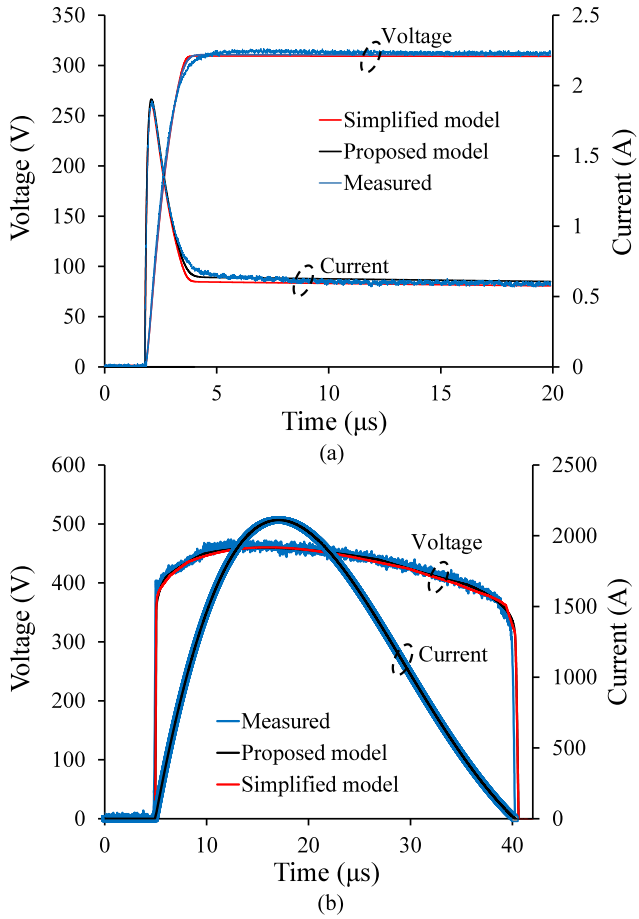

Fig. 19. Measured and simulated varistor voltage and current. (a) Low impulse voltage/current, (b) high impulse voltage/current.

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