Analytical Modeling of Modular Multilevel Converter Under Pole-to-Pole DC Fault and Application to System Design and Protection

Peng Wang, Maren Kuschke, and Kai Strunz

***Abstract*—An analytical model for the half-bridge submodule based modular multilevel converter (MMC) under pole-to-pole fault is formulated, implemented, and validated. The events after the fault occurrence are categorized into four stages, and the equivalent circuit of each stage is derived. A generic equivalent circuit is developed respectively for the analytical calculation of the AC grid currents and the circulating currents during the fault, taking into account the conducting states of the switching devices. With knowledge of those currents, further analytical expressions of the fault currents of the converter arms and the DC grid are derived. Since the analytical expressions of the fault currents are functions of the main circuit parameters and the prefault operating point, the analytical model of the MMC under the pole-to-pole DC fault offers an answer to an entire set of problems. Enhanced insight into the parameters influencing the fault currents is available with the help of the analytical model. As a promising application, the proposed analytical models are utilized for the parameter design of the converter and for the selection of the interrupting capability of the circuit breakers. In the performed validation involving the CIGRE B4 DC test system, the analytical results are shown to be highly consistent with those of computationally more expensive solutions based on numerical simulation.**

***Index Terms*—Analytical models, equivalent circuits, fault currents, HVDC transmission, modular multilevel converter, power system simulation, power system transients, protection, short-circuit currents, system analysis and design.**

NOMENCLATURE

Acronyms

AC	Alternating current.
CB	Circuit breaker.
DC	Direct current.
EMT	Electromagnetic transient.
HVDC	High-voltage direct current.
IGBT	Insulated gate bipolar transistor.
MMC	Modular multilevel converter.
SM	Submodule.
VSC	Voltage source converter.

Variables

$\boldsymbol{A}$	State matrix of AC system equivalent circuit.
$\boldsymbol{B}$	Input matrix of AC system equivalent circuit.
C	Capacitance of submodule.
e	Inner electromotive force of converter.
$\hat{I}$	Current amplitude.
$\boldsymbol{i}$	State vector of AC system currents.
i	Instantaneous current.
j	Phase.
L	Inductance.
M	Modulation index.
N	Number of submodules in one arm.
R	Resistance.
s	Complex frequency.
t	Time.
$\hat{V}$	Voltage amplitude.
$\boldsymbol{v}$	Input vector of AC system voltages.
v	Instantaneous voltage.
ρ	Conducting state of AC circuit breaker.
σ	Operating state of submodule.
ς	Conducting state of arm.
φ	Phase lag of AC grid current with respect to inner electromotive force of converter.
ω	Angular frequency.

Superscripts and Subscripts

$+$	Beginning of stage.
$-$	Ending of previous stage.
0	Instant of fault occurrence.
A	Analytical method.
Af	Alternating feeding.
arm	Arm of converter.
bs	Blocking submodules.
cir	Circulating.
crit	Critical.
cz	Crossing zero.
dc	Direct current.
D	Diode.
e	Inner electromotive force of converter.
l	Lower.

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The authors are with the Chair of Sustainable Electric Networks and Sources of Energy, Technische Universität Berlin, 10587 Berlin, Germany (e-mail: wangpengtu@gmail.com; maren.kuschke@tu-berlin.de; kai.strunz@tu-berlin.de).

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la	Lower arm phase a.
leg	Leg of converter.
N	Numerical method.
ob	Opening breaker.
pre	Prefault.
rip	Ripple.
rupt	Interrupting capability.
s	AC system.
sa	AC system phase a.
ta	Converter terminal phase a.
u	Upper.
ua	Upper arm phase a.

I. Introduction

THE modular multilevel converter (MMC) has become the most prominent converter topology for high-voltage direct current (HVDC) and multi-terminal DC (MTDC) applications [1], [2], [3]. The performance of converters subjected to DC fault is to be considered when developing DC grids. The susceptibility to a DC short-circuit fault, and particularly the potential damage caused to the converter IGBTs due to overcurrent, is an issue that must be addressed. As such, efforts have been taken to investigate the fault responses and protections [4]. In this context, the availability of an analytical model of the MMC under DC fault condition would be very valuable. It would provide an in-depth insight into parameters influencing overcurrent and overvoltage. Thanks to analytical modeling, engineering formulations for system design and circuit breaker configuration become available, providing valuable information for both manufacturers and system operators. This observation has motivated the analytical modeling described in this paper.

An important building block of the MMC is the submodule, denoted by SM in Fig. 1. Submodules are available in several variants. Among those variants, the most common one is the half-bridge submodule for its merits of low initial cost and high efficiency [4]. When employing the half-bridge submodule, an MMC is vulnerable to DC short-circuit faults, among which the pole-to-pole fault is the most severe one [5]. During the pole-to-pole fault, an overcurrent occurs in the converter due to a low DC link voltage. The rate of change of the fault currents is limited by the arm inductors. When selecting an appropriate arm inductance design, the overload capability of the insulated gate bipolar transistors (IGBTs) is to be considered since the IGBTs in the converter arms have limited overload capability and may be damaged by large currents [6], [7]. The fault currents are eventually cleared by opening the AC circuit breakers (CBs). The requirement of the interrupting capability of the circuit breaker relies on the knowledge of the fault currents [8]. Taking into account the physical limitation of the converter and the importance of a secure operation of the power system, it is essential to understand the fault response. It is also essential to quantify the impacts of the system parameters as well as of the operating point on the fault currents.

To quantify the fault currents, numerical simulation may be adopted. In [9] and [10], the solutions of the fault currents are obtained from electromagnetic transient (EMT) simulations for

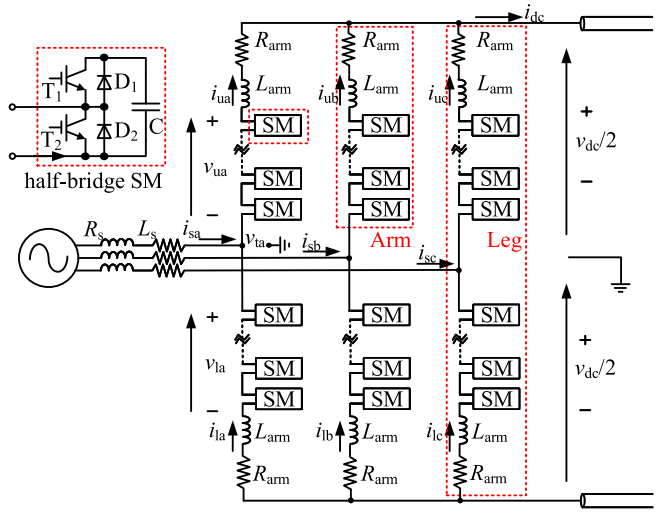

Fig. 1. Basic topology of MMC and circuit of half-bridge submodule.

HVDC systems based on the two-level voltage source converter (VSC) and the MMC. Repeated EMT simulations are necessary to get information such as the minimum arm inductance needed to keep arm currents within acceptable limits. Moreover, the influence of each parameter on the fault currents is not readily apparent.

Compared with a numerical model, an analytical model offers mathematical closed-form expressions of fault currents and so gives an in-depth illustrative insight. Analytical models of the MMC under the pole-to-ground fault are given in [11], [12], [13]. The power keeps being transmitted in the first few milliseconds after the pole-to-ground fault. The submodules are not blocked. The two arms of a phase and the AC grounding path in the corresponding phase form a circuit in star connection. Applying the star-delta transformation to the circuit yields an equivalent circuit of constant parameters [11]. While this is applicable to the pole-to-ground fault, such transformation cannot be applied to the MMC under the pole-to-pole fault. The fault current flows through different paths under these two types of DC faults. Instead of flowing through the AC grounding path, the fault current of the MMC under the pole-to-pole fault flows through the arms and the DC link.

After a few milliseconds of the fault occurrence, all IGBTs may be turned off due to overcurrent. Simultaneously with the turning-off actions of the IGBTs, the submodules are blocked. Then, the fault current flows through the freewheeling diodes, as denoted by D_2 of the submodule shown in the upper left part of Fig 1. The MMC may behave like a three-phase halfwave rectifier, and analytical solutions to fault currents are given in [13]. Such analytical solutions cannot be extended to the MMC under pole-to-pole faults. During such faults, large arm currents and low DC-link voltage result in different switching actions of freewheeling diodes in comparison with the MMC under the pole-to-ground fault.

For the MMC under the pole-to-pole fault, most of the analytical models for the fault current calculation are proposed on the premise that the submodules are non-blocked. Such a premise is

reasonable if the arm currents could remain at relatively small values [14]. Analytical models of the MMC with non-blocked submodules are given in [14], [15], [16]. In those models, the ripples of the submodule capacitor voltages are neglected. In fact, the voltage ripple could reach up to 10% of the DC component of the capacitor voltage [17]. Neglecting the capacitor voltage ripples results in inaccurate calculation of the capacitor discharging currents. Shortly after the fault occurrence, all IGBTs may be turned off due to overcurrent caused by capacitor discharging behaviors. For the MMC with all IGBTs in off states, the fault currents flow through the freewheeling diodes. The conducting states of the arms vary due to changing operating states of the freewheeling diodes. The varying conducting states of the arms result in diverse topologies of the converter [18]. Two converter topologies with respectively three and four arms in conducting state are taken into consideration in [14]. Based on observations from reality, with diverse main circuit parameters and operating points, there are more topologies beyond those two considered. A generic analytical model valid for diverse topologies of the MMC under pole-to-pole faults is still missing.

In this work, the events following the pole-to-pole fault occurrence of the MMC based on the half-bridge submodule is categorized into four stages, and the equivalent circuit of each stage is derived. In the analysis, the impacts of the capacitor voltage ripples are taken into consideration. Generic equivalent circuits valid for all four stages are developed, taking into account the conducting states of the circuit breakers, the submodules, and the converter arms. Based on these generic equivalent circuits, the analytical solutions of the fault currents of the AC grid, of the converter arms, and of the DC grid are derived. As an engineering application, the proposed analytical model is applied to the design of the arm inductance and the selection of the circuit breaker interrupting capability. Iterative numerical computations are not involved.

Following this introduction, the mathematical model of the MMC in the steady state is summarized in Section II. In Section III, the events following the pole-to-pole fault occurrence are categorized into four stages, and the equivalent circuit of each stage is derived. Section IV is concerned with the derivation of the analytical solutions of the fault currents and voltages. In Section V, the analytical model is applied to the circuit parameter design and the selection of the circuit breaker interrupting capability. The validation is performed using the CIGRE B4 DC test system in Section VI. Conclusions are drawn in Section VII. Plausible assumptions and modeling details are summarized in the appendix.

II. Review of Basic Operating Principles

The three-phase MMC, as depicted in Fig. 1, is shown to be composed of three legs. Each leg consists of two arms connected in series. An arm contains N identical half-bridge submodules in series connection. Each such submodule consists of two insulated gate bipolar transistors (IGBTs), two diodes, and one capacitor. In each arm, there is one inductor of inductance L_{arm} connected in series with the submodules.

A. Mathematical Model of MMC in Steady State

The voltages generated by the cascade of submodules in the arms of phase a are represented by v_{ua} and v_{la}, where subscripts u and l denote the upper and lower arms. Likewise, the upper and lower arm currents in phase a are denoted by i_{ua} and i_{la}. The AC terminal voltage of the converter and the AC grid current in phase a are respectively denoted by v_{ta} and i_{sa}, while the DC terminal voltage is v_{dc}.

The DC and AC terminal voltages can be obtained by Kirchhoff's voltage law as

$$v_{\text{dc}} = v_{\text{la}} + v_{\text{ua}} - L_{\text{arm}} \frac{\mathrm{d}\left(i_{\text{ua}} + i_{\text{la}}\right)}{\mathrm{d}t} - R_{\text{arm}}\left(i_{\text{ua}} + i_{\text{la}}\right) \tag{1}$$

$$v_{\text{ta}} = \frac{v_{\text{la}} - v_{\text{ua}}}{2} + \frac{L_{\text{arm}}}{2} \frac{\mathrm{d}\left(i_{\text{ua}} - i_{\text{la}}\right)}{\mathrm{d}t} + \frac{R_{\text{arm}}}{2}\left(i_{\text{ua}} - i_{\text{la}}\right). \tag{2}$$

The arm resistance R_{arm} representing the on-state resistance of power electronic switching devices is negligible in normal operation [19]. With respect to (2), it is convenient to define the inner electromotive force e_{sa} generated in the leg of phase a as [20]

$$e_{\text{sa}} = \frac{v_{\text{la}} - v_{\text{ua}}}{2}. \tag{3}$$

To determine the phase angles of sinusoidal quantities, a reference waveform must be chosen:

$$e_{\text{sa}}(t) = \hat{V}_{\text{s}} \cos\left(\omega_{\text{s}} t\right) \tag{4}$$

where ω_{s} is the angular frequency of the AC grid, and $\hat{V}_{\text{s}}$ is the amplitude of the inner electromotive force.

For steady-state analysis, the AC grid current is defined as

$$i_{\text{sa}}(t) = \hat{I}_{\text{s}} \cos\left(\omega_{\text{s}} t - \varphi\right) \tag{5}$$

where $\hat{I}_{\text{s}}$ is the amplitude of the AC grid current, and φ is the phase lag of i_{sa} with respect to e_{sa}. The AC grid current is equally fed into the two arms of one leg under balanced condition. Except for the AC feeding current, the circulating current also exists in each arm [18]. The circulating current flowing in each leg of the converter consists of a DC component and harmonic components [21]. The DC component is one third of the DC link current. The harmonic components of the circulating current are well suppressed in accordance with assumption 1 of Appendix A. Consequently, the upper and lower arm currents can be expressed by the sum of the AC feeding current and the circulating current as

$$i_{\text{ua}}(t) = \frac{1}{2} \hat{I}_{\text{s}} \cos\left(\omega_{\text{s}} t - \varphi\right) + \frac{i_{\text{dc}}}{3} \tag{6a}$$

$$i_{\text{la}}(t) = -\frac{1}{2} \hat{I}_{\text{s}} \cos\left(\omega_{\text{s}} t - \varphi\right) + \frac{i_{\text{dc}}}{3}. \tag{6b}$$

Neglecting R_{arm} and inserting (6) into (1) eliminates i_{la} and i_{ua} from (1), resulting in $v_{\text{dc}} = v_{\text{la}} + v_{\text{ua}}$ in steady-state operation. Combining the obtained equation with (3) and then inserting (4) results in the upper arm voltage v_{ua} and the lower arm voltage v_{la} as

$$v_{\text{ua}}(t) = \frac{v_{\text{dc}}}{2}\left(1 - M \cos\left(\omega_{\text{s}} t\right)\right) \tag{7a}$$

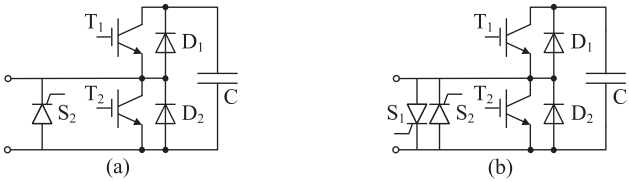

Fig. 2. Structure of half-bridge submodule with bypass switches; (a) single thyristor switch, (b) double thyristor switches.

$$v_{\mathrm{la}}(t) = \frac{v_{\mathrm{dc}}}{2}\left(1 + M\cos\left(\omega_{\mathrm{s}}t\right)\right) \tag{7b}$$

where the modulation index M is given by

$$M = 2\hat{V}_{\mathrm{s}}/v_{\mathrm{dc}}. \tag{8}$$

B. Calculation of Ripple Voltages of Capacitors

As shown in the upper left part of Fig. 1, depending on the switching signal issued by the controller to the submodule, the submodule capacitor is inserted into the arm, or it is bypassed. The inserted capacitors may discharge or be charged according to the arm current polarity. Due to switching actions, the ripple voltages of the capacitors appear at the AC terminal of the submodule. According to [19], taking into consideration N submodules in one arm, the total ripple voltages up to third-order terms respectively for the upper arm and the lower arm are given by (49) and (50) in Appendix B. By summing up the ripple voltages of the upper and lower arms, the total ripple voltage $v_{\mathrm{a,rip}}(t)$ of the leg in phase a is approximated by

$$\begin{aligned} v_{\mathrm{a,rip}}(t) = & -\frac{NM\hat{I}_{\mathrm{s}}}{8\omega_{\mathrm{s}}C}\sin\varphi \\ & +\frac{3NM\hat{I}_{\mathrm{s}}}{16\omega_{\mathrm{s}}C}\sin\left(2\omega_{\mathrm{s}}t-\varphi\right)-\frac{NM^2 i_{\mathrm{dc}}}{12\omega_{\mathrm{s}}C}\sin\left(2\omega_{\mathrm{s}}t\right) \end{aligned} \tag{9}$$

where N is the number of submodules in one arm, and C is the capacitance of the submodule capacitor. The ripple voltages for phases b and c can be obtained in a similar manner. Because of symmetry in the steady state, the ripple voltages of the three phases will be identical apart from phase shifts of 0 rad, $-4\pi/3$ rad, and $4\pi/3$ rad applied to the sinusoidal quantities that are functions of time t in the phases a, b, and c.

C. Half-Bridge Submodule With Bypass Thyristor

Overcurrents have been reported during transient disturbances, such as AC and DC short-circuit faults [17], [18]. To avoid damage on diode D_2, as shown in Fig. 2(a), it is common practice to connect a single thyristor in parallel with the AC port of the submodule [18]. The fault current then flows through thyristor S_2 in parallel with diode D_2. A single thyristor is usually sufficient if the aim is just to protect the diode from overcurrent. Double thyristor switches, as shown in Fig. 2(b), provide a path for both positive and negative arm currents [5]. Thus, the AC current cannot feed into the DC grid thanks to the symmetrical topology of the converter. The impacts of the thyristors on the fault responses are detailed later in Section III-D.

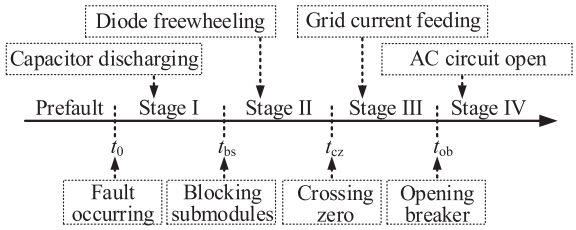

Fig. 3. Definition of four stages of the pole-to-pole fault.

III. Distinctive Stages of Pole-to-Pole Fault and Equivalent Circuits

The analytical modeling of the MMC under the pole-to-pole fault makes use of the proposed equivalent circuits. There are multiple equivalent circuits during the fault stages due to the varying conducting states of the circuit breakers, the submodules, and the converter arms. According to those varying conducting states, the events following the pole-to-pole fault occurrence are categorized into four stages. An overview of the fault stages is given in Section III-A. The transient responses and the equivalent circuit of each stage are detailed in Section III-B. The conducting states of the circuit breakers, the submodules, and the converter arms for the four stages of the fault responses are summarized in Section III-C. In Section III-D, the impacts of the protection scheme using thyristors are discussed.

A. Overview of Fault Scenario and Fault Stages

A pole-to-pole short-circuit fault on the DC link of the MMC is considered. The analysis focuses on the converter based on half-bridge submodules with the basic circuit as shown in the upper left part of Fig. 1. The submodule topology with bypass thyristor switches, as discussed in Section II-C, is considered as a special case. The fault scenario is described as follows. The pole-to-pole short-circuit fault on the DC link occurs at time t_0. Shortly after the fault occurrence, the submodules are blocked at t_{bs} due to overcurrent. The MMC based on half-bridge submodules is unable to extinguish the DC arc by blocking the submodules [22]. Therefore, the AC circuit breakers are opened at t_{ob} so as to isolate the short-circuit fault. The time interval from the time t_{bs} of blocking submodules to the time t_{ob} of opening the circuit breaker is expected to lie in a range of 60 ms to 100 ms [23].

The fault process is decomposed into four stages, as shown in Fig. 3. The stage I, extending from time t_0 of fault occurrence to time t_{bs} of blocking submodules, is the capacitor discharging stage. The stage II is the diode freewheeling stage with the time span from t_{bs} to the time t_{cz} of the first zero-crossing of the arm currents. Spanning from t_{cz} to the time t_{ob} of opening AC circuit breakers, the stage III is defined as the grid current feeding stage. Going from the time t_{ob} to the end, the stage IV is called the AC circuit open stage.

B. Transient Responses and Equivalent Circuits

In what follows, the system behavior and the equivalent circuit of each stage are detailed.

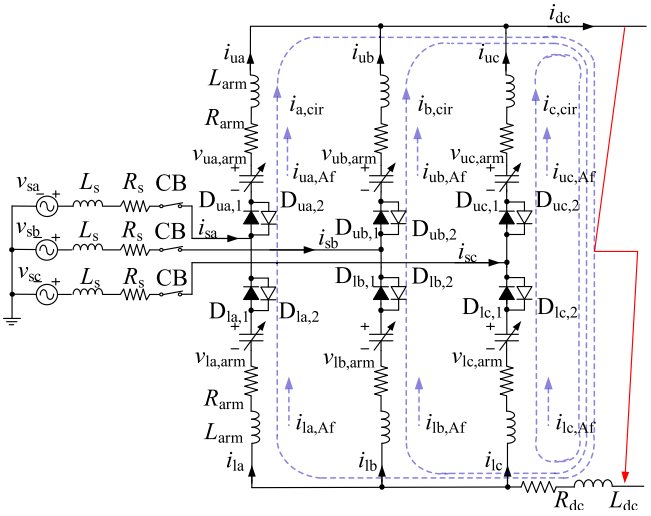

Fig. 4. Equivalent circuit for stage I: capacitor discharging stage.

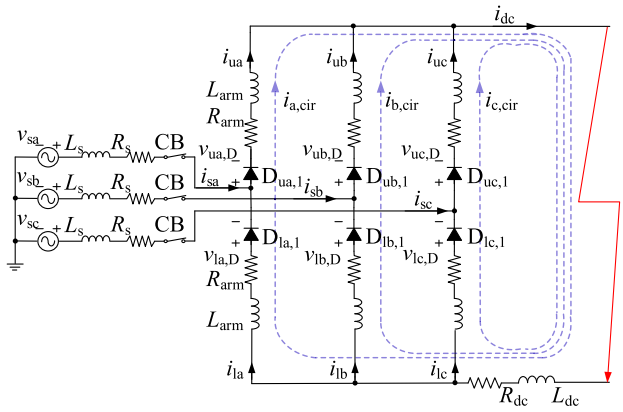

Fig. 5. Equivalent circuit for stage II: diode freewheeling stage.

1) Stage I - Capacitor Discharging Stage: During this stage, the submodules continue to switch as in the prefault operation. The submodule capacitors, as shown in the upper left part of Fig. 1, alternate between inserted and bypassed states. The inserted capacitors discharge through the arms and the DC link due to low voltage at the DC terminal, leading to overcurrent. Despite the discharging behavior, the capacitor voltages may be regarded as constant because of the short duration of the discharging period [15]. Consequently, the topology of the converter is the same as that in the prefault condition.

The equivalent circuit for the stage I is shown in Fig. 4. At the AC terminal of the converter, the AC circuit breakers (CBs) remain closed. In the DC link, R_{dc} and L_{dc} are the resistance and inductance of the cable between the converter DC terminal and the fault location, respectively. In each arm of the converter, there is one resistor of resistance R_{arm}, representing the on-state resistance of the power electronic switching devices in the arm. Anti-parallel equivalent diodes are added to each arm since the arm current can be positive or negative. For the upper arm of phase a, the anti-parallel equivalent diodes are referred to as $\mathrm{D_{ua,1}}$, $\mathrm{D_{ua,2}}$. When the arm current is positive, the upper arm current of phase a flows through $\mathrm{D_{ua,1}}$. Referring to Fig. 1, the positive arm current flows through the $\mathrm{T_1}$ of inserted submodules and through the $\mathrm{D_2}$ of the bypassed submodules. When the arm current is negative, the upper arm current of phase a flows through $\mathrm{D_{ua,2}}$ of the equivalent circuit in Fig. 4. Referring to Fig. 1, the negative arm current flows through the $\mathrm{D_1}$ of inserted submodules and through the $\mathrm{T_2}$ of the bypassed submodules.

A variable capacitor is added to each arm to represent the total inserted capacitors. The voltages of the variable capacitors in the upper and lower arms are denoted by $v_{\mathrm{u}j,\mathrm{arm}}$ and $v_{\mathrm{l}j,\mathrm{arm}}$. Each capacitor voltage is composed of two terms. One term is the voltage $v_{\mathrm{u}j}$ or $v_{\mathrm{l}j}$ representing constant capacitor voltages as given by (7). The other term is the voltage $v_{\mathrm{u}j,\mathrm{rip}}(t)$ or $v_{\mathrm{l}j,\mathrm{rip}}(t)$ caused by ripples of the capacitor voltages, as given by (49) and (50). The composite of those two terms yields the voltages of the variable capacitors in the upper and lower arms:

$$v_{\mathrm{u}j,\mathrm{arm}}(t) = v_{\mathrm{u}j}(t) + v_{\mathrm{u}j,\mathrm{rip}}(t) \tag{10}$$

$$v_{\mathrm{l}j,\mathrm{arm}}(t) = v_{\mathrm{l}j}(t) + v_{\mathrm{l}j,\mathrm{rip}}(t). \tag{11}$$

Referring to (7), (49), and (50), the second-order harmonic components are included in the arm voltages $v_{\mathrm{u}j,\mathrm{arm}}(t)$ and $v_{\mathrm{l}j,\mathrm{arm}}(t)$. The higher-order harmonic components of the arm voltages are neglected in accordance with assumption 2 of Appendix A.

The AC grid operates in the same way as in the prefault time period since the submodules continue to switch as under normal operating conditions. With the AC grid in quasi-steady state, the grid current $i_{\mathrm{s}j}, j \in \{\mathrm{a,b,c}\}$ is the same as that in the prefault condition. The AC grid current is equally fed into the upper and lower arms since the converter topology is symmetrical. Besides the AC feeding currents, the circulating current $i_{j,\mathrm{cir}}, j \in \{\mathrm{a,b,c}\}$ does exist in the arms, as marked by the dashed lines in Fig. 4. The circulating currents flow through the legs and the DC link. Because of the discharging behavior of the inserted capacitors, the circulating currents increase rapidly. Consequently, the arm current is composed of the AC feeding current and the circulating current as

$$i_{\mathrm{u}j}(t) = i_{\mathrm{u}j,\mathrm{Af}}(t) + i_{j,\mathrm{cir}}(t) \tag{12a}$$

$$i_{\mathrm{l}j}(t) = i_{\mathrm{l}j,\mathrm{Af}}(t) + i_{j,\mathrm{cir}}(t) \tag{12b}$$

where $i_{\mathrm{u}j,\mathrm{Af}}(t)$ and $i_{\mathrm{l}j,\mathrm{Af}}(t)$ are the AC feeding currents in the upper and lower arms, and $i_{j,\mathrm{cir}}(t)$ is the respective circulating current. The reference directions of the AC feeding currents are the same as those of the respective circulating current, as marked in Fig. 4. Due to the rapidly increasing circulating currents, the arm currents increase rapidly, too.

2) Stage II - Diode Freewheeling Stage: At the beginning of this stage, all IGBTs of the converter are turned off due to overcurrents in the arms. The arm currents are positive as a consequence of the capacitor discharging currents of stage I. The arm currents are forced to flow through the freewheeling diodes, i.e., the diode $\mathrm{D_2}$ of the submodule, as shown in the upper left part of Fig. 1. Simultaneously with the turning-off actions of the IGBTs, the capacitors are bypassed and stop discharging. The equivalent circuit of this stage is shown in Fig. 5. The

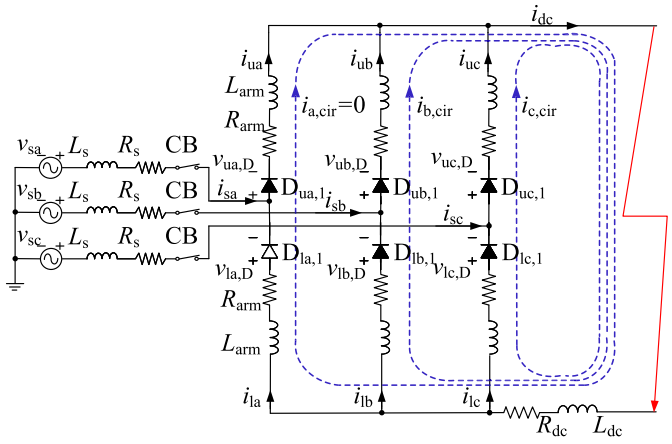

Fig. 6. Equivalent circuit for stage III: grid current feeding stage.

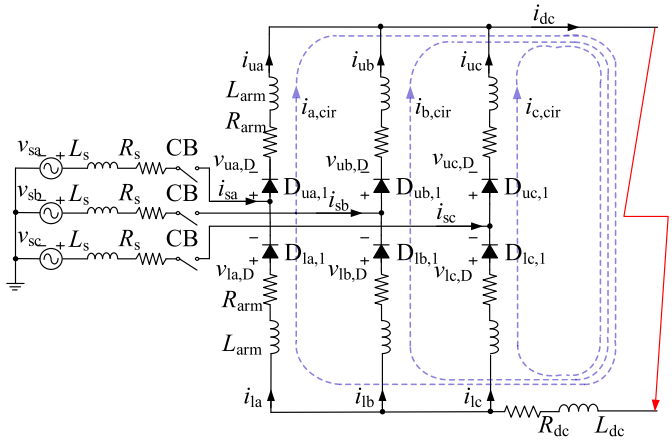

Fig. 7. Equivalent circuit for stage IV: AC circuit open stage.

equivalent diodes $D_{ua,1}$, $D_{ub,1}$, $D_{uc,1}$, $D_{la,1}$, $D_{lb,1}$, and $D_{lc,1}$ in the six arms are in conducting states. The diodes in the arms are unidirectional since the arm currents are positive. Because of the positive arm currents, the equivalent diodes $D_{ua,2}$, $D_{ub,2}$, $D_{uc,2}$, $D_{la,2}$, $D_{lb,2}$, and $D_{lc,2}$ in the equivalent circuit of the stage I in Fig. 4 are absent in the equivalent circuit of the stage II. The forward voltage drops of the equivalent diodes in the upper and lower arms are denoted by $v_{uj,D}$ and $v_{lj,D}$ with $j \in \{a,b,c\}$. In comparison with the equivalent circuit of the stage I in Fig. 4, the variable capacitors are absent in the equivalent circuit of this stage since all capacitors are bypassed.

3) Stage III - Grid Current Feeding Stage: This stage is initiated as soon as one of the six arm currents reaches zero. The corresponding arm gets into a non-conducting state, and the circuit becomes asymmetrical. Due to the resulting asymmetry of the circuit, the AC grid currents begin to feed into the DC grid. The equivalent circuit of this stage is shown in Fig. 6, in which at least one of the six arms is non-conductive. In the illustrated equivalent circuit, the lower arm of phase a is non-conductive, and the equivalent diode $D_{la,1}$ is in off state. The AC grid current i_{sa} flows through the upper arm of phase a, while the circulating current $i_{a,cir}$ of this leg becomes zero. The operating states of the freewheeling diodes vary during this stage. A diode becomes non-conductive when the arm current reaches zero and is forced to be conductive when its forward voltage drop becomes positive.

4) Stage IV - AC Circuit Open Stage: To isolate the DC short-circuit fault, the AC circuit breakers are opened within tens of milliseconds of the fault occurrence [17]. The equivalent circuit of this stage is shown in Fig. 7, in which all six arms are in the conducting state.

The AC grid currents $i_{sj}, j \in \{a,b,c\}$ are forced to be zero since the AC circuit breakers are opened. In the converter arms, the AC feeding currents are absent, while the circulating currents $i_{j,cir}$ continue to flow. The circulating currents decay slowly since the arm resistance R_{arm} and the cable resistance R_{dc} are relatively small, while the arm inductance L_{arm} is relatively large. Thus, it takes a relatively long time for the circulating currents to practically disappear.

TABLE I
OVERVIEW OF STATES OF SWITCHING DEVICES

Stage	Circuit breaker state (ρ_{sa},ρ_{sb},ρ_{sc})	Submodules state (σ_{ea},σ_{eb},σ_{ec})	Arm conducting state (ς_{ua},ς_{ub},ς_{uc},ς_{la},ς_{lb},ς_{lc})
I	(1, 1, 1)	(1, 1, 1)	(1, 1, 1, 1, 1, 1)
II	(1, 1, 1)	(0, 0, 0)	(1, 1, 1, 1, 1, 1)
III	(1, 1, 1)	(0, 0, 0)	Varying
IV	(0, 0, 0)	(0, 0, 0)	(1, 1, 1, 1, 1, 1)

C. Operating States of Switching Devices

The topologies of the equivalent circuits differ among the fault stages. For the purpose of finally deriving a generic equivalent circuit that is valid for the entire transient process, three sets of operating states are defined, as summarized in Table I.

Firstly, the conducting states $(\rho_{sa}, \rho_{sb}, \rho_{sc})$ of the AC circuit breakers in phases $j \in \{a, b, c\}$ are defined as

$$\rho_{sj}(t) = \begin{cases} 1, & \text{circuit breaker closed} \\ 0, & \text{circuit breaker opened.} \end{cases} \tag{13}$$

The circuit breakers remain closed in stages I to III and are open in stage IV.

Secondly, the operating states $(\sigma_{ea}, \sigma_{eb}, \sigma_{ec})$ of the submodules in phases $j \in \{a, b, c\}$ are defined as

$$\sigma_{ej}(t) = \begin{cases} 1, & \text{submodules non-blocked} \\ 0, & \text{submodules blocked.} \end{cases} \tag{14}$$

The submodules are non-blocked in the stage I and are blocked in the stages II to IV. In the non-blocked state, the IGBTs are turned on and off as in the prefault operation. The submodule capacitors, as shown in the upper left part of Fig. 1, alternate between inserted and bypassed states. In the blocked state, all IGBTs of submodules are in off states, and submodule capacitors are bypassed. The arm currents flow through the freewheeling diodes, as depicted by D_2 in the upper left part of Fig. 1.

Thirdly, the conducting states $(\varsigma_{ua}, \varsigma_{ub}, \varsigma_{uc}, \varsigma_{la}, \varsigma_{lb}, \varsigma_{lc})$ of the converter arms are defined as

$$\varsigma_{uj}(t) = \begin{cases} 1, & \text{upper arm conductive} \\ 0, & \text{upper arm non-conductive,} \end{cases} \tag{15}$$

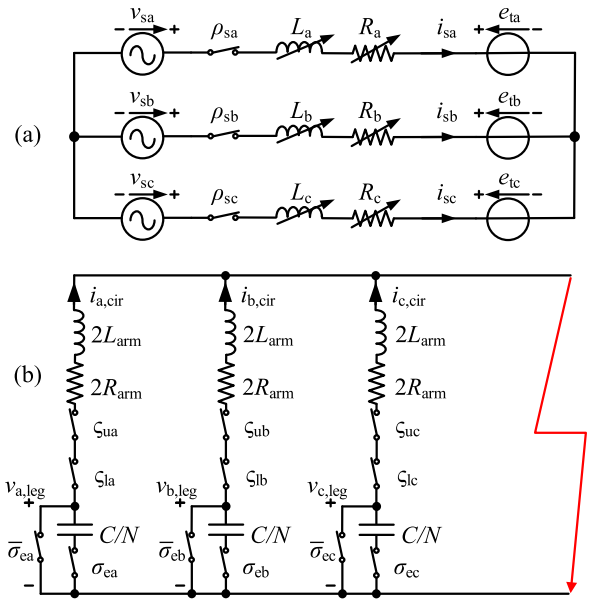

Fig. 8. Equivalent circuits for calculation of (a) AC grid currents and (b) circulating currents.

$$\varsigma_{lj}(t) = \begin{cases} 1, & \text{lower arm conductive} \\ 0, & \text{lower arm non-conductive.} \end{cases} \tag{16}$$

The converter arms are conductive in stage I. The arm currents can be positive or negative. The bidirectional arm currents flow through the anti-parallel equivalent diodes $\mathrm{D}_{uj,1}$, $\mathrm{D}_{uj,2}$ of the upper arms and $\mathrm{D}_{lj,1}$, $\mathrm{D}_{lj,2}$ of the lower arms in Fig. 4. In stages II and IV, the converter arms are also conductive. The arm currents are positive and flow through the freewheeling diodes, as shown by D_2 in the upper left part of Fig. 1. As shown in Figs. 5 to 7, the unidirectional arm currents flow through the equivalent diodes $\mathrm{D}_{uj,1}$ and $\mathrm{D}_{lj,1}$. In stage III, the arm conducting states vary. The arm currents could be positive or zero, as discussed in Section III-B3. In the illustrated equivalent circuit in Fig. 6, the lower arm current of phase a is zero, and the equivalent diode $\mathrm{D}_{la,1}$ is in off state.

D. Impacts of Bypassing Thyristors on Fault Stages

For a submodule with a single thyristor, as depicted in Fig. 2(a), the thyristor S_2 operates in parallel with the diode D_2. The thyristor S_2 is kept in the off state in the prefault condition and stage I, and it is triggered on as soon as the fault is detected. The transient responses to the pole-to-pole fault are the same as that of the MMC utilizing submodules without bypass thyristors. The corresponding equivalent circuits for the four stages of the transient responses are given as in Figs. 4 to 7. The arm resistance R_{arm} in the stages II, III, and IV includes the on-state resistance of the freewheeling diodes and the thyristors of one arm with each diode D_2 and thyristor S_2 of one submodule illustrated in the upper left part of Fig. 1.

For the submodule with double thyristors, as depicted in Fig. 2(b), the thyristors are kept in the off states in the prefault condition and in the stage I. Both thyristors are switched on as soon as the fault is detected. With those bidirectional switches, all arms are conductive throughout the fault period. Consequently, the transient responses stay within the stages I and II.

In order to develop a generic model of the MMC under the pole-to-pole fault, the submodule without thyristors as shown in the upper left part of Fig. 1 is considered hereafter. From the so obtained generic model, MMCs with thyristors in the submodules are obtained as special cases.

IV. Analytical Modeling of Fault Currents of MMC Under Pole-to-Pole Fault

To address the varying topologies of the converter caused by changing conducting states of switching devices, two generic equivalent circuits respectively for the calculations of the AC grid currents and the circulating currents are developed. Through these two generic equivalent circuits, the analytical expressions of the AC grid currents, the arm currents, and the DC grid current are derived.

A. Generic Equivalent Circuits for Severe Pole-to-Pole Fault

A pole-to-pole fault could happen at any location on the DC link. For applications such as the parameter design of the converter and protection, it is of interest to focus on the most severe situation [24]. As such, a pole-to-pole fault is applied close to the converter in accordance with assumption 3 of Appendix A. Thus, the resistance R_{dc} and the inductance L_{dc} in the DC link are set to zero. The bypassing thyristors of the submodules illustrated in Fig. 2 are not considered yet as those lead to special cases as discussed in Section III-D.

The topologies of the equivalent circuits of the fault stages vary because of the changing conducting states of the switching devices, as depicted in Figs. 4 to 7 and given in Table I. Referring to assumption 4 of Appendix A, for any topology as defined by the states of the switching devices, the corresponding equivalent circuit is linear. In order to develop the generic equivalent circuits, considerations start with the composition of the arm currents. As discussed in (12) of Section III-B, the arm currents are composed of the AC feeding currents and the circulating currents. The AC feeding currents are attributed to the AC grid currents, while the circulating currents only flow through the legs and the DC link. Since the circulating currents do not flow into the AC grid, the AC grid currents and the circulating currents are decoupled.

Depending on the equivalent circuits of Figs. 4 to 7, taking into account the conducting states of the switching devices listed in Table I, two equivalent circuits respectively for the calculations of the AC grid currents and the circulating currents are developed and given in Fig. 8. The equivalent circuit for the calculation of the AC grid currents is shown in Fig. 8(a). The AC grid voltages are denoted by v_{sa}, v_{sb}, and v_{sc}. Binary variables ρ_{sa}, ρ_{sb}, and ρ_{sc} denote the states of the ideal AC circuit breakers, as given by (13). The equivalent resistance R_j and inductance L_j of phase $j \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ cover the resistors and inductors of the AC grid and the converter arms. The upper and lower arms of one leg operate in parallel if both arms are conductive, resulting in $R_j = R_{\mathrm{s}} + R_{\mathrm{arm}}/2$ and $L_j = L_{\mathrm{s}} + L_{\mathrm{arm}}/2$. If one of the upper and

lower arms of one leg is non-conductive, the AC grid current of the corresponding phase only flows through the conductive arm, resulting in $R_j = R_\mathrm{s} + R_\mathrm{arm}$ and $L_j = L_\mathrm{s} + L_\mathrm{arm}$. Taking into account the above mentioned arm conducting states, the resistance R_j and the inductance L_j of the phase $j \in \{\mathrm{a, b, c}\}$ are defined as

$$R_j = R_\mathrm{s} + \frac{1}{\varsigma_{\mathrm{u}j} + \varsigma_{\mathrm{l}j}} R_\mathrm{arm} \tag{17}$$

$$L_j = L_\mathrm{s} + \frac{1}{\varsigma_{\mathrm{u}j} + \varsigma_{\mathrm{l}j}} L_\mathrm{arm} \tag{18}$$

where $\varsigma_{\mathrm{u}j}$ and $\varsigma_{\mathrm{l}j}$ represent the arm conducting states, as given in (15) and (16).

The voltage sources e_ta, e_tb, and e_tc represent the converter inner electromotive forces obtained by the voltages of the capacitors inserted in the arms. During the stage I, the capacitors continue to switch as in the prefault operation, as shown by the variable capacitors in Fig. 4. Thus, the AC grid operates in quasi-steady state, and the inner electromotive force is given by $e_{\mathrm{s}j}$ with $j \in \{\mathrm{a, b, c}\}$, as shown in (4). During the stages II to IV, the capacitors are bypassed since the submodules are blocked, resulting in the absence of $e_{\mathrm{s}j}$ in the equivalent circuit. Thus, the voltage source $e_{\mathrm{t}j}$ is defined by weighting $e_{\mathrm{s}j}$ by the operating state $\sigma_{\mathrm{e}j}$ of the submodules as:

$$e_{\mathrm{t}j} = \sigma_{\mathrm{e}j} e_{\mathrm{s}j} \tag{19}$$

where $\sigma_{\mathrm{e}j}$ is equal to 0 or 1 as given by (14).

The equivalent circuit for the calculation of the circulating current $i_{j,\mathrm{cir}}$ of phase $j \in \{\mathrm{a, b, c}\}$ is shown in Fig. 8(b). The circulating current flows through the leg and the DC link. Considering upper and lower arms of one leg, the equivalent resistance and the equivalent inductance of the leg are given by $2R_\mathrm{arm}$ and $2L_\mathrm{arm}$. In each leg, the ideal switches $\varsigma_{\mathrm{u}j}$ and $\varsigma_{\mathrm{l}j}$ with $j \in \{\mathrm{a, b, c}\}$, as given by (15) and (16), represent the arm conducting states. The binary variable $\sigma_{\mathrm{e}j}$ gives the state of submodules of phase $j \in \{\mathrm{a,b,c}\}$, as given by (14). The binary variable $\bar{\sigma}_{\mathrm{e}j}$ denotes the negation logic of $\sigma_{\mathrm{e}j}$. According to (14), $\bar{\sigma}_{\mathrm{e}j} = 0$ when the submodules are non-blocked, and $\bar{\sigma}_{\mathrm{e}j} = 1$ when the submodules are blocked. The binary variables $\varsigma_{\mathrm{u}j}$, $\varsigma_{\mathrm{l}j}$, and $\sigma_{\mathrm{e}j}$ in the four stages of the DC fault are given in Table I. In stage I, all these binary values are equal to 1. With each submodule having a capacitor of capacitance C, the equivalent capacitance of one leg is given by C/N since N submodules are inserted within one leg [25]. The voltage across the ideal switch $\sigma_{\mathrm{e}j}$ with $j \in \{\mathrm{a, b, c}\}$ and the equivalent capacitance C/N is given by $v_{j,\mathrm{leg}}$. In the stages II to IV, the binary variable $\sigma_{\mathrm{e}j}$ is equal to 0. The equivalent capacitance C/N is bypassed since the submodules are blocked. In stage III, the conducting states of the ideal switches $\varsigma_{\mathrm{u}j}$ and $\varsigma_{\mathrm{l}j}$ are changing since the arm conducting states are varying, as discussed in Section III-B3.

The voltage $v_{j,\mathrm{leg}}$ in Fig. 8(b) represents the total voltage across the inserted capacitors of one leg of phase $j \in \{\mathrm{a, b, c}\}$. For the convenience of later calculating the circulating current $i_{j,\mathrm{cir}}$, the initial values of $v_{j,\mathrm{leg}}$ at the beginning of each fault stage are to be formulated. The total voltages of the inserted capacitors respectively in the upper and lower arms at time t_0 of fault occurrence are given by $v_{\mathrm{u}j,\mathrm{arm}}(t_0)$ and $v_{\mathrm{l}j,\mathrm{arm}}(t_0)$ in (10) and (11). The ripple components $v_{\mathrm{u}j,\mathrm{rip}}(t)$ and $v_{\mathrm{l}j,\mathrm{rip}}(t)$ of $v_{\mathrm{u}j,\mathrm{arm}}(t)$ and $v_{\mathrm{l}j,\mathrm{arm}}(t)$ at the beginning of the stage I are considered since they are to affect the capacitor discharging currents. The voltage $v_{j,\mathrm{leg}}(t_0)$ of one leg is then obtained by summing up the upper and lower arm voltages at the time t_0 of the fault occurrence, that is $v_{\mathrm{u}j,\mathrm{arm}}(t_0) + v_{\mathrm{l}j,\mathrm{arm}}(t_0)$. During the stages II to IV, the capacitors are bypassed since all IGBTs are turned off, resulting in zero initial and steady-state values of $v_{j,\mathrm{leg}}$ in each stage. Consequently, the voltage $v_{j,\mathrm{leg}}$ at the beginning of each stage is obtained as

$$v_{j,\mathrm{leg}}(0_+) = \sigma_{\mathrm{e}j}\left(v_{\mathrm{u}j,\mathrm{arm}}(t_0) + v_{\mathrm{l}j,\mathrm{arm}}(t_0)\right) \tag{20}$$

where $\sigma_{\mathrm{e}j}$ is the representation of the state of the submodules of phase $j \in \{\mathrm{a, b, c}\}$ according to Table I, and 0_+ denotes the time instant of the beginning of a stage. Inserting (7) and (9) into (10) and (11), and further inserting the obtained result into (20) yields the voltage $v_{\mathrm{a,leg}}$ at the beginning of each stage for the leg a as:

$$\begin{aligned} v_{\mathrm{a,leg}}(0_+) &= \sigma_{\mathrm{ea}} v_{\mathrm{dc,pre}} - \sigma_{\mathrm{ea}} \frac{NM\hat{I}_\mathrm{s}}{8\omega_\mathrm{s} C}\sin\varphi \\ &+\sigma_{\mathrm{ea}}\left(\frac{3NM\hat{I}_\mathrm{s}}{16\omega_\mathrm{s} C}\sin(2\omega_\mathrm{s} t_0 - \varphi) - \frac{NM^2 i_{\mathrm{dc,pre}}}{12\omega_\mathrm{s} C}\sin(2\omega_\mathrm{s} t_0)\right) \end{aligned} \tag{21}$$

where $v_{\mathrm{dc,pre}}$ and $i_{\mathrm{dc,pre}}$ are the DC voltage and current at the prefault operation. Taking into consideration the phase shifts of 0 rad, $-4\pi/3$ rad, and $4\pi/3$ rad in the phases a, b, and c of the ripple voltages, the voltages $v_{\mathrm{b,leg}}(0_+)$ and $v_{\mathrm{c,leg}}(0_+)$ for the legs b and c can be obtained similarly.

B. Analytical Modeling of AC Grid Currents

The analytical modeling of the AC grid currents is to only rely on the equivalent circuit of Fig. 8(a). The equivalent circuit of Fig. 8(b) for the circulating currents is not involved since the AC grid currents and the circulating currents are decoupled. Applying Kirchhoff's voltage law to the equivalent circuit yields

$$-v_\mathrm{sa} + L_\mathrm{a}\frac{\mathrm{d}i_\mathrm{sa}}{\mathrm{d}t} + R_\mathrm{a} i_\mathrm{sa} + e_\mathrm{ta} - e_\mathrm{tb} - L_\mathrm{b}\frac{\mathrm{d}i_\mathrm{sb}}{\mathrm{d}t} - R_\mathrm{b} i_\mathrm{sb} + v_\mathrm{sb} = 0 \tag{22}$$

$$-v_\mathrm{sa} + L_\mathrm{a}\frac{\mathrm{d}i_\mathrm{sa}}{\mathrm{d}t} + R_\mathrm{a} i_\mathrm{sa} + e_\mathrm{ta} - e_\mathrm{tc} - L_\mathrm{c}\frac{\mathrm{d}i_\mathrm{sc}}{\mathrm{d}t} - R_\mathrm{c} i_\mathrm{sc} + v_\mathrm{sc} = 0. \tag{23}$$

Insertion of $i_\mathrm{sc} = -i_\mathrm{sa} - i_\mathrm{sb}$, $v_\mathrm{sc} = -v_\mathrm{sa} - v_\mathrm{sb}$, and $e_\mathrm{tc} = -e_\mathrm{ta} - e_\mathrm{tb}$ into (23) eliminates i_sc, v_sc, and e_tc. The AC grid currents i_sa and i_sb are independent state variables, yielding the state vector $\boldsymbol{i} = [i_\mathrm{sa}\ i_\mathrm{sb}]^\mathrm{T}$. The input vector is given by $\boldsymbol{v} = [v_\mathrm{sa} - e_\mathrm{ta}\ v_\mathrm{sb} - e_\mathrm{tb}]^\mathrm{T}$. Thus, the differential equations (22) and (23) are written in state-space form as

$$\dot{\boldsymbol{i}} = \boldsymbol{A}\boldsymbol{i} + \boldsymbol{B}\boldsymbol{v} \tag{24}$$

with the state matrix $\boldsymbol{A}$ and input matrix $\boldsymbol{B}$ given by

$$\boldsymbol{A} = \frac{1}{L_\mathrm{a}L_\mathrm{b} + L_\mathrm{b}L_\mathrm{c} + L_\mathrm{c}L_\mathrm{a}} \cdot \begin{bmatrix} -(R_\mathrm{a}L_\mathrm{b} + R_\mathrm{c}L_\mathrm{b} + R_\mathrm{a}L_\mathrm{c}) & R_\mathrm{b}L_\mathrm{c} - R_\mathrm{c}L_\mathrm{b} \\ R_\mathrm{a}L_\mathrm{c} - R_\mathrm{c}L_\mathrm{a} & -(R_\mathrm{b}L_\mathrm{a} + R_\mathrm{b}L_\mathrm{c} + R_\mathrm{c}L_\mathrm{a}) \end{bmatrix} \tag{25}$$

$$\boldsymbol{B} = \frac{1}{L_\mathrm{a}L_\mathrm{b} + L_\mathrm{b}L_\mathrm{c} + L_\mathrm{c}L_\mathrm{a}} \cdot \begin{bmatrix} 2L_\mathrm{b} + L_\mathrm{c} & L_\mathrm{b} - L_\mathrm{c} \\ L_\mathrm{a} - L_\mathrm{c} & 2L_\mathrm{a} + L_\mathrm{c} \end{bmatrix}. \tag{26}$$

Applying the Laplace Transform to (24) yields

$$\boldsymbol{i}(s) = (s\mathbf{E} - \boldsymbol{A})^{-1} (\boldsymbol{i}(0_+) + \boldsymbol{B}\boldsymbol{v}(s)) \tag{27}$$

with

$$(s\mathbf{E} - \boldsymbol{A})^{-1} = \frac{\mathrm{adj}\,(s\mathbf{E} - \boldsymbol{A})}{(s - a_{11})(s - a_{22}) - a_{12}a_{21}} \tag{28}$$

where $\boldsymbol{i}(0_+)$ is the initial value of the state vector; $\mathbf{E}$ is the identity matrix; adj$(s\mathbf{E} - \boldsymbol{A})$ is the adjugate matrix; a_{11}, a_{12}, a_{21}, and a_{22} are the elements of the state matrix $\boldsymbol{A}$.

The voltage sources v_sa, v_sb, e_ta and e_tb in the input vector $\boldsymbol{v}$ are sinusoidal quantities of angular frequency ω_s. Inserting (28) into (27) and further multiplying the numerator and denominator by $s^2 + \omega_\mathrm{s}^2$ yields

$$\boldsymbol{i}(s) = \frac{\mathrm{adj}\,(s\mathbf{E} - \boldsymbol{A})(\boldsymbol{i}(0_+) + \boldsymbol{B}\boldsymbol{v}(s))\left(s^2 + \omega_\mathrm{s}^2\right)}{((s - a_{11})(s - a_{22}) - a_{12}a_{21})(s^2 + \omega_\mathrm{s}^2)}. \tag{29}$$

Solving $((s - a_{11})(s - a_{22}) - a_{12}a_{21})(s^2 + \omega_\mathrm{s}^2) = 0$ gives

$$\begin{aligned} &s_1 = \mathrm{j}\omega_\mathrm{s};\ s_2 = -\mathrm{j}\omega_\mathrm{s};\ D = (a_{11} - a_{22})^2 + 4a_{12}a_{21}; \\ &s_3 = \frac{a_{11} + a_{22} + \sqrt{D}}{2};\quad s_4 = \frac{a_{11} + a_{22} - \sqrt{D}}{2} \end{aligned} \tag{30}$$

where j is the imaginary unit, D could be positive or zero for the diverse topologies of the converter during the fault. When the circuit is asymmetrical, insertion of (17) and (18) into a_{11}, a_{12}, a_{21}, a_{22} of the elements of the state matrix $\boldsymbol{A}$ results in $D = (R_\mathrm{s}L_\mathrm{arm} - R_\mathrm{arm}L_\mathrm{s})^2$. When the circuit is symmetrical, $a_{11} = a_{22}$, $a_{12} = 0$, $a_{21} = 0$, resulting in $D = 0$. The inverse Laplace Transform of (29) is performed for these two cases, respectively.

In the case of $D > 0$, the four roots s_1, s_2, s_3, and s_4 in (30) are different from each other. Application of the inverse Laplace Transform gives the AC grid currents

$$\begin{aligned} \boldsymbol{i}(t) = {} & (\boldsymbol{C}_1 + \boldsymbol{C}_2)\cos(\omega_\mathrm{s}t) + \mathrm{j}\,(\boldsymbol{C}_1 - \boldsymbol{C}_2)\sin(\omega_\mathrm{s}t) \\ & + \boldsymbol{C}_3\mathrm{e}^{s_3t} + \boldsymbol{C}_4\mathrm{e}^{s_4t} \end{aligned} \tag{31}$$

where the coefficients $\boldsymbol{C}_m = \lim_{s\to s_m}(s - s_m)\boldsymbol{i}(s)$, $m = 1, 2, 3, 4$; $(\boldsymbol{C}_1 - \boldsymbol{C}_2)$ gives an imaginary value. In the case of $D = 0$, s_3 and s_4 in (30) are the same. Applying the inverse Laplace Transform to (29) yields the AC grid current

$$\begin{aligned} \boldsymbol{i}(t) = {} & (\boldsymbol{C}_1 + \boldsymbol{C}_2)\cos(\omega_\mathrm{s}t) + \mathrm{j}\,(\boldsymbol{C}_1 - \boldsymbol{C}_2)\sin(\omega_\mathrm{s}t) \\ & + (\boldsymbol{C}_\mathrm{rp3} + \boldsymbol{C}_\mathrm{rp4}t)\,\mathrm{e}^{s_3t} \end{aligned} \tag{32}$$

where the coefficients $\boldsymbol{C}_1$ and $\boldsymbol{C}_2$ correspond to those of (31), $\boldsymbol{C}_\mathrm{rp3} = \lim_{s\to s_3}\frac{\mathrm{d}}{\mathrm{d}t}((s - s_3)^2\boldsymbol{i}(s))$, $\boldsymbol{C}_\mathrm{rp4} = \lim_{s\to s_3}(s - s_3)^2\boldsymbol{i}(s)$. The AC grid currents in (31) and (32) are shown to be composed of the steady-state and the transient components. The steady-state components are sinusoidal quantities, while the transient components decay exponentially.

C. Analytical Modeling of Arm Currents

In accordance with (12), the arm currents are composed of the AC feeding currents $i_{\mathrm{u}j,\mathrm{Af}}(t)$, $i_{\mathrm{l}j,\mathrm{Af}}(t)$ and the circulating currents $i_{j,\mathrm{cir}}(t)$. The AC feeding currents $i_{\mathrm{u}j,\mathrm{Af}}(t)$ and $i_{\mathrm{l}j,\mathrm{Af}}(t)$ in the upper and lower arms are attributed to the AC grid currents, taking into account the arm conducting states. When both the upper and lower arms of one leg are conductive, the AC grid current is equally split between the two arms. When one of the upper and lower arms of a leg is non-conductive, the AC grid current flows through the conductive arm. Based on this observation, the AC feeding currents $i_{\mathrm{u}j,\mathrm{Af}}(t)$ and $i_{\mathrm{l}j,\mathrm{Af}}(t)$ in the upper and lower arms of leg $j \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ are calculated as

$$i_{\mathrm{u}j,\mathrm{Af}}(t) = \frac{\varsigma_{\mathrm{u}j}}{\varsigma_{\mathrm{u}j} + \varsigma_{\mathrm{l}j}} i_{\mathrm{s}j}(t) \tag{33a}$$

$$i_{\mathrm{l}j,\mathrm{Af}}(t) = \frac{-\varsigma_{\mathrm{l}j}}{\varsigma_{\mathrm{u}j} + \varsigma_{\mathrm{l}j}} i_{\mathrm{s}j}(t) \tag{33b}$$

where the AC grid current $i_{\mathrm{s}j}$ is given by (31) and (32) involving i_sa and i_sb, while i_sc is obtained as $(-i_\mathrm{sa} - i_\mathrm{sb})$; $\varsigma_{\mathrm{u}j}$ and $\varsigma_{\mathrm{l}j}$ are the representations of the arm conducting states, as given by (15).

Another contribution to the arm current is given by the circulating current $i_{j,\mathrm{cir}}(t)$, which flows through the leg and the DC link, as shown in Fig. 8(b). Each leg is composed of the inductance $2L_\mathrm{arm}$, the resistance $2R_\mathrm{arm}$, the equivalent capacitance C/N, and the ideal switches representing operating states of the switching devices. According to the equivalent circuit, the dynamic response of the circulating current $i_{j,\mathrm{cir}}$ is described by

$$2L_\mathrm{arm}\frac{\mathrm{d}^2 i_{j,\mathrm{cir}}}{\mathrm{d}t^2} + 2R_\mathrm{arm}\frac{\mathrm{d}i_{j,\mathrm{cir}}}{\mathrm{d}t} + \frac{N\sigma_{\mathrm{e}j}}{C} i_{j,\mathrm{cir}} = 0 \tag{34}$$

where N is the number of submodules per arm, C is the capacitance of each submodule; $\sigma_{\mathrm{e}j}$ denotes the operating states of the submodules, as given by (14). Solving (34), the circulating current $i_{j,\mathrm{cir}}(t)$ in the leg $j \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ is expressed by

$$\begin{aligned} i_{j,\mathrm{cir}}(t) = {} & \left(\frac{i_{j,\mathrm{cir}}(0_+)}{2} + \frac{v_{j,\mathrm{leg}}(0_+) - R_\mathrm{arm}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_\mathrm{arm}^2 - 2L_\mathrm{arm}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_1t} \\ & + \left(\frac{i_{j,\mathrm{cir}}(0_+)}{2} - \frac{v_{j,\mathrm{leg}}(0_+) - R_\mathrm{arm}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_\mathrm{arm}^2 - 2L_\mathrm{arm}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_2t} \end{aligned} \tag{35}$$

with

$$p_1 = \frac{-R_\mathrm{arm} + \sqrt{R_\mathrm{arm}^2 - 2L_\mathrm{arm}N\sigma_{\mathrm{e}j}/C}}{2L_\mathrm{arm}} \tag{36}$$

$$p_2 = \frac{-R_\mathrm{arm} - \sqrt{R_\mathrm{arm}^2 - 2L_\mathrm{arm}N\sigma_{\mathrm{e}j}/C}}{2L_\mathrm{arm}} \tag{37}$$

where 0_+ denotes the initial value at the beginning of the present fault stage. The initial value $v_{j,\mathrm{leg}}(0_+)$ is given by (20) and (21). Details on the formulation of the initial value of the circulating current $i_{j,\mathrm{cir}}(0_+)$ are formulated in Appendix C.

Referring to (12), the combination of (33) and (35) yields the upper and lower arm currents as

$$i_{\mathrm{u}j}(t)=\left(\frac{i_{j,\mathrm{cir}}(0_+)}{2}+\frac{v_{j,\mathrm{leg}}(0_+)-R_{\mathrm{arm}}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_{\mathrm{arm}}^2-2L_{\mathrm{arm}}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_1 t}+\left(\frac{i_{j,\mathrm{cir}}(0_+)}{2}-\frac{v_{j,\mathrm{leg}}(0_+)-R_{\mathrm{arm}}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_{\mathrm{arm}}^2-2L_{\mathrm{arm}}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_2 t}+\frac{\varsigma_{\mathrm{u}j}i_{\mathrm{s}j}(t)}{\varsigma_{\mathrm{u}j}+\varsigma_{\mathrm{l}j}} \tag{38a}$$

$$i_{\mathrm{l}j}(t)=\left(\frac{i_{j,\mathrm{cir}}(0_+)}{2}+\frac{v_{j,\mathrm{leg}}(0_+)-R_{\mathrm{arm}}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_{\mathrm{arm}}^2-2L_{\mathrm{arm}}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_1 t}+\left(\frac{i_{j,\mathrm{cir}}(0_+)}{2}-\frac{v_{j,\mathrm{leg}}(0_+)-R_{\mathrm{arm}}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_{\mathrm{arm}}^2-2L_{\mathrm{arm}}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_2 t}-\frac{\varsigma_{\mathrm{l}j}i_{\mathrm{s}j}(t)}{\varsigma_{\mathrm{u}j}+\varsigma_{\mathrm{l}j}} \tag{38b}$$

with $v_{j,\mathrm{leg}}$ given by (20) and (21); $i_{\mathrm{s}j}(t)$ is given by (31) and (32); and $i_{j,\mathrm{cir}}(0_+)$ is given by (51). The expressions of the arm currents are shown to be dependent on the main circuit parameters and the arm conducting states. The arm conducting states of both the previous and present fault stages are taken into consideration in the calculation of $i_{j,\mathrm{cir}}(0_+)$ in Appendix C.

D. Analytical Modeling of DC Grid Current

The DC grid current $i_{\mathrm{dc}}(t)$ is calculated by summing up the upper arm currents of each phase:

$$i_{\mathrm{dc}}(t)=\sum_{j\in\{\mathrm{a,b,c}\}}\left(\frac{i_{j,\mathrm{cir}}(0_+)}{2}+\frac{v_{j,\mathrm{leg}}(0_+)-R_{\mathrm{arm}}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_{\mathrm{arm}}^2-2L_{\mathrm{arm}}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_1 t}+\sum_{j\in\{\mathrm{a,b,c}\}}\left(\frac{i_{j,\mathrm{cir}}(0_+)}{2}-\frac{v_{j,\mathrm{leg}}(0_+)-R_{\mathrm{arm}}i_{j,\mathrm{cir}}(0_+)}{2\sqrt{R_{\mathrm{arm}}^2-2L_{\mathrm{arm}}N\sigma_{\mathrm{e}j}/C}}\right)\mathrm{e}^{p_2 t}+\sum_{j\in\{\mathrm{a,b,c}\}}\frac{\varsigma_{\mathrm{u}j}}{\varsigma_{\mathrm{u}j}+\varsigma_{\mathrm{l}j}}i_{\mathrm{s}j}(t). \tag{39}$$

Also, the DC grid current is seen to be composed of the AC feeding currents and the circulating currents. The sum of the AC feeding currents is non-zero only in the stage III due to the asymmetrical behavior of the converter, in which at least one arm is in non-conducting state. The circulating currents increase in stage I because of the discharging behavior of the inserted capacitors, and they decrease in the stages II to IV since the capacitors are being bypassed.

V. Parameter Design of Arm Inductor and Selection of Circuit Breaker Interrupting Capability

For a secure operation of the power system, the overload capability of the power electronic switching devices is an important parameter [7]. Furthermore, it must be possible to isolate a fault by opening the circuit breakers in order not to significantly disturb the healthy parts of the system [15]. With regard to those requirements, the parameter design of the arm inductor is considered in Section V-A. Section V-B is concerned with the determination of the circuit breaker interrupting capability.

A. Parameter Design of Arm Inductor

The arm inductor is known as one of the most critical parts of MMC converters, and it plays a dominant role in converter operation [26]. There are various principles of designing arm inductance based on different criteria, such as current ripple, capacitor energy variation, and short-circuit current. Taking into consideration the MMC under the pole-to-pole fault, the converter arms may suffer from overcurrent due to the capacitor discharging in stage I, as discussed in Section III-B1. The arm inductors limit the rise of fault currents involved. One principle of the arm inductance selection is to limit the maximum arm current within a preset critical value at time of blocking submodules at the end of stage I. To calculate the maximum arm current, a common practice is to employ an equivalent circuit consisting of DC voltage sources, arm inductors, and the DC-link fault path. Such an equivalent circuit neglects the AC feeding currents in the arms and the ripple voltages of the capacitors. These neglected factors are carefully considered in the proposed analytical model of the MMC under the pole-to-pole fault, resulting in better accuracy of the maximum arm current calculation.

For the analysis in (12) and (38), the maximum values of AC feeding currents and circulating currents at the time t_{bs} of blocking submodules are defined as $i_{\mathrm{Af,bs}}$ and $i_{\mathrm{cir,bs}}$ hereafter. Taking into account these maximum values, the maximum arm current $i_{\mathrm{arm,bs}}$ at t_{bs} is formulated as:

$$i_{\mathrm{arm,bs}}=i_{\mathrm{Af,bs}}+i_{\mathrm{cir,bs}}. \tag{40}$$

For the calculation of the maximum AC feeding current $i_{\mathrm{Af,bs}}$, (33) is useful. Depending on the arm conducting states, the AC feeding current is one half of the AC grid current in the stage I. Thus, the maximum AC feeding current $i_{\mathrm{Af,bs}}$ is obtained as

$$i_{\mathrm{Af,bs}}=\hat{I}_{\mathrm{s}}/2 \tag{41}$$

where $\hat{I}_{\mathrm{s}}$ is the amplitude of the AC grid current, as given by (5).

Referring to Fig. 8(b), the circulating current at the time t_{bs} of blocking submodules is calculated with (35). The submodules are blocked shortly after the occurrence of the pole-to-pole short-circuit fault in practical application [17]. The voltage of the equivalent capacitance could so assumed to be constant, as given in assumption 5 of Appendix A. As such, the circulating current flows through the constant DC voltage source $v_{j,\mathrm{leg}}$, the inductance $2L_{\mathrm{arm}}$ and the resistance $2R_{\mathrm{arm}}$. The circulating current $i_{j,\mathrm{cir}}(t_{\mathrm{bs}})$ at the time t_{bs} of blocking submodules is obtained as

$$i_{j,\mathrm{cir}}\left(t_{\mathrm{bs}}\right)=\left(\frac{i_{\mathrm{dc,pre}}}{3}-\frac{v_{j,\mathrm{leg}}}{2R_{\mathrm{arm}}}\right)\mathrm{e}^{-\frac{R_{\mathrm{arm}}}{L_{\mathrm{arm}}}t_{\mathrm{bs}}}+\frac{v_{j,\mathrm{leg}}}{2R_{\mathrm{arm}}}. \tag{42}$$

Focusing on the most severe condition, the maximum value of $v_{j,\mathrm{leg}}$ in (21) at the time t_{bs} of blocking submodules with random time t_0 of the fault occurrence is defined as $v_{\mathrm{leg,bs}}$. According to the details in Appendix D, the maximum value $v_{\mathrm{leg,bs}}$ is expressed

by

$$v_{\text{leg,bs}} = v_{\text{dc,pre}} - \frac{NM\hat{I}_{\text{s}}}{8\omega_{\text{s}}C}\sin\varphi + \sqrt{\left(\frac{NM^2 i_{\text{dc,pre}}}{12\omega_{\text{s}}C} - \frac{3NM\hat{I}_{\text{s}}}{16\omega_{\text{s}}C}\cos\varphi\right)^2 + \left(\frac{3NM\hat{I}_{\text{s}}}{16\omega_{\text{s}}C}\sin\varphi\right)^2} \tag{43}$$

where φ is the phase lag of the AC grid current with respect to the inner electromotive force of the converter. Substituting the maximum value $v_{\text{leg,bs}}$ for $v_{j,\text{leg}}$ in (42), the maximum circulating current $i_{\text{cir,bs}}$ at t_{bs} is obtained as

$$i_{\text{cir,bs}} = \left(\frac{i_{\text{dc,pre}}}{3} - \frac{v_{\text{leg,bs}}}{2R_{\text{arm}}}\right)\mathrm{e}^{-\frac{R_{\text{arm}}}{L_{\text{arm}}}t_{\text{bs}}} + \frac{v_{\text{leg,bs}}}{2R_{\text{arm}}}. \tag{44}$$

Insertion of (41) and (44) into (40), the maximum arm current $i_{\text{arm,bs}}$ at the time t_{bs} of blocking submodules is formulated as

$$i_{\text{arm,bs}} = \frac{\hat{I}_{\text{s}}}{2} + \left(\frac{i_{\text{dc,pre}}}{3} - \frac{v_{\text{leg,bs}}}{2R_{\text{arm}}}\right)\mathrm{e}^{-\frac{R_{\text{arm}}}{L_{\text{arm}}}t_{\text{bs}}} + \frac{v_{\text{leg,bs}}}{2R_{\text{arm}}}. \tag{45}$$

Taking into account the overload capability of the IGBTs, the maximum arm current $i_{\text{arm,bs}}$ is required to be smaller than a critical value $i_{\text{arm,crit}}$, that is

$$i_{\text{arm,bs}} \leq i_{\text{arm,crit}}. \tag{46}$$

Insertion of (45) into (46), the principle for the parameter design of the arm inductance is given by

$$L_{\text{arm}} \geq \frac{R_{\text{arm}}t_{\text{bs}}}{\ln\left(\frac{i_{\text{dc,pre}}}{3} - \frac{v_{\text{leg,bs}}}{2R_{\text{arm}}}\right) - \ln\left(i_{\text{arm,crit}} - \frac{\hat{I}_{\text{s}}}{2} - \frac{v_{\text{leg,bs}}}{2R_{\text{arm}}}\right)}. \tag{47}$$

The converter may be overloaded up to 50% of its rated capacity for a short duration [6]. Thus, when applying (47), the critical arm current $i_{\text{arm,crit}}$ may be chosen as 150% of the maximum value of the arm current at rated output power.

B. Selection of Circuit Breaker Interrupting Capability

After blocking of the submodules, the fault currents continue to flow through the freewheeling diodes, as discussed in Section III. Those fault currents cannot be cleared until the circuit breakers are opened [27]. The interrupting capability of the AC circuit breaker is defined as $i_{\text{ac,rupt}}$, which indicates the maximum current that can be successfully interrupted by the circuit breaker. This interrupting capability $i_{\text{ac,rupt}}$ is required to be larger than the maximum value of the AC grid currents at the time t_{ob} of opening AC circuit breakers. Thus, to isolate the fault successfully, the interrupting capability of the AC circuit breaker is determined as

$$i_{\text{ac,rupt}} \geq \max_{j\in\{\text{a,b,c}\}} i_{\text{s}j}(t_{\text{ob}}) \tag{48}$$

where the AC grid current $i_{\text{s}j}$ is obtained from (31) and (32).

VI. Validation

The performance of the developed analytical model is validated by application to a point-to-point MMC-HVDC of the CIGRE B4 DC test system [28]. The configuration of the test system is shown in Fig. 9 with a focus on the converter MMC-1. The main circuit parameters and the fault scenario are described in Section VI-A. In SectionVI-B, the analytical models of the fault currents and voltages are evaluated. The principle of the parameter design of the arm inductor is applied in Section VI-C.

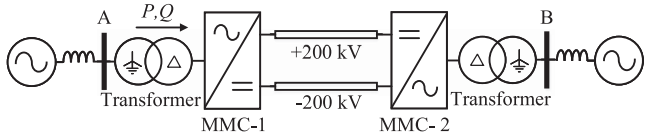

Fig. 9. Point-to-point MMC-HVDC link of CIGRE B4 DC test system.

TABLE II
Fault Scenario of MMC-HVDC Under Pole-to-Pole Fault [28]

Event	Time (ms) after fault
DC fault occurrence at t_0 (applied at 1 s)	0
Blocking submodules of MMC-1 at t_{bs}	0.62
Blocking submodules of MMC-2	1.59
Opening ac circuit breakers of MMC-1 at t_{ob}	62.26
Opening ac circuit breakers of MMC-2	64.72

A. Test System and Fault Scenario

The main circuit parameters of the point-to-point MMC-HVDC system are given in [17]. Each converter has one hundred half-bridge submodules per arm. The DC link voltage of the converter in prefault operation is at $\pm$200 kV. The active power injected from the AC grid into the converter MMC-1 is set to 400 MW, while the reactive power is set to zero.

The events and time sequence of the fault scenario are described in Table II. A metallic pole-to-pole fault occurs at the DC terminal of the converter MMC-1 at 1 s. Due to overcurrent, the submodules of the MMC-1 are blocked at $t_{\text{bs}} = 0.62$ ms after the disturbance. For the converter with half-bridge submodules, the fault currents are eventually interrupted by opening the AC circuit breakers at $t_{\text{ob}} = 62.26$ ms.

B. Validation of Analytical Model of Fault Currents

The analytical result of the DC grid current in Fig. 9 is obtained from (39), while the AC grid currents are calculated by (31) and (32). The upper and lower arm currents in the three legs are obtained from (38). In Figs. 10 and 11, the fault currents are depicted in dotted lines. In order to get reference values, the test system is also implemented in the digital simulator PSCAD at a time step size of 1μs. The numerical simulation results are depicted in solid lines in Figs. 10 and 11. The subscripts A and N are used to distinguish between the analytical and numerical results. The analytical results are shown to closely match the numerical results. The maximum deviation between the analytical and numerical results for the DC grid current is less than 0.05%. The maximum deviations of the AC grid currents and the arm currents are at less than 0.03% and 0.05%, respectively.

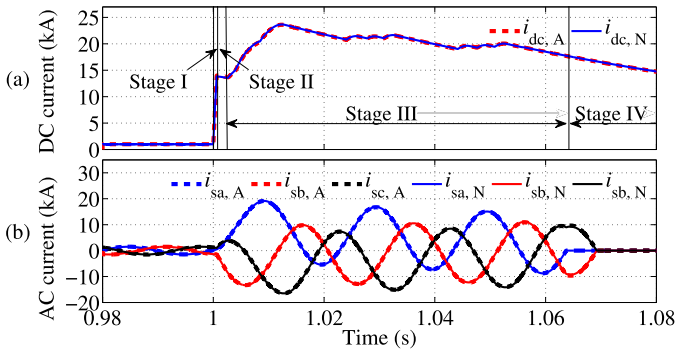

Fig. 10. Analytical and numerical results of (a) DC grid current and (b) AC grid currents.

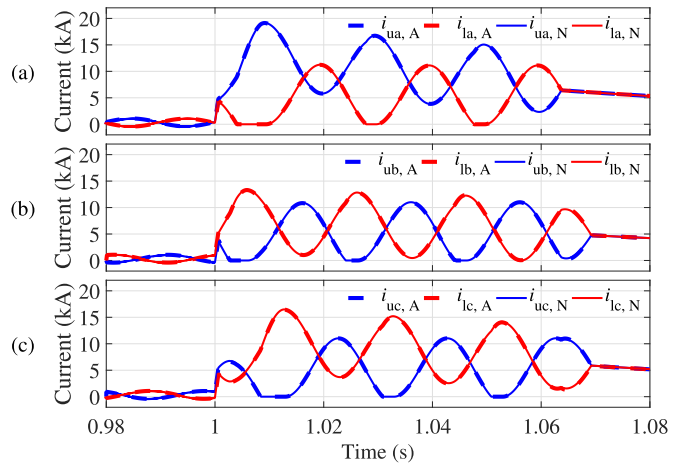

Fig. 11. Analytical and numerical results of upper and lower arm currents in (a) leg a, (b) leg b, and (c) leg c.

The four stages of the transient responses of the MMC under the pole-to-pole fault are annotated in Fig. 10(a). It is shown that the durations of the stages I and II are short, while the durations of the stages III and IV are relatively long. In the stage I, the DC grid current is subject to a steep rise due to the discharging behavior of the capacitors of the submodules, as discussed in Section III-B1. No obvious increase in the AC grid currents is observed since the AC grid operates in quasi-steady state in this stage. In the stage II, the AC grid currents begin to increase since the submodule capacitors in the converter arms are bypassed, resulting in a shorted AC grid. The fault currents cannot be cleared by blocking the submodules for an MMC utilizing half-bridge submodules. Meanwhile, the DC grid current decreases since the submodule capacitors are bypassed, and the AC grid currents cannot feed into the DC grid. It is noticed that the DC grid current and arm currents reach maximum values in the stage III and decay slowly in the stage IV.

C. Validation of Parameter Design of Arm Inductor

The converter arms of the MMC under the pole-to-pole fault suffer from overcurrent, as shown in Fig. 11. The IGBTs may be damaged by overcurrent due to poor overload capability [6].

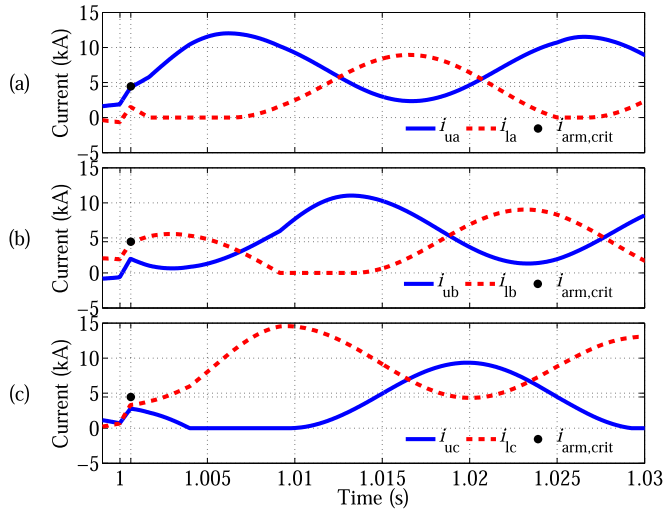

Fig. 12. Analytical and numerical results of upper and lower arm currents in three legs of MMC with arm inductance $L_{\text{arm}} = 0.057$ H.

In order to turn off the IGBTs safely, the arm currents at the time of blocking submodules are required to be smaller than a critical value $i_{\text{arm,crit}}$, as discussed in Section V-A. This critical arm current may be chosen as 150% of the maximum value of the arm current at the rated output power. For the given test system, $i_{\text{arm,crit}}$ is set to 4.454 kA. To respect the overload capability of the IGBTs, the minimum arm inductance is obtained as $L_{\text{arm}} = 0.057$ H according to (47).

To demonstrate the capability of the arm inductors to limit fault currents, an MMC with the arm inductance of $L_{\text{arm}} = 0.057$ H in Fig. 9 is considered. The active power is set to the rated value of 800 MW in the prefault operation, while the reactive power is set to zero. A pole-to-pole fault is applied to the DC terminal of the converter at 1 s. After $t_{\text{bs}} = 0.62$ ms, the submodules are blocked due to overcurrent. The fault scenario is as given in Table II. In Fig. 12, the upper and lower arm currents of the three legs are shown. The critical arm current $i_{\text{arm,crit}} = 4.454$ kA at the time of blocking submodules is marked by a black dot. At the time of blocking submodules, any arm current is shown not to exceed the critical value, while the arm currents i_{ua} and i_{lb} come close to the critical arm current. The other arm currents remain much smaller at this time of blocking submodules. The arm inductance may also be obtained from the commonly used analytical model in [29], [30], in which the capacitor voltage ripples and the AC feeding currents are neglected. The so obtained arm inductance is 0.037 H, which is smaller than 0.057 H. As such, the commonly used parameter design principle of the arm inductance is inaccurate, resulting in arm current exceeding its preset critical value.

VII. Conclusion

An analytical model for the MMC based on half-bridge submodules under the pole-to-pole fault was formulated, illustrated, and validated. The fault currents throughout the DC short-circuit

fault were calculated analytically, taking into account the changing operating states of the switching devices and the resulting changing topologies of the converter.

The overall analytical modeling is distinguished by three contributions. Firstly, generic equivalent circuits of an MMC under the pole-to-pole fault were developed, involving the varying topologies of the converter. The equivalent circuits are applicable throughout the DC fault thanks to the defined binary variables denoting the operating states of the switching devices. Secondly, analytical solutions of the fault currents were formulated based on the proposed generic equivalent circuits. The analytical solutions are valid throughout the four stages of the pole-to-pole fault by updating the binary variables and initial values at the beginning of each stage. The ripple voltages of the submodule capacitors are taken into consideration, providing accurate initial values for the capacitor discharging behavior. The analytical formulas offer a deep insight into the main circuit parameters and the prefault operating point affecting the fault currents. Thirdly, as a promising application, an analytical equation for the design of the arm inductance was provided, taking into consideration the overload capability of the power electronic switching devices. As opposed to a numeric solution, the visibility of all the parameters affecting the design is fully given since the analytic solution was entirely derived through symbolic computations. Such visibility is interesting for follow-up investigation, leading to further advancements in system parameter design and protection configuration of the modular multilevel converter system. In sum, the contributions made offer an illustrative and accurate model of the MMC under the pole-to-pole fault.

APPENDIX

A. Assumptions

To support the analytical modeling of the MMC under the pole-to-pole fault, the following assumptions are made:

1) In steady state, the harmonic components of the circulating current are well suppressed [18].
2) The higher-order harmonic components of the arm voltages are neglected.
3) The pole-to-pole fault is close to the DC terminal of the converter, and therefore R_{dc} and L_{dc} in the DC link are equal to zero, respectively.
4) For any topology as defined by the states of the switching devices, the corresponding equivalent circuit is linear.
5) Shortly after the pole-to-pole fault, the capacitor voltage remains at its predisturbance value due to short discharging period.

B. Ripple Voltages in Converter Arms

The capacitors of the submodules are either inserted or bypassed, depending on the switching actions of power electronic switching devices. The inserted capacitors may be charged or discharged depending on the arm current direction, resulting in ripple voltages. Due to the switching actions, the ripple voltages of the capacitors appear at the AC terminal of the submodule. According to [19], taking into consideration N submodules in one arm, the ripple voltages $v_{\mathrm{u}j,\mathrm{rip}}(t)$ and $v_{\mathrm{l}j,\mathrm{rip}}(t)$ of the upper and lower arms are given by

$$\begin{aligned} v_{\mathrm{u}j,\mathrm{rip}}(t) = &-\frac{NM\hat{I}_{\mathrm{s}}}{16\omega_{\mathrm{s}}C}\sin\varphi + \frac{NMi_{\mathrm{dc}}}{12\omega_{\mathrm{s}}C}\sin(\omega_{\mathrm{s}}t) \\ &- \left(\frac{N\hat{I}_{\mathrm{s}}}{8\omega_{\mathrm{s}}C} + \frac{NM^2\hat{I}_{\mathrm{s}}}{64\omega_{\mathrm{s}}C}\right)\sin(\omega_{\mathrm{s}}t-\varphi) - \frac{NM^2i_{\mathrm{dc}}}{24\omega_{\mathrm{s}}C}\sin(2\omega_{\mathrm{s}}t) \\ &+ \frac{3NM\hat{I}_{\mathrm{s}}}{32\omega_{\mathrm{s}}C}\sin(2\omega_{\mathrm{s}}t-\varphi) - \frac{NM^2\hat{I}_{\mathrm{s}}}{64\omega_{\mathrm{s}}C}\sin(3\omega_{\mathrm{s}}t-\varphi) \end{aligned} \tag{49}$$

$$\begin{aligned} v_{\mathrm{l}j,\mathrm{rip}}(t) = &-\frac{NM\hat{I}_{\mathrm{s}}}{16\omega_{\mathrm{s}}C}\sin\varphi - \frac{NMi_{\mathrm{dc}}}{12\omega_{\mathrm{s}}C}\sin(\omega_{\mathrm{s}}t) \\ &+ \left(\frac{N\hat{I}_{\mathrm{s}}}{8\omega_{\mathrm{s}}C} + \frac{NM^2\hat{I}_{\mathrm{s}}}{64\omega_{\mathrm{s}}C}\right)\sin(\omega_{\mathrm{s}}t-\varphi) - \frac{NM^2i_{\mathrm{dc}}}{24\omega_{\mathrm{s}}C}\sin(2\omega_{\mathrm{s}}t) \\ &+ \frac{3NM\hat{I}_{\mathrm{s}}}{32\omega_{\mathrm{s}}C}\sin(2\omega_{\mathrm{s}}t-\varphi) + \frac{NM^2\hat{I}_{\mathrm{s}}}{64\omega_{\mathrm{s}}C}\sin(3\omega_{\mathrm{s}}t-\varphi) \end{aligned} \tag{50}$$

where N is the number of submodules of one arm; M is the modulation index as in (8); and C is the capacitance of the submodule capacitor.

C. Initial Circulating Current

The initial circulating current $i_{j,\mathrm{cir}}(0_+)$ in leg $j \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ is derived for three cases depending on the arm conducting states of the previous stage. In the first case, both upper and lower arms of leg j are conductive in the previous stage, that is $\varsigma_{\mathrm{u}j}(0_-)=1$ and $\varsigma_{\mathrm{l}j}(0_-)=1$. The initial value $i_{j,\mathrm{cir}}(0_+)$ is equal to the circulating current $i_{j,\mathrm{cir}}(0_-)$ at the end of the previous stage since the circulating current continues to flow in the leg and the DC link. The circulating current $i_{j,\mathrm{cir}}(0_-)$ is weighted by $2\varsigma_{\mathrm{u}j}(0_-)\varsigma_{\mathrm{l}j}(0_-)/(\varsigma_{\mathrm{u}j}(0_-)+\varsigma_{\mathrm{l}j}(0_-))$. This weighting factor is equal to 1 when both the upper and lower arms of one leg are conductive in the previous stage, and it is equal to 0 when one of the upper and lower arms is non-conductive.

In the second case, just the upper arm in leg j is conductive in the previous stage, that is $\varsigma_{\mathrm{u}j}(0_-)=1$ and $\varsigma_{\mathrm{l}j}(0_-)=0$. The upper arm current at the end of that previous stage is given by $i_{\mathrm{s}j}(0_-)$. At the beginning of the present stage, according to (38), the upper arm current is given by $i_{\mathrm{s}j}(0_-)/2+i_{j,\mathrm{cir}}(0_+)$ when both the upper and lower arms in leg j are conductive. The arm currents cannot change suddenly because of the arm inductors. As such, the upper arm current at the beginning of the present stage is the same as at the end of the previous stage, that is $i_{\mathrm{s}j}(0_-)/2+i_{j,\mathrm{cir}}(0_+)=i_{\mathrm{s}j}(0_-)$. The initial value $i_{j,\mathrm{cir}}(0_+)$ is then obtained as $i_{\mathrm{s}j}(0_-)/2$. The term $i_{\mathrm{s}j}(0_-)/2$ is then weighted by $\varsigma_{\mathrm{u}j}(0_-)(\varsigma_{\mathrm{u}j}(0_-)-\varsigma_{\mathrm{l}j}(0_-))$, which is equal to 1 only in this case.

In the third case, only the lower arm in leg j is conductive. Similar to the second case, the initial value is obtained by weighting $-i_{\mathrm{s}j}(0_-)/2$ by $\varsigma_{\mathrm{l}j}(0_-)(\varsigma_{\mathrm{l}j}(0_-)-\varsigma_{\mathrm{u}j}(0_-))$. The weighting factor is equal to 1 only in this case.

By summing up the initial values of the aforementioned three cases, the initial circulating current is obtained as

$$i_{j,\mathrm{cir}}(0_+) = \varsigma_{\mathrm{u}j}(0_+)\,\varsigma_{\mathrm{l}j}(0_+)\cdot \left(\frac{2\varsigma_{\mathrm{u}j}(0_-)\,\varsigma_{\mathrm{l}j}(0_-)}{\varsigma_{\mathrm{u}j}(0_-)+\varsigma_{\mathrm{l}j}(0_-)} i_{\mathrm{cir},j}(0_-) + \left(\varsigma_{\mathrm{u}j}^2(0_-) - \varsigma_{\mathrm{l}j}^2(0_-)\right)\frac{i_{\mathrm{s}j}(0_-)}{2}\right) \tag{51}$$

where $\varsigma_{\mathrm{u}j}(0_+)\varsigma_{\mathrm{l}j}(0_+)$ is employed to honor the fact that the circulating current in the present fault stage exists if both upper and lower arms of one leg are conducting. Without loss of generality, the stage I is taken as an example to illustrate the calculation of $i_{j,\mathrm{cir}}(0_+)$. The arm conducting states in the prefault condition are given by $\varsigma_{\mathrm{u}j}(0_-) = 1$ and $\varsigma_{\mathrm{l}j}(0_-) = 1$. The circulating current at the end of the prefault operation is given as one third of the DC grid current, that is $i_{j,\mathrm{cir}}(0_-) = i_{\mathrm{dc,pre}}/3$. The arm conducting states in stage I are given by $\varsigma_{\mathrm{u}j}(0_+) = 1$ and $\varsigma_{\mathrm{l}j}(0_+) = 1$. Inserting these arm conducting states and $i_{j,\mathrm{cir}}(0_-) = i_{\mathrm{dc,pre}}/3$ into (51), the initial circulating current of stage I is obtained as $i_{j,\mathrm{cir}}(0_+) = i_{\mathrm{dc,pre}}/3$.

D. Maximum Voltage of Inserted Capacitors of one Arm

To obtain the maximum circulating current in (42), the maximum value of the total voltage $v_{j,\mathrm{leg}}$ of the inserted capacitors of one arm is calculated. Referring to $v_{\mathrm{a,leg}}$ in (21), the submodule state σ_{ea} is equal to 1 according to Table I. The total voltage $v_{\mathrm{a,leg}}$ of inserted capacitors in the leg a is rearranged as

$$v_{\mathrm{a,leg}} = v_{\mathrm{dc,pre}} - \frac{NM\hat{I}_{\mathrm{s}}}{8\omega_{\mathrm{s}}C}\sin\varphi - \left(\frac{3NM\hat{I}_{\mathrm{s}}}{16\omega_{\mathrm{s}}C}\sin\varphi\right)\cos(2\omega_{\mathrm{s}}t_0) - \left(\frac{NM^2 i_{\mathrm{dc,pre}}}{12\omega_{\mathrm{s}}C} - \frac{3NM\hat{I}_{\mathrm{s}}}{16\omega_{\mathrm{s}}C}\cos\varphi\right)\sin(2\omega_{\mathrm{s}}t_0)\,. \tag{52}$$

The term $(v_{\mathrm{dc,pre}} - \frac{NM\hat{I}_{\mathrm{s}}}{8\omega_{\mathrm{s}}C}\sin\varphi)$ is constant and independent of the time t_0 of fault occurrence. The remaining two terms of $v_{\mathrm{a,leg}}$ rely on the random time t_0. Focusing on the most severe condition, the maximum value of the sum of those cosine and sine terms is obtained as the root sum square of their amplitudes. Thus, the maximum value of the total voltage of the inserted capacitors of one arm is obtained as given by $v_{\mathrm{leg,bs}}$ in (43).

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Peng Wang was born in Shandong, China in 1988. He received the M.E. degree from Shandong University, Jinan, China, in 2014, and the Dr.-Ing. degree (summa cum laude) from Technische Universität Berlin, Berlin, Germany, in 2020. He is currently working with the School of Electrical Engineering, Shandong University. His research interests include modeling and stability analysis of AC-DC power systems integrated with renewable power generation.

Maren Kuschke received the Dipl.-Ing. and Dr.-Ing. degrees from Technische Universität Berlin, Berlin, Germany, in 2008 and 2014, respectively. She studied electrical engineering with focus on electrical drives, photovoltaics, and electric energy systems with TU Berlin and KTH Stockholm, Stockholm, Sweden. She was the recipient of the VDI Award from the Association of German Engineers in 2009, the IEEE PES German Chapter Best Master Thesis Award in 2010, and the IEEE PES Prize Paper Award 2015.

Kai Strunz received the Dr.-Ing. degree (summa cum laude) from Saarland University, Saarbrücken, Germany, in 2001. He was with Brunel University, Uxbridge, U.K., from 1995 to 1997. From 1997 to 2002, he was with the Division Recherche et Développement of Electricité de France in Paris. From 2002 to 2007, he was an Assistant Professor of electrical engineering with the University of Washington, Seattle, WA, USA. Since 2007, he has been a Professor for Sustainable Electric Networks and Sources of Energy with Technische Universität Berlin, Berlin, Germany. He has been a Guest Professor of the Chinese Academy of Sciences, Beijing, China, since 2017. He was the General Chair of the Conference IEEE PES Innovative Smart Grid Technologies Europe in 2012. He is the Chair of the IEEE PES Subcommittee Distributed Energy Resources and the Co-Chair of the IEEE Working Group Dynamic Performance and Modeling of HVDC Systems and Power Electronics for Transmission Systems. He was the recipient of the IEEE PES Prize Paper Award in 2015, the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS First Prize Paper Award 2015, and the 2020 Best Paper Award in the field of electric machines and drives by IEEE TRANSACTIONS ON ENERGY CONVERSION. On behalf of the Intergovernmental Panel on Climate Change, he acted as the Review Editor for the Special Report on Renewable Energy Sources and Climate Change Mitigation.