Novel Cascaded Switched-Diode Multilevel Inverter for Renewable Energy Integration

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***Abstract*—In this paper, a new topology of two-stage cascaded switched-diode (CSD) multilevel inverter is proposed for medium-voltage renewable energy integration. First, it aims to reduce the number of switches along with its gate drivers. Thus, the installation space and cost of a multilevel inverter are reduced. The spike removal switch added in the first stage of the inverter provides a flowing path for the reverse load current, and as a result, high voltage spikes occurring at the base of the stepped output voltage based upon conventional CSD multilevel inverter topologies are removed. Moreover, to resolve the problems related to dc source fluctuations of multilevel inverter used for renewable energy integration, the clock phase-shifting (CPS) one-cycle control (OCC) is developed to control the two-stage CSD multilevel inverter. By shifting the clock pulse phase of every cascaded unit, the staircase-like output voltage waveforms are obtained and a strong suppression ability against fluctuations in dc sources is achieved. Simulation and experimental results are discussed to verify the feasibility and performances of the two-stage CSD multilevel inverter controlled by the CPS OCC method.**

***Index Terms*—Novel cascaded multilevel inverter, two-stage, one-cycle control.**

I. Introduction

VARIOUS multilevel inverter topologies were proposed in the past decade, which have been extensively studied for renewable energy integration systems [1]–[3]. Fig. 1 shows the block diagram of a renewable energy generation system using a multilevel inverter. It integrates a variety of renewable sources, such as solar energy, wind energy, tide energy and so on and they are connected to a converter to generate DC power, which is stored in a capacitor or battery. After connected to a multilevel inverter, DC power is converted into AC power. It is evident that the multilevel inverter capable of converting a single DC voltage source from a capacitor or battery into an AC voltage source is a key element of most stand-alone renewable energy generation systems. The multilevel inverter topologies, in general, can generate high-quality voltage waveforms, where power switches are operated at a very low frequency [4], [5]. The basic topologies of the existing multilevel converters are divided into three types: the cascaded multilevel inverter topology [6]–[8], the diode-clamped multilevel inverter topology [9], [10] and the flying-capacitor multilevel inverter topology [11], [12]. Among these topologies, the cascaded multilevel converter has attracted more attention due to its simple structure and individual DC power sources for each cascaded unit. It has great potential to be employed in renewable energy generation systems, such as solar energy, wind energy, fuel cells.

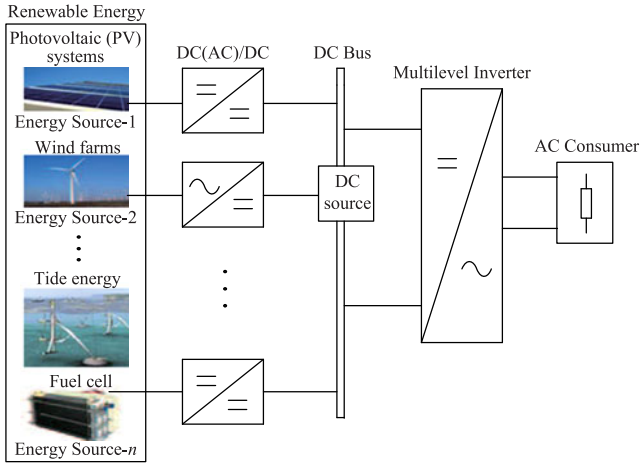

Fig. 1. Renewable energy generation system with multilevel inverter.

The typical cascaded multilevel inverter topology is the cascaded H-bridge (CHB) multilevel inverter, and the primary disadvantage of the CHB topology is the requirement of a high number of switches and its related gate drivers, which may lead to an expensive and complex overall system. Therefore, several new multilevel inverter topologies using a reduced number of switches and related gate drivers were developed in recent years. Among them, a cascaded half-bridge topology proposed by Babaei and Hosseini [13] effectively reduced almost half the number of required switches compared with the CHB topology. Then, Rasoul Shalchi Alishah proposed a cascaded switched-diode topology [14], [15]. Compared with the cascaded half-bridge topology, it can produce more voltage levels with a less number of switches. However, due to the lack of a path for reverse load currents, under a R-L load, high voltage spikes occur at the base of the stepped output voltage, which tend to deteriorate power quality. This paper presents a novel two-stage CSD multilevel topology, achieving a higher number of voltage levels with a lower number of switches, which also removes high voltage spikes under R-L loads by adding a path for reverse load currents.

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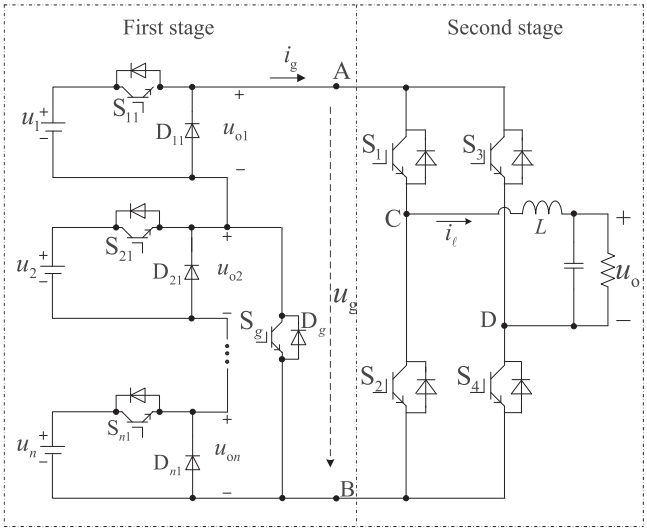


Fig. 2. The structure of the proposed two-stage CSD topology.

Meanwhile, the commonly used modulation strategies for cascaded multilevel inverters are the fundamental frequency control method, the carrier based sinusoidal PWM (SPWM), the space vector modulation (SVM) [2], [16]–[18] and some nonlinear modulation methods, such as hysteresis control [19], [20], sliding mode control [21] and so on. However, in a renewable energy integration system, DC power sources of a multilevel inverter are supplied by the renewable energy generation, as shown in Fig. 1. In practice, the DC supply is always with fluctuation because of all sorts of complex factors. For instance, outputs of solar cells change in a certain range following variations of light intensity, temperatures, and so on, which manifest as an output mixed with low frequency ripples. When using such a DC supply as the input of multilevel converters, conventional modulation methods are unable to meet the need of industrial applications. Hence, there is a necessity to develop a universal control method with an accurate static performance and a strong suppression ability against the interference in DC sources. In this paper, a CPS OCC method is developed for controlling the proposed CSD multilevel topology. By shifting the phase of the triggering clock pulses of every cascaded unit, the staircase-like output voltage waveforms are obtained and a strong inhibition ability against the interference in DC sources is achieved.

The paper is organized as follows: The proposed two-stage CSD multilevel topology is introduced in Section II, and the advantages of the two-stage CSD topology are demonstrated compared with the CHB and cascaded half-bridge topologies in Section III. Section IV illustrates the design and implementation procedures of the CPS OCC method. In Sections V and VI, simulation and experimental results are presented. The conclusions are drawn in Section VII.

II. Topology of The Proposed Two-Stage CSD Multilevel Inverter

Fig. 2 illustrates the proposed two-stage CSD topology, which comprises a n cascaded switched-diode converter with one spike removal switch $S_{\rm g}$ and a full-bridge inverter, where n is the number of the cascaded basic units. The basic unit 1 shown in Fig. 2 consists of a DC voltage source (or a capacitor with a DC voltage equal to u_1), a switch S_{11} with its internal reverse diode and a diode $\rm D_{11}$. It is clear that the parallel connection of the diode $\rm D_{11}$ avoids the shoot-through phenomenon of a bridge arm. Two values can be obtained for $u_{\rm o1}$ of the basic unit 1, which are u_1 when switch S_{11} conducts and 0 when switch S_{11} is turned off. The spike removal switch $S_{\rm g}$, connected between unit 2 and unit n, provides a flowing path for the reverse load current. When S_{11} is on, $S_{21}\cdots S_{n1}$ is off, $S_{\rm g}$ is turned on.

TABLE I
Values of $u_{\rm g}$ With Respect to Switch States of the First Stage

State	Switches states						$u_{\rm g}$
	S_{11}	S_{21}	S_{31}	$\cdots$	$S_{(n-1)1}$	S_{n1}	
1	off	off	off	$\cdots$	off	off	0
2	on	off	off	$\cdots$	off	off	u_1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$
n	off	off	off	$\cdots$	off	on	u_n
$n+1$	on	on	off	$\cdots$	off	off	u_1+u_2
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$
2^n	on	on	on	$\cdots$	on	on	$\sum_{i=1}^{n} u_i$

TABLE II
Values of $u_{\rm o}$ With Respect to Switch States of the Second Stage

State	Switches states				$u_{\rm o}$	Condition
	S_1	S_2	S_3	S_4		
1	on	off	off	on	$u_{\rm g}$	$u_{\rm ref}\geqslant 0$
2	off	on	on	off	$-u_{\rm g}$	$u_{\rm ref}<0$

The cascading layout of n basic units and $S_{\rm g}$ form the first stage, as shown in Fig. 2. The maximum output voltage of the first stage is given as follows:

$$u_{\rm g}=u_{\rm o1}+u_{\rm o2}+\cdots+u_{\rm on}. \tag{1}$$

and for states of switches S_{11}, S_{21}, $\cdots$, $S_{(n-1)1}$, S_{n1}, 2^n different values of $u_{\rm g}$ are obtained, as listed in Table I.

As shown in Table I, the first-stage converter can generate positive staircase-like output voltage waveforms. For generating both positive and negative output voltages, the second stage converter is needed. Table II lists the switch state analysis with respect to the positive sign or negative sign of a reference voltage $u_{\rm ref}$. It is clear that the employment of the second-stage achieves both the positive and negative halves of the output voltage.

Under the symmetric case, that is, all the DC voltage sources are equal to $u_{\rm dc}$, the number of output voltage levels $N_{\rm level}$ and the total number of switches $N_{\rm IGBT}$ required are calculated as follows, respectively.

$$N_{\rm level}=2n+1 \tag{2}$$

$$N_{\rm IGBT}=n+5 \tag{3}$$

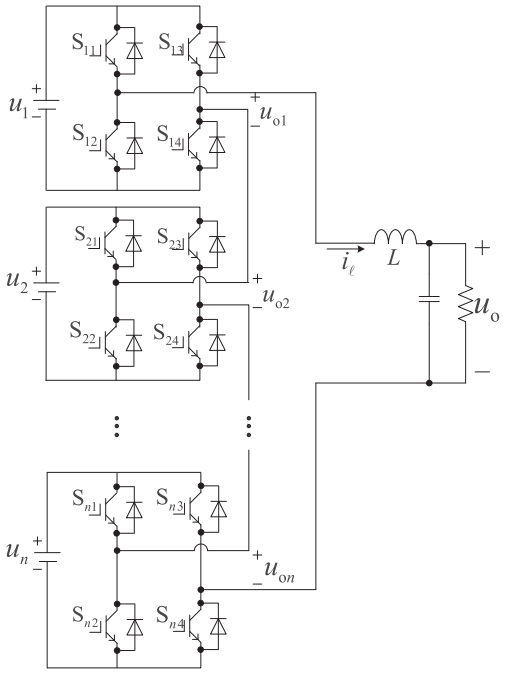


Fig. 3. The CHB multilevel topology.

then the number of the required switches for a $N_{\rm level}$ output voltage is derived as follows:

$$N_{\rm IGBT} = \frac{N_{\rm level} + 9}{2}. \tag{4}$$

III. Comparison With Topologies of CHB and Cascaded Half-Bridge

The CHB topology consists of n DC sources or cells each connected to a H-bridge inverter, as shown in Fig. 3. Each H-bridge can generate three levels of voltage output, i.e., $u_{\rm dc}$, 0 and $-u_{\rm dc}$, respectively. Under the symmetric case, the number of the required switches for a $N_{\rm level}$ output voltage is derived as follows:

$$N_{\rm IGBT} = 2N_{\rm level} - 2. \tag{5}$$

Compared with the CHB topology, a cascaded half-bridge topology proposed by Babaei and Hosseini [13] effectively reduces almost half the number of switches, as shown in Fig. 4. It is composed of a n cascaded half-bridge converter and a full-bridge inverter. Under the symmetric case, the number of the required switches for a $N_{\rm level}$ output voltage is derived as follows:

$$N_{\rm IGBT} = N_{\rm level} + 3. \tag{6}$$

The main purpose of this proposed CSD topology is to reduce the number of required switches against required voltage levels, since switches define the reliability, circuit size, cost and control complexity. Another important factor in designing a multilevel converter is the rating of switches. Therefore, the comparison of the power component requirements among the CHB, the cascaded half-bridge and the proposed CSD topologies is listed

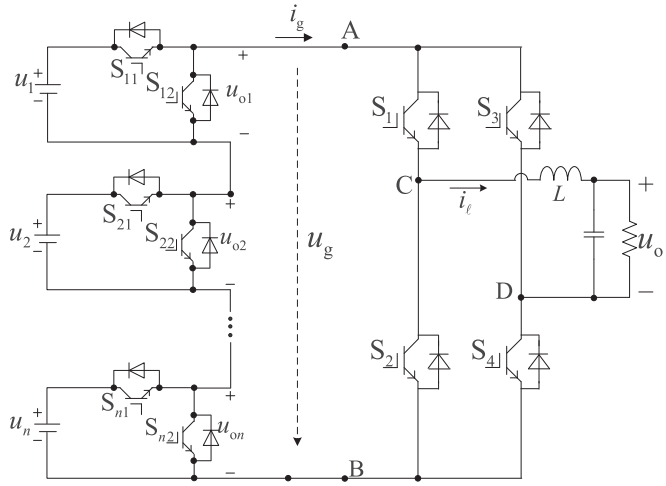


Fig. 4. Inverter topology by Babei and Hosseini [13].

in Table III concerning the number of required switches and voltage rating of all the devices (switches and diodes).

Based on (4)–(6) , the number of required switches and drivers for realizing $N_{\rm level}$ voltages for output are compared in Table III. Fig. 5 illustrates the results of the comparison $N_{\rm IGBT}$ against $N_{\rm level}$ from different points. As the figure shows, under the symmetric case, the CSD topology requires a less number of IGBTs and its related gate drivers for realizing $N_{\rm level}$ output voltage. For instance, to generate a 21-level output voltage, the CSD topology (Point 3) needs 15 IGBTs/drivers. However, the CHB topology (Point 1) and cascaded half-bridge topology (Point 2) require 40 IGBTs/drivers and 24 IGBTs/drivers, respectively. Although there are 10 diodes added in the proposed topology, the required number of the IGBTs and its related gate drivers are greatly reduced from 40 (CHB) or 24 (cascaded half-bridge) to 15 (two-stage CSD). Such reductions are more remarkable with the increase of the output levels. The analysis under the asymmetric case is similar to that of the symmetric case, and the number reduction of required switches along with drivers is more remarkable.

The voltage and current rating of devices is an important factor in designing inverters. In the three topologies, the currents of all the devices are equal to the rated current of loads. However, this is not true for the voltage rating [13], [14]. Suppose that the multiplication of voltage rating per device is represented by:

$$u_{\rm device} = \sum_{i=1}^{n} u_{\rm switch,i} + \sum_{j=1}^{n} u_{\rm diode,j}. \tag{7}$$

where $u_{\rm switch,i}$ and $u_{\rm diode,j}$ represent the voltage rating of the ith switch and jth diode, respectively.

Equation (7) can be considered as a criterion for the comparison of different topologies concerning the voltage rating of devices. A lower criterion indicates that a smaller voltage is applied at the terminal of the devices of the topology. As listed in Table III, for realizing $N_{\rm level}$ output voltages, the voltage rating of switches $S_{11} - S_{n1}$, diodes $\rm D_{11} - D_{n1}$ (CSD) and switches $S_{11} - S_{n2}$ (Cascade half-bridge) is less than that of switches $S_{11} - S_{n4}$ (CHB). However, the full-bridge directing switches

TABLE III
COMPARISON OF POWER COMPONENT REQUIREMENTS

	CHB	Cascaded half-bridge	CSD
Maximum output voltage	$u_{\rm dc}(\frac{N_{\rm level}-1}{2})$	$u_{\rm dc}(\frac{N_{\rm level}-1}{2})$	$u_{\rm dc}(\frac{N_{\rm level}-1}{2})$
Number of switches (IGBTs and drivers)	$2(N_{\rm level}-1)$	$N_{\rm level}+3$	$\frac{N_{\rm level}+9}{2}$
Voltage rating of $S_{11}-S_{n4}$ (CHB); $S_{11}-S_{n2}$ (Half-bridge); $S_{11}-S_{n1}, \rm D_{11}-D_{n1}$ (CSD)	$2u_{\rm dc}(N_{\rm level}-1)$	$u_{\rm dc}(N_{\rm level}-1)$	$u_{\rm dc}(N_{\rm level}-1)$
Voltage rating of $S_{\rm g}$ (CSD)	N/A	N/A	$\frac{u_{\rm dc}(N_{\rm level}-3)}{2}$
Voltage rating of $\rm S_1-S_4$ (Half-bridge, CSD)	N/A	$2u_{\rm dc}(N_{\rm level}-1)$	$2u_{\rm dc}(N_{\rm level}-1)$
Voltage rating of all the switches and diodes	$2u_{\rm dc}(N_{\rm level}-1)$	$3u_{\rm dc}(N_{\rm level}-1)$	$3u_{\rm dc}(N_{\rm level}-1)+\frac{u_{\rm dc}(N_{\rm level}-3)}{2}$

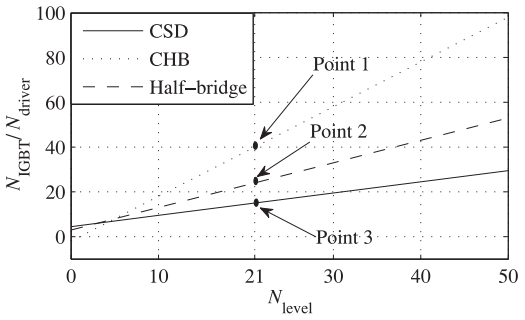


Fig. 5. Number of IGBTs and drivers against the number of voltage levels.

$S_1 - S_4$ in the CSD and cascaded half-bridge contribute to a total voltage rating equal to the entire CHB, thus the CSD and cascaded half-bridge have higher total power switch cost over the CHB. Besides, there is a spike removal switch S_g in the first stage of the proposed CSD topology. It is connected between cascaded unit 2 and unit n, which blocks high voltage. Adding the voltage rating of S_g, as listed in Table III, the proposed CSD topology has the highest total voltage rating. This indicates that the voltage rating of the spike removal switch in the first stage and the full-bridge directing switches in the output side lead to the restriction on high-voltage applications. As a result, the proposed CSD topology is more suitable for medium-voltage ($2.3, 3.3, 4.16$ or 6.9 kV) applications [4].

IV. THE PROPOSED CPS OCC METHOD FOR THE TWO-STAGE CSD MULTILEVEL INVERTER

A. The Design of CPS OCC

Fig. 6 displays the diagram of the proposed CPS OCC method for controlling the proposed two-stage CSD multilevel inverter. As shown in Table II, the positive and negative halves of output waveforms are implemented by the second stage of the multilevel inverter through comparing the reference voltage $u_{\rm ref}$ with zero. Thus the CPS OCC is designed for the first stage, which only considers the positive state. The structure indicates that every cascaded basic unit of the first stage has an independent OCC controller, which is similar but with a phase-shift for $T_{\rm s}/n$ of the clock pulse, where $T_{\rm s}$ represents the switching cycle of the multilevel inverter. The main principal of the OCC controller is to control the average voltage or current in a switch cycle by cycle, forcing it to be equal to a desired value [22]. For every

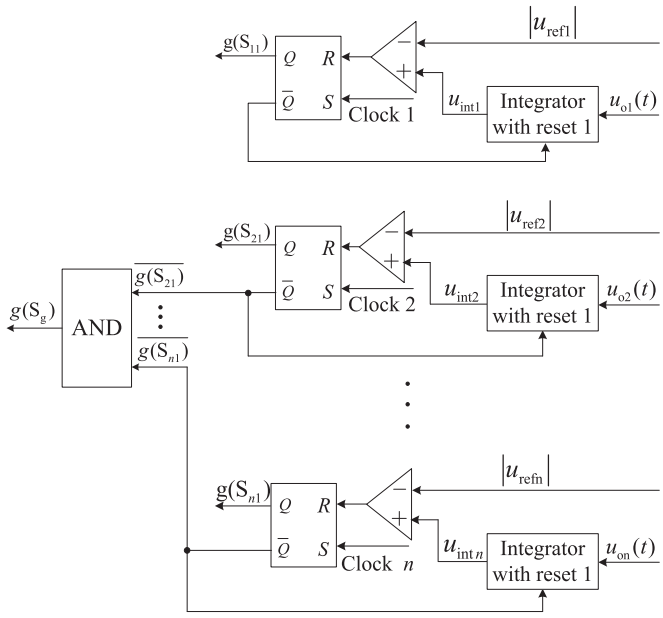


Fig. 6. The control diagram of CPS OCC for the two-stage CSD inverter.

cascaded unit, e.g., unit 1, it means that, during the $n^{\rm th}$ switching cycle $[(n-1)T_{\rm s}, nT_{\rm s})$, the average value of $u_{\rm o1}$ is equal to the reference value $u_{\rm ref1}$, as

$$\frac{1}{T_{\rm s}}\int_{(n-1)T_{\rm s}}^{(n-1)T_{\rm s}+T_{\rm s}} u_{\rm o1}(t)dt = |u_{\rm ref1}|. \tag{8}$$

The analysis of the topology in Section II shows that there are two values for $u_{\rm o1}$ of the basic unit 1, which are u_1 when S_{11} conducts and 0 when S_{11} is turned off. The state analysis shows that the DC source u_1 works in the time interval from $(n-1)T_{\rm s}$ to $(n-1)T_{\rm s}+t_{\rm on}(n)$. Thus, the control equation of CPS OCC for unit 1 is expressed as

$$\frac{1}{T_{\rm s}}\int_{(n-1)T_{\rm s}}^{(n-1)T_{\rm s}+T_{\rm on}} u_1(t)dt = |u_{\rm ref1}|. \tag{9}$$

At the base of the stepped sinusoidal wave, when $u_{\rm o}$ changes from positive to negative or from negative to positive, there may be two values of $u_{\rm o}$: when $S_{11}-S_{n1}$ are all turned off, $u_{\rm o}=0$. In this switching state, $i_\ell = 0$, therefore, there is no reverse load current when $u_{\rm o}$ changes from positive to negative or from negative to positive. When S_{11} is on and $S_{21}-S_{n1}$ are

turned off, $u_{\rm o} = u_1$. In this switching state, $i_\ell \neq 0$, therefore, there is a reverse load current under a R-L load. If there is no $S_{\rm g}$, high voltage spikes are produced at the base of the stepped sinusoidal wave. This is because the reverse load current i_ℓ is blocked by the diode of $D_{21}, \cdots, D_{n1}$, abruptly decreasing the current flowing in the inductive component of the load, and subsequently the inductive components of the load produce a high voltage spike due to the collapsing magnetic field in a very short time. In the proposed two-stage CSD topology, a spike removal switch $S_{\rm g}$ is connected between unit 2 and unit n to provide a flowing path for the reverse load current. The control signal of $S_{\rm g}$ is obtained by simple logic functions, as shown in Fig. 6. When $S_{21} \cdots S_{n1}$ are off, $S_{\rm g}$ is turned on. Then the reverse load current flows through the loops ($S_1 \rightarrow S_{11} \rightarrow {\rm u}_1 \rightarrow {\rm S_g} \rightarrow {\rm S}_4$) or ($S_3 \rightarrow S_{11} \rightarrow {\rm u}_1 \rightarrow {\rm S_g} \rightarrow {\rm S}_2$). Thus, the high voltage spikes at the base of the stepped sinusoidal wave are removed.

B. The Implementation of CPS OCC

CPS OCC is implemented with simple logic functions (comparison and integration) as shown in Fig. 6. Here, the implementation for control of basic unit 1 is described as follows: the integration process starts at the moment when S_{11} is turned on by a fixed frequency clock pulse. At this moment, $u_{\rm o1}(t) = u_1(t)$. As time goes on, the integration value $u_{\rm int1}(n)$ increases from its initial value:

$$u_{\rm int1}(t) = \int_{(n-1)T_{\rm s}}^{t} u_1(t)dt. \tag{10}$$

and $u_{\rm int1}(t)$ is compared with the control reference $u_{\rm ref1}$ instantaneously. At the instant when $u_{\rm int1}(t)$ reaches $u_{\rm ref1}$, the comparator generates a reset pulse to reset the RS flip-flop ($Q = 0$). Then S_{11} is changed from the on-state to off-state. At the same time, the integrator is reset to zero. At this moment $u_{\rm o1}(t) = 0$. Switch S_{11} is off until the arrival of the next clock pulse, which starts the $(n+1)^{\rm th}$ switching cycle.

As the design and implementation for other cascaded basic units are similar to that of unit 1, the details of other units are not presented here.

V. Simulation Results

Simulations are undertaken to demonstrate the feasibility and performances of the proposed two-stage CSD multilevel inverter using the CPS OCC method. In simulation studies, a 5-level and a 9-level two-stage CSD multilevel inverter with a switching frequency of 2500 Hz are built. The parameters are $u_1 = u_2 = \cdots = u_n = 80$ V, $R = 60\ \Omega$, $L = 10$ mH, $C = 2.2\ \mu$F, $u_{\rm ref1} = u_{\rm ref2} = \cdots = u_{\rm refn} = 60$ V. To evaluate the ability of the CPS OCC method to suppress DC source fluctuations, a comparative study with the carrier phase shifted-sinusoidal pulse width modulation (CPS-SPWM) is presented for controlling the multilevel inverter in the renewable energy integration system, as shown in Fig. 1. Here, low frequency ripples are added into DC voltages to simulate DC sources with fluctuations supplied by renewable energy generations.

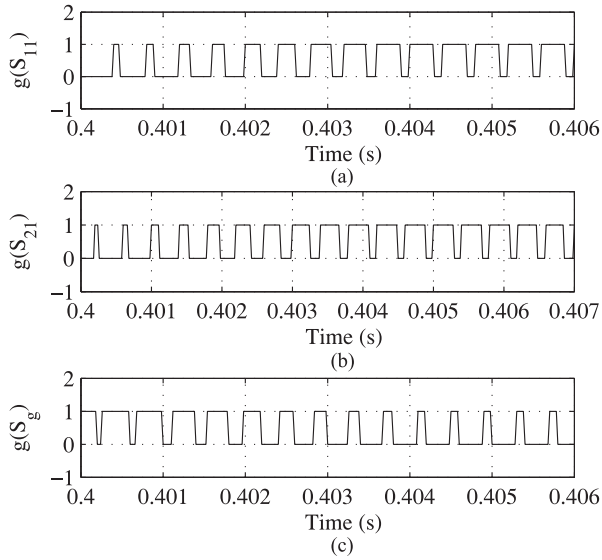


Fig. 7. The gate signals of the first stage of the 5-level simulation prototype.

A. The Operation of CPS OCC

Fig. 7 shows the gate signals of the first-stage converter. The clock pulse of each cascaded unit is shifted by $T_{\rm s}/n$, where $T_{\rm s}$ is the switching period and n is the number of the cascaded units of the first-stage converter. And the gate signal of the spike removal switch S_g is shown in Fig. 7(c). From Fig. 7(c), it can be seen that when S_{21} is off, $S_{\rm g}$ is turned on. Then, at the base of the sinusoidal wave, the reverse load current flows through the loop ($S_1 \rightarrow S_{11} \rightarrow {\rm u}_1 \rightarrow {\rm S_g} \rightarrow {\rm S}_4$) or ($S_3 \rightarrow S_{11} \rightarrow {\rm u}_1 \rightarrow {\rm S_g} \rightarrow {\rm S}_2$). Thus, the high voltage spikes occurring in the convention topology at the base of the stepped sinusoidal wave are removed.

The gate signals of the second-stage inverter are shown in Fig. 8. By comparing $u_{\rm ref}$ with zero, S_1 and S_4 conduct when $u_{\rm ref} \geq 0$. In this state, the output voltage $u_{\rm o} = u_{\rm g}$. When $u_{\rm ref} < 0$, S_1 and S_4 are turned off and S_2 and S_3 are turned on. In this state, the output voltage $u_{\rm o} = -u_{\rm g}$ for the negative half cycle. Thus both the positive and negative halves of output waveforms are obtained.

The output voltage $u_{\rm g}$ of the first-stage converter, which is the sum of the outputs of all the cascaded units, has zero and positive values, as shown in Fig. 9(a). And the output current $i_{\rm g}$ of the first-stage converter shown in Fig. 9(b) is also positive.

Fig. 10 illustrates the stepped output voltage waveform $u_{\rm CD}$, the output voltage $u_{\rm o}$ and the inductor current i_ℓ. As shown, $u_{\rm CD}$ is a staircase waveform of 50 Hz, and there is no high voltage spikes at the base of the stepped sinusoidal wave. Meanwhile, the output voltage and current are almost sinusoidal after the $(L-C)$ filter. The total harmonic distortion (THD) of the stepped output voltage waveform $u_{\rm CD}$ of the 5-level multilevel inverter is 41.91%, as shown in Fig. 11. The frequencies of the main harmonics focusing on is twice of the switching frequency (2500 Hz) and its multiples.

Then the output voltage $u_{\rm g}$ and current $i_{\rm g}$ of the first-stage converter of the 9-level multilevel inverter are shown in Fig. 12. As the figure shows, $u_{\rm g}$ and current $i_{\rm g}$ are positive. The 9-level

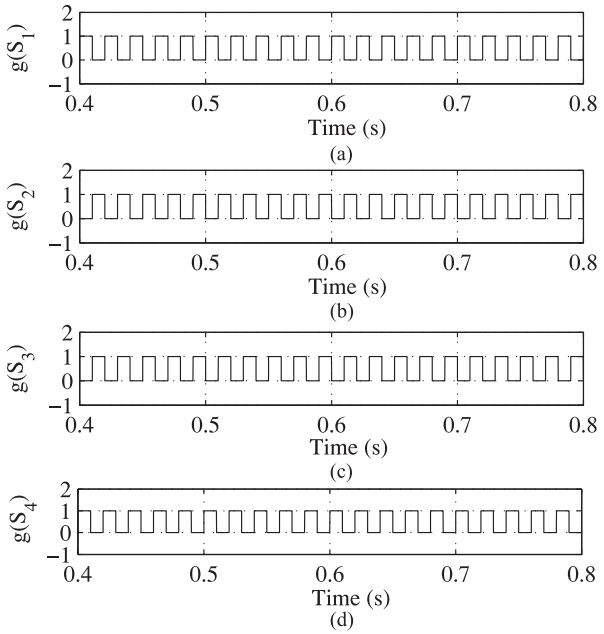


Fig. 8. The gate signals of the second stage of the 5-level simulation prototype.

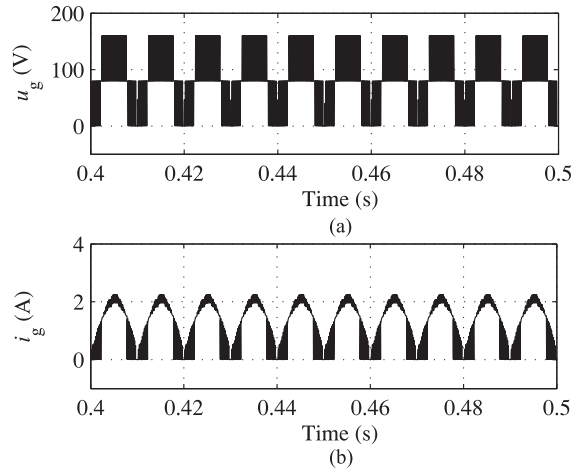


Fig. 9. The output voltage and current of the first stage converter of the 5-level simulation prototype. (a) Output voltage $u_{\rm g}$; (b) Output current $i_{\rm g}$.

stepped output voltage waveform is displayed in Fig. 13(a), which is a 50 Hz staircase waveform with an amplitude of 320 V, and there is no high voltage spike at the base of the stepped sinusoidal wave. The output voltage and current, as shown in Fig. 13(b) and (c), are almost sinusoidal after passing through the $(L-C)$ filter. The THD of stepped output voltage waveform $u_{\rm CD}$ of the 9-level multilevel inverter is 16.82%, as shown in Fig. 14. And the frequency that the main harmonics focusing on is 4 times of the switching frequency (2500 Hz) and its multiples. Compared with the THD of stepped output voltage waveform of the 5-level multilevel inverter, the THD is lower and the frequencies that the main harmonics focusing on moves backward, thus releasing output filter requirements for the compliance of output voltage harmonic standards.

It is clear that the CPS OCC method is feasible for the proposed two-stage CSD multilevel inverter.

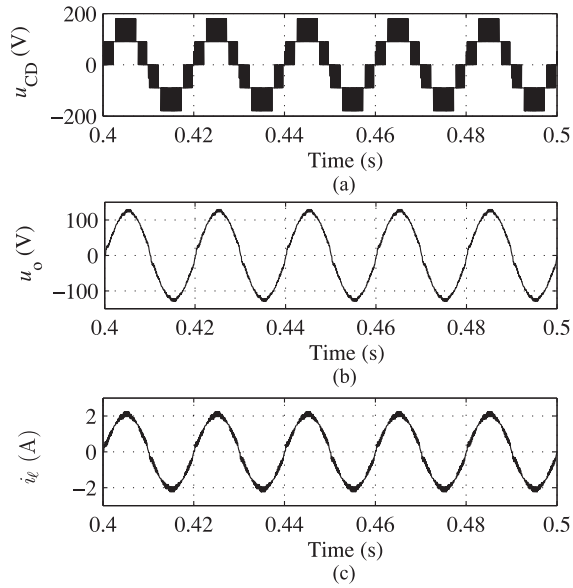


Fig. 10. The output voltage and inductor current of the 5-level simulation prototype. (a) Output voltage $u_{\rm CD}$; (b) Output voltage after filter $u_{\rm o}$; (c) Inductor current i_ℓ.

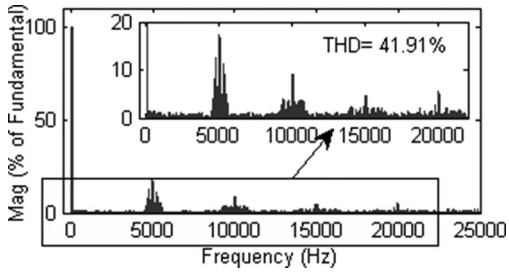


Fig. 11. The FFT analysis result of the stepped voltage $u_{\rm CD}$ of the 5-level multilevel inverter.

B. The Suppression Ability Against Interferences in DC Sources

To evaluate the performances of CPS OCC, the DC sources with fluctuations supplied by renewable energy generations are simulated by adding low frequency interferences in DC voltages $(u_1, u_2, \ldots, u_n)$ of the multilevel inverter. Figs. 15 and 16 demonstrate the ability of CPS OCC to resist the unbalance or low frequency ripples in DC sources of the 5-level case.

Fig. 15 shows the simulation results under unbalance DC sources (there is a 10 Hz ripple with an amplitude 16 V in the DC source of the basic unit 1). The comparisons demonstrate that the output voltage $u_{\rm o}$ using CPS SPWM contains corresponding ripples from the DC source, as shown in Fig. 15(b). In contrast, using CPS OCC, the output voltage $u_{\rm o}$ is kept as a stable output, as shown in Fig. 15(a). Similarly, when the DC sources of the 5-level multilevel inverter contain low frequency ripples (there is a 10 Hz ripple with an amplitude 8 V in the DC sources of basic unit 1 and 2, respectively). The results of Fig. 16(a) and (b) illustrate that the output voltage $u_{\rm o}$ using CPS SPWM contains corresponding ripples. In comparison, using CPS OCC, the output voltage $u_{\rm o}$ is kept as a consistant output.

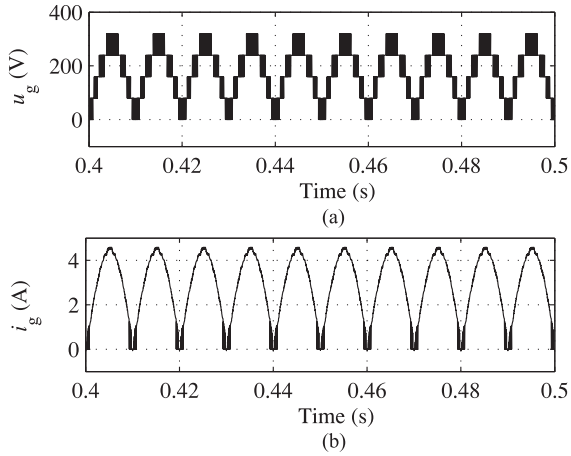


Fig. 12. The output voltage and current of the first stage converter of the 9-level simulation prototype. (a) Output voltage $u_{\rm g}$; (b) Output current $i_{\rm g}$.

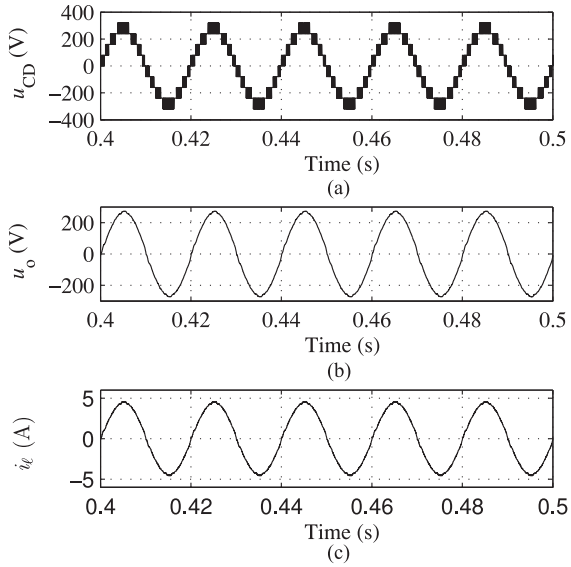


Fig. 13. The output voltage and inductor current of the 9-level simulation prototype. (a) Output voltage $u_{\rm CD}$; (b) Output voltage after filter $u_{\rm o}$; (c) Inductor current i_ℓ.

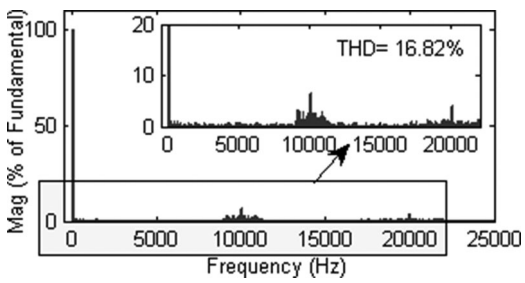


Fig. 14. The FFT analysis result of the stepped voltage $u_{\rm CD}$ of the 9-level multilevel inverter.

VI. Experimental Verification

In this research, a 5-level hardware prototype with identical parameters to that of the simulation model is constructed. In the experiment, the voltage and current measurements are sampled using HALL sensors CHV-25P and CHB-25NP/6 A,

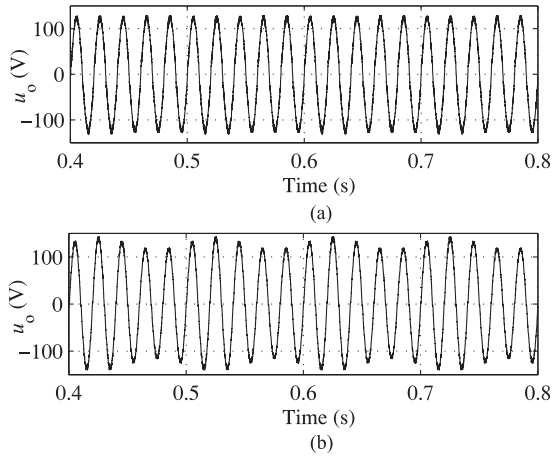


Fig. 15. The simulation results of the 5-level prototype: DC source with basic unit 1 contains a 10 Hz ripple with amplitude 16 V. (a) $u_{\rm o}$ using CPS OCC; (b) $u_{\rm o}$ using CPS SPWM.

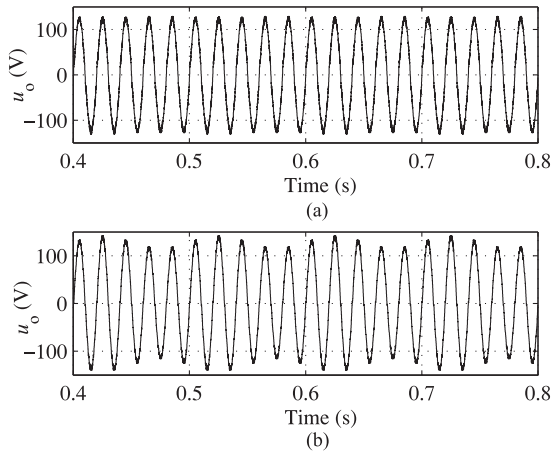


Fig. 16. The simulation results of the 5-level prototype: DC source with each basic unit contains a 10 Hz ripple with amplitude 8 V. (a) $u_{\rm o}$ using CPS OCC; (b) $u_{\rm o}$ using CPS SPWM.

respectively. The IGBT gate drivers are based on SKYPER 32R, which are powered with 0/15 V. All the experiments are implemented using dSPACE DS1104. To verify the performances of CPS OCC, a comparative study with CPS SPWM is carried out for the cases of unbalanced DC sources and DC sources with low frequency ripples. In this study, the unbalance or the low-frequency ripple of DC sources are generated by a function generator SUIN TFG1900B. Since the maximum current of the function generator is 400 mA, the load resistance of the prototype is changed to $R = 400\ \Omega$ under the cases of unbalanced DC sources and DC sources with low frequency ripples.

A. The Operation of CPS OCC

Fig. 17 demonstrates the operation results of the 5-level multilevel inverter using CPS OCC. It can be observed that the experimental results are consistent with the simulation results in Figs. 9 and 10. The output voltage and current of the first-stage converter have zero or positive values. The 5-level staircase waveform is implemented and the output voltage and

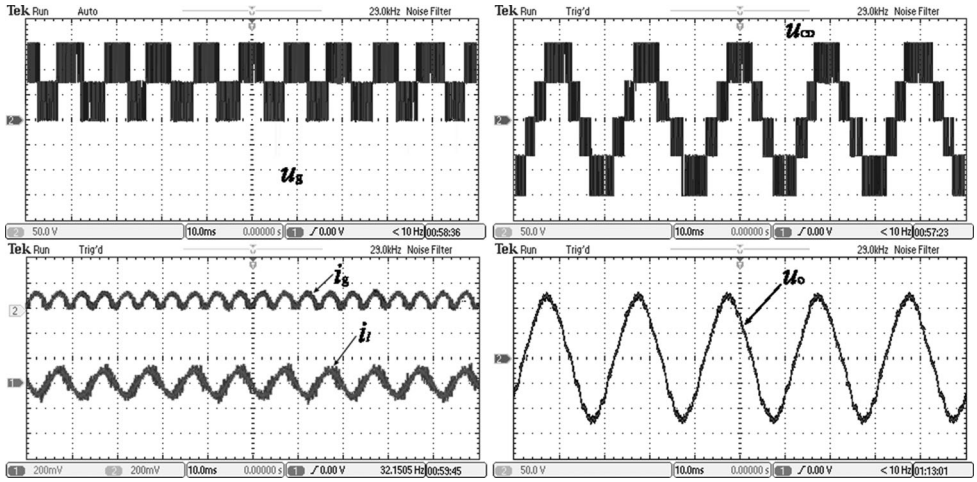
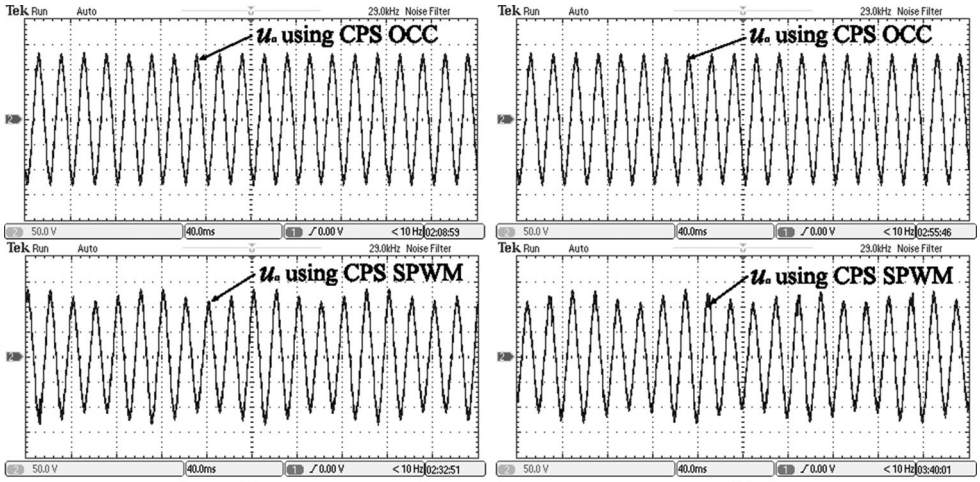


Fig. 17. The experimental results of the 5-level prototype using CPS OCC.



(a) (b)

Fig. 18. The experimental results of the 5-level prototype. (a) DC source of each unit contains a 10 Hz ripple with amplitude 8 V; (b) DC source of the basic unit 1 contains a 10 Hz ripple with amplitude 16 V.

current are almost sinusoidal after passing through the $(L-C)$ filter.

B. The Suppression Ability Against Interferences in DC Sources

Fig. 18 shows the comparison results of the 5-level multilevel inverter employing the CPS OCC and the CPS SPWM under the cases of unbalanced DC sources and DC sources with low frequency ripples, respectively. It demonstrates that the experimental results are consistent with the simulation results of Figs. 15 and 16. The output voltage using CPS SPWM contains corresponding ripples due to the fluctuations in DC sources. However, the output voltage using CPS OCC is always kept as a consistant output.

VII. Conclusion

A new topology of two-stage CSD multilevel inverter has been proposed in this paper. n cascaded basic units and one spike removal switch form the first stage. Then by adding a full-bridge inverter as the second-stage converter, both of the positive and negative output voltage levels are generated. Since the one full-bridge converter in the output side leads to the restriction on high-voltage applications, the proposed topology is suitable for medium-voltage renewable energy integration. The comparisons with the CHB and cascaded half-bridge topologies show that the CSD topology requires less switches and related gate drivers for realizing $N_{\rm level}$ output voltage. As a result, the installation space and cost of the multilevel inverter are reduced. Meanwhile, the spike removal switch added in the first stage provides a flowing path for the reverse load current under R-L loads, thus, the high voltage spikes, due to the collapsing magnetic field in a very short time interval, are removed.

The CPS OCC method, which is composed by n similar but dependent OCC controllers, has been designed and implemented to control the CSD multilevel inverter. Simulation and experimental results demonstrate that, by shifting the clock pulse phase

of each cascaded unit, the staircase-like voltage waveforms are obtained. Moreover, to evaluate the performance of CPS OCC, in both the simulation and experiment, the DC sources mixed with low frequency ripples are implemented to simulate the DC supply from renewable energy generations, and the comparative results between CPS OCC and CPS SPWM reveal that CPS OCC possesses a superior ability in suppressing the unbalance or low frequency ripples in DC sources. These results demonstrate that the CPS OCC method can be a substitute for conventional controllers to control multilevel inverters for renewable energy integration with improved control performances.

REFERENCES

[1] M. S. B. Ranjiana, P. S. Wankhade, and N. D. Gondhalekar, "A modified cascaded H-bridge multilevel inverter for solar applications," in *Proc. 2014 Int. Conf. Green Comput. Commun. Elect. Eng.*, 2014, pp. 1–7.

[2] F. S. Kang, S. J. Park, S. E. Cho, C. U. Kim, and T. Ise, "Mutilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[3] L. V. Nguyen, H.-D. Tran, and T. T. Johnson, "Virtual prototyping for distributed control of a fault-tolerant modular multilevel inverter for photovoltaics," *IEEE Trans. Energy Convers.*, vol. 29, no. 4, pp. 841–850, Dec. 2014.

[4] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Mutilevel inverters: A survey of topologies, controls, and application," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] F. Z. Peng and J. S. Lai, "Mutilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[6] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[7] F. Khoucha, M. S. Lagoun, A. Kheloui, and M. E. H. Benbouzid, "A comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 64–72, Mar. 2011.

[8] M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, "Integrating hybrid power sources into an islanded MV microgrid using CHB multilevel inverter under unbalanced and nonlinear load conditions," *IEEE Trans. Energy Convers.*, vol. 28, no. 3, pp. 643–651, Sep. 2013.

[9] S. A. Khajehoddin, A. Bakhshai, and P. K. Jain, "A simple voltage balancing scheme for m-level diode-clamped multilevel converters based on a generalized current flow model," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2248–2259, Sep. 2008.

[10] A. Nami, F. Zare, G. Ledwich, A. Ghosh, and F. Blaabjerg, "Comparison between symmetrical and asymmetrical single phase multilevel inverter with diode-clamped topology," in *Proc. 2008 IEEE Power Electron. Spec. Conf.*, 2008, pp. 2921–2926.

[11] H. Sepahvand, K. A. Corzine, M. Ferdowsi, and M. Khazraei, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, Feb. 2012.

[12] A. Khoshkbar-Sadigh, V. Dargabi, and K. Corzine, "New flying-capacitor-based multilevel converter with optimized number of switches and capacitors for renewable energy integration," *IEEE Trans. Energy Convers.*, vol. 31, no. 3, pp. 846–859, Sep. 2016.

[13] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum of switches," *Energy Convers. Manage.*, vol. 50, no. 4, pp. 2761–2767, 2009.

[14] D. N. R. S. Alishah and S. H. Hosseini, "Novel topologies for symmetric, asymmetric, and cascade switched-diode mutilevel converter with minimum number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5300–5310, Oct. 2014.

[15] R. S. Alishah and D. Nazarpour, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electron.*, vol. 7, no. 1, pp. 96–104, 2013.

[16] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. T. Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Elect. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, 2007.

[17] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[18] B. N. Roodsari and E. P. Nowicki, "Fast space vector modulation algorithm for multilevel inverters and its extension for operation of the cascaded H-bridge inverter with non-constant DC sources," *IET Power Electron.*, vol. 6, no. 7, pp. 1288–1298, 2013.

[19] A. Shukla, A. Ghosh, and A. Joshi, "Hysteresis modulation of multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1396–1409, May 2011.

[20] S. Gautam and R. Gupta, "Switching frequency derivation for the cascaded multilevel inverter operating in current control mode using multiband hysteresis modulation," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1480–1489, Mar. 2014.

[21] R. Gupta, A. Ghosh, and A. Joshi, "Multi-band hysteresis modulation and switching characterization for sliding mode controlled cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2344–2353, Jul. 2010.

[22] K. M. Smedley and S. Cuk, "One-cycle control of switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 625–633, Nov. 1995.

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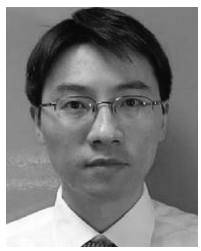

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